PART 5 MARCH 1971

Digital Integrated Circuits

Linear Integrated Circuits

SEMICONDUCTORS AND INTEGRATED CIRCUITS

Part 5 **March 1971**

DATA HANDBOOK SYSTEM

To provide you with a comprehensive source of information on electronic components, subassemblies and materials, our Data Handbook System is made up of three series of handbooks, each comprising several parts.
The three series, identified by the colours noted, are:

ELECTRON TUBES (9 parts) BLUE

SEMICONDUCTORS AND INTEGRATED CIRCUITS (5 parts) RED

COMPONENTS AND MATERIALS (5 parts) GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued annually; the contents of each series are summarized on the following pages.
We have made every effort to ensure that each series is as accurate, comprehensive and up-to-date as possible, and we hope you will find it to be a valuable source of reference. Where ratings or specifications quoted differ from those published in the preceding edition they will be pointed out by arrows. You will understand that we can not guarantee that all products listed in any one edition of the handbook will remain available, or that their specifications will not be changed, before the next edition is published. If you need confirmation that the pusblished data about any of our products are the latest available, may we ask that you contact our representative. He is at your service and will be glad to answer your inquiries.

January 1970

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 — **January 1971**

Transmitting tubes (Tetrodes, Pentodes)
Associated accessories

Part 2 — **February 1970**

Tubes for microwave equipment

Part 3 — **March 1970**

Special Quality tubes
Miscellaneous devices

Part 4 — **April 1970**

Receiving tubes

Part 5 — **May 1970**

Cathode-ray tubes
Photo tubes
Camera tubes
Photoconductive devices
Associated accessories

Part 6 — **June 1970**

Photomultiplier tubes
Scintillators
Photoscintillators
Radiation counter tubes
Semiconductor radiation detectors
Neutron generator tubes
Associated accessories

Part 7 — **July 1970**

Voltage stabilizing and reference tubes
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
Ignitrons
Industrial rectifying tubes
High-voltage rectifying tubes

Part 8 — **August 1970**

T.V. Picture tubes

Part 9 — **January 1971**

Transmitting tubes (Triodes)
Tubes for R.F. heating (Triodes)
Associated accessories

January 1971

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Diodes and Thyristors — **September 1970**

General
Signal diodes
Tunnel diodes
Variable capacitance diodes
Voltage regulator diodes
Rectifier diodes
Thyristors, diacs, triacs
Rectifier stacks
Accessories
Heatsinks

Part 2 Low frequency; Deflection — **October 1970**

General
Low frequency transistors (low power)
Low frequency power transistors
Deflection transistors
Accessories

Part 3 High frequency; Switching — **November 1970**

General
High frequency transistors
Switching transistors
Accessories

Part 4 Special types — **December 1970**

General
Transmitting transistors
Microwave devices
Field effect transistors
Dual transistors
Microminiature devices for thick- and thin-film circuits
Beam lead devices for thick- and thin-film circuits
Photo devices
Accessories

Part 5 Integrated Circuits — **March 1971**

General
Digital integrated circuits
DTL (FC family)
TTL (FJ family)
MOS (FD family)
Linear integrated circuits

COMPONENTS AND MATERIALS (GREEN SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Circuit Blocks, Input/Output Devices — **September 1970**

Circuit blocks 100 kHz Series
Circuit blocks 1-Series
Circuit blocks 10-Series
Circuit blocks 20-Series
Circuit blocks 40-Series
Counter modules 50-Series
Norbits 60-Series, 61-Series
Circuit blocks 90-Series
Circuit blocks for ferrite core memory drive
Input/output devices

Part 2 Resistors, Capacitors — **December 1970**

Fixed resistors
Variable resistors
Non-linear resistors
Ceramic capacitors
Polyester, polycarbonate, polystyrene, paper capacitors
Electrolytic capacitors
Variable capacitors

Part 3 Radio, Audio, Television — **February 1971**

FM tuners
Coils
Piezoelectric ceramic resonators and filters
Loudspeakers
Audio and mains transformers
Television tuners
Components for black and white television
Components for colour television
Deflection assemblies for camera tubes

Part 4 Magnetic Materials, White Ceramics — **March 1970**

Ferrites for radio, audio and television
Ferroxcube potcores and square cores
Microchokes
Ferroxcube transformer cores
Piezoxide
Permanent magnet materials

Part 5 Memory Products, Magnetic Heads, Quartz Crystals, Microwave Devices, Variable Transformers, Electro-mechanical Components — **June 1970**

Ferrite memory cores
Matrix planes, matrix stacks
Complete memories
Magnetic heads
Quartz crystal units, crystal filters
Isolators, circulators
Variable mains transformers
Electro-mechanical components

Technology relating to the products described in this publication is shared by the following companies.

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FAPESA I.y.C.
Melincué 2594
Tel. 50-9941/8155
BUENOS AIRES

Australia
Philips Industries Ltd.
Miniwatt Electronics Division
20, Herbert St.
Tel 43-2171
ARTARMON, N.S.W.

Austria
WIVEG
Zieglergasse 6
Tel. 93 26 22
1072 WIEN

Belgium
M.B.L.E.
80, rue des Deux Gares
Tel. 23 00 00
1070 BRUSSELS

Brazil
IBRAPE S.A.
Av. Paulista, 2073-S/Loja
Tel. 93-5141
SAO PAULO

Canada
Philips Electron Devices
116, Vanderhoof Ave.
Tel. 425-5161
TORONTO 17, Ontario

Chile
Philips Chilena S.A.
Av. Santa Maria 0760
Tel. 39 40 01
SANTIAGO

Colombia
SADAPE S.A.
Calle 19, No.5-51
Tel. 422-175
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Miniwatt A/S
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DK-2400 KØBENHAVN NV

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Oy Philips A.B.
Elcoma Division
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HELSINKI 10

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La Radiotechnique-Compelec
Avenue Ledru Rollin 130
Tel. 797-99-30
PARIS 11

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Valvo Haus
Burchardstrasse 19
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Elcoma Division
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St. George's Building 21st Fl.
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Varsovia No.36
Tel. 5-33-11-80
MEXICO 6, D.F.

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Boschdijk, VB
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Tel. 24/6701
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Turk Philips Ticaret A.S.
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United States
Amperex Electronic Corp.
Electron Tubes Div.
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HICKSVILLE N.Y.

Sem. and Microcircuits Div.
Tel. 401-762-9000
SLATERSVILLE R.I. 02876

Electronic Components Div.
Tel. 516-234-7000
HAUPPAGE N.Y.

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Luzilectron S.A.
Rondeau 1567, piso 5
Tel. 9 43 21
MONTEVIDEO

Venezuela
C.A. Philips Venezolana
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CARACAS

General

PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.
The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.
Values cited as typical are given for information only.
For an explanation of the type designation code, see the section Type Designation.
For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.
If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.
Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.
Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.
Dual in-line packages have a notch at one end to identify pin 1.
Take care not to mistake adventitious moulding marks for the pin 1 identification.
Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.
Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE

The type number consists of three letters followed by three figures (sometimes followed by a version letter*)
For the purpose of type designation integrated circuits are divided in four groups:
- Digital family circuits
- Digital solitary circuits
- Analogue (including linear) circuits
- Mixed digital/analogue circuits

DIGITAL FAMILY TYPES

First two letters: family
Third letter: circuit function
First two figures: serial number
Third figure: operating ambient temperature range

DIGITAL SOLITARY TYPES

First letter: "S"
Second letter: extension of serial number
Third letter: circuit function
First two figures: serial number
Third figure: operating ambient temperature range

ANALOGUE (LINEAR) TYPES

First letter: "T"
Second and third letter: extension of serial number
First two figures: serial number
Third figure: operating ambient temperature range

MIXED DIGITAL/ANALOGUE TYPES

First letter: "U"
Second and third letter: extension of serial number
First two figures: serial number
Third figure: operating ambient temperature range

*The version letter denotes a variant with respect to electrical performance and/or encapsulation

FUNCTION

H = Combinatorial circuit
J = Bistable or multistable sequential circuit
K = Monostable sequential circuit
L = Level converter
N = Bimetastable or multimetastable sequential circuit
Q = Read/write memory circuit
R = Read-only memory circuit
S = Sense amplifier
Y = Miscellaneous

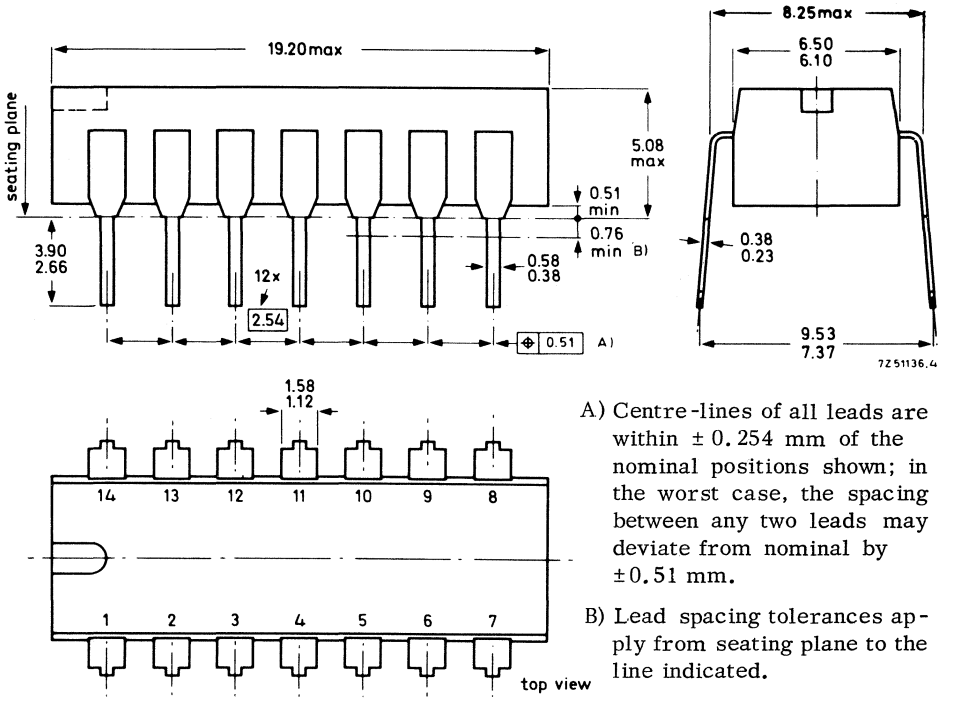
OPERATING AMBIENT TEMPERATURE RANGE

1 = 0 to + 70 °C or wider
2 = −55 to +125 °C or wider
3 = −10 to + 85 °C or wider
4 = +15 to + 55 °C or wider
5 = −25 to + 70 °C or wider
6 = −40 to + 85 °C or wider
0 = Open

PACKAGE OUTLINES

14 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

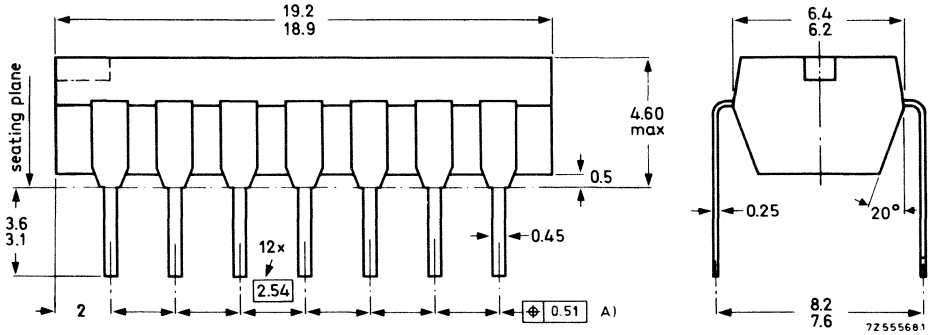
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

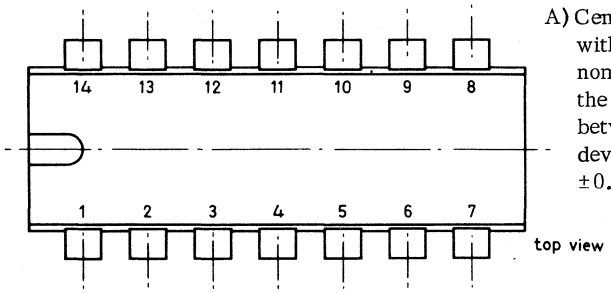
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

14 LEAD PLASTIC DUAL IN-LINE (type B)

Dimensions in mm





A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown: in the worst case, the spacing between any two leads may deviate from nominal by ±0.51 mm.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for more than 5 seconds.

2. By dip or wave

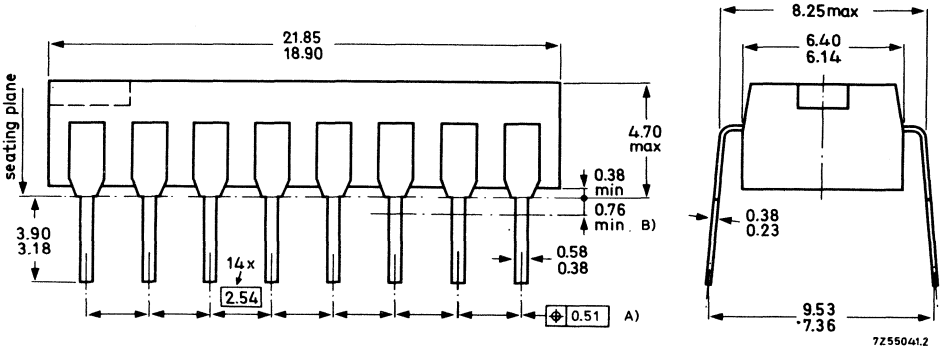
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

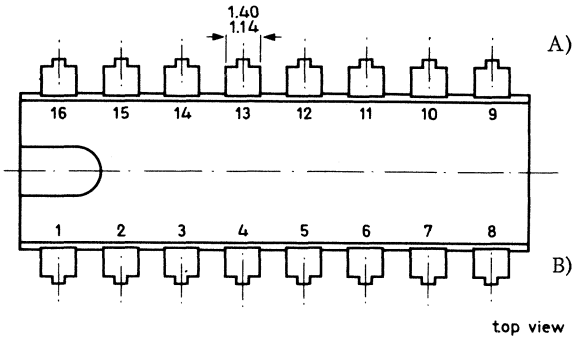
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm





A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

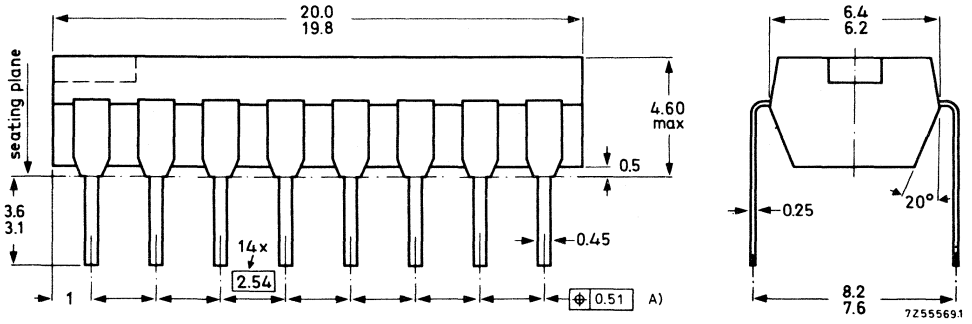
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

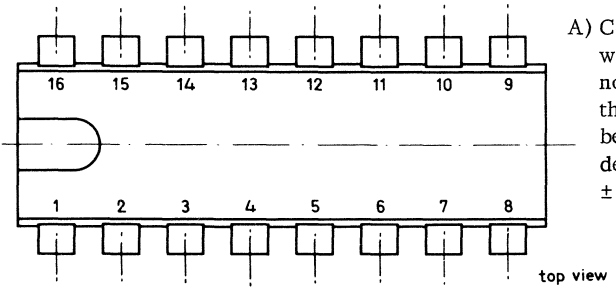
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE (type B)

Dimensions in mm





A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

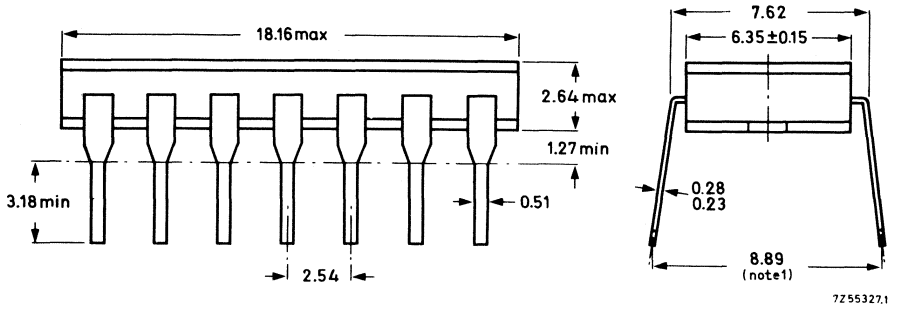
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

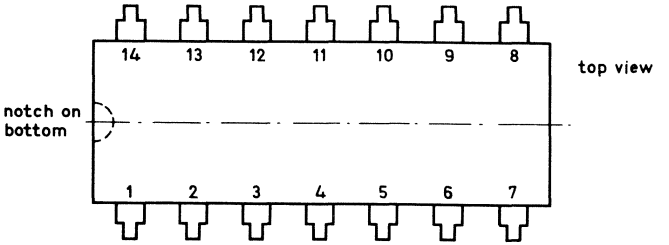
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

14 LEAD METAL-CERAMIC DUAL IN-LINE

Dimensions in mm

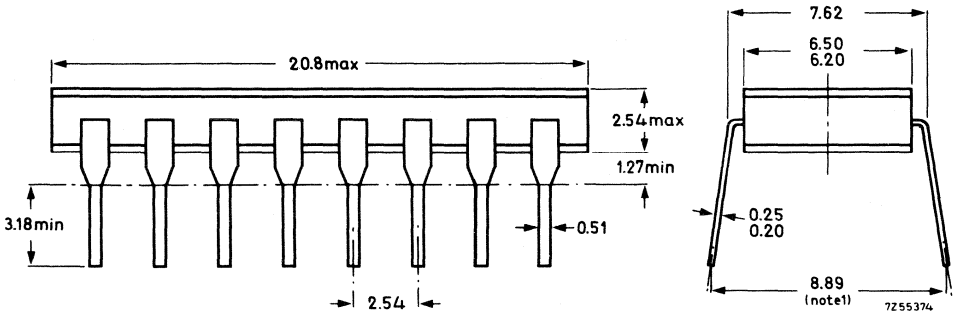


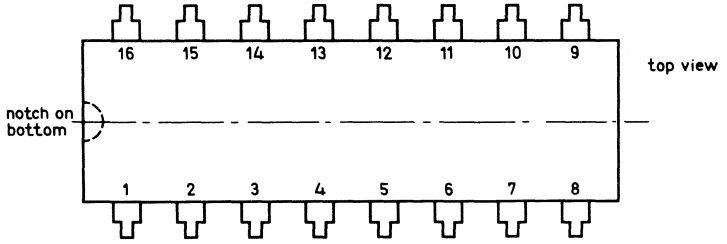


1. Leads on opposite sides are designed to fit in holes 7.62 mm apart. They are given positive misaligment so that they grip after insertion.
2. Pin 1 is normally marked by a dot.

16 LEAD METAL-CERAMIC DUAL IN-LINE

Dimensions in mm

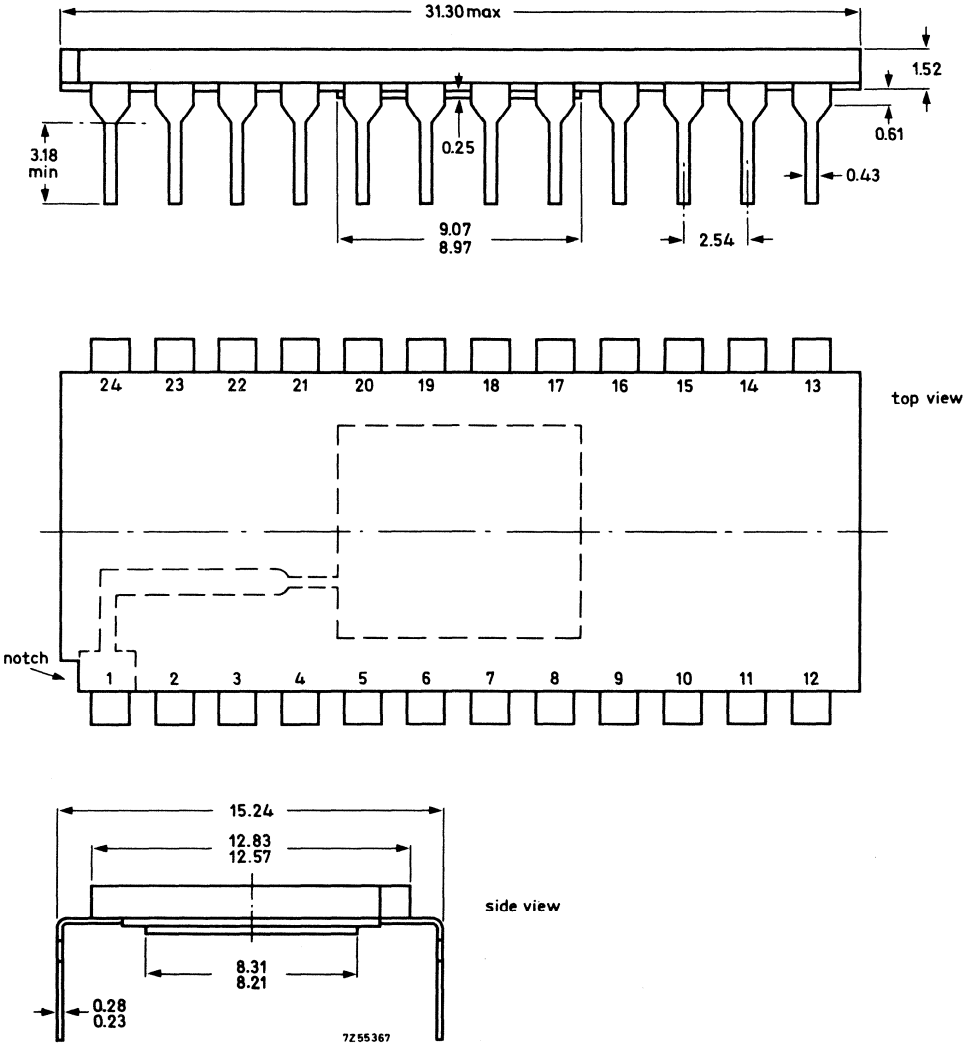




1. Leads on opposite sides are designed to fit in holes 7.62 mm apart. They are given positive misaligment so that they grip after insertion.
2. Pin 1 is normally marked by a dot.

24 LEAD METAL-CERAMIC DUAL IN-LINE

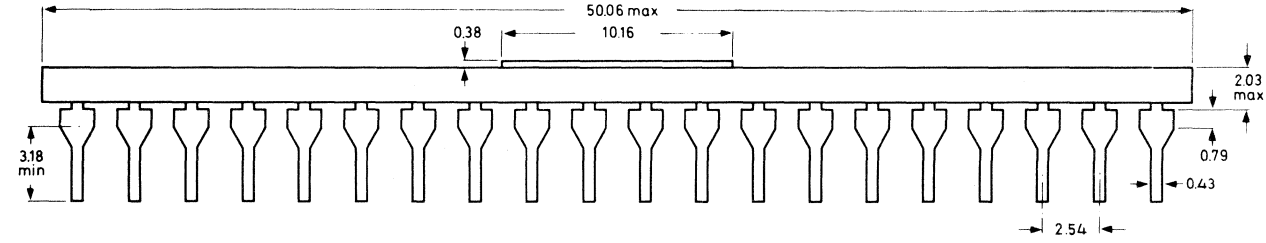
Dimensions in mm

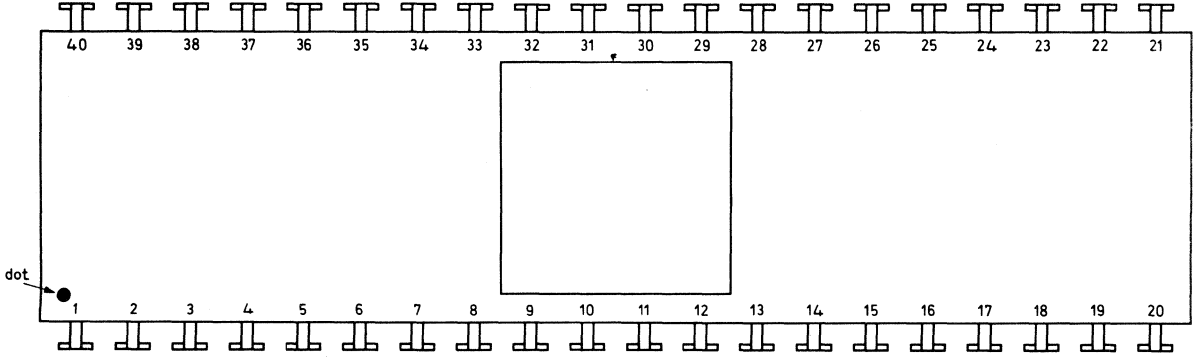


Notes

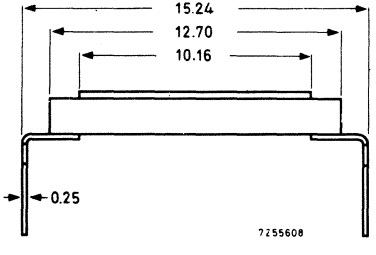
1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a notch and connected to the metal lid on the bottom of the package.

40 LEAD METAL-CERAMIC DUAL IN-LINE





top view



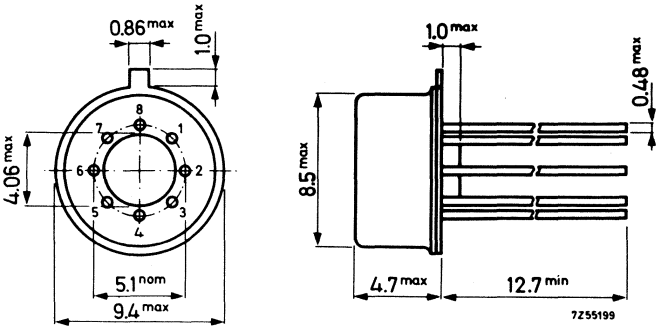
side view

Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a dot.
3. Dimensions in mm.

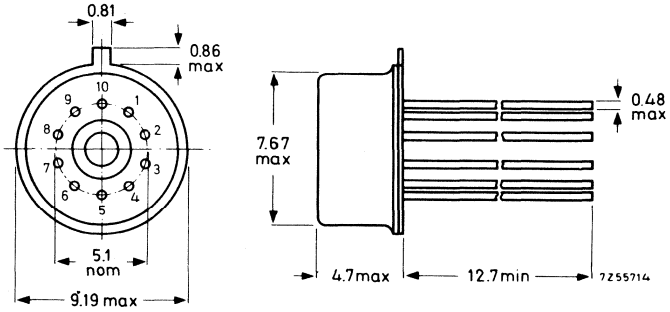
TO-99 METAL ENVELOPE

Dimensions in mm



TO-100 METAL ENVELOPE

Dimensions in mm



GATE SYMBOLS

Symbols taken from MIL-STD-806B published 26-2-1962 together with the explanation given in the MIL-STD are framed (the number in brackets refers to the section of the MIL-STD from which the extract has been made).
Other symbols and explanations are unframed.

A. LOGIC SYMBOLS (5 partial)*)

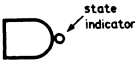
AND The symbol shown below represents the AND function (5.1).

OR The symbol shown below represents the OR function (5.2).

EXCLUSIVE-OR The symbol shown below represents the Exclusive-OR function (5.6).

STATE INDICATOR (Active) (5.3). The presence of the small circle symbol at the input(s) or output(s) of a function indicates:

(a) Input Condition. The electrical condition at the input terminal(s) which control the active state of the respective function.
(b) Output Condition. The electrical condition existing at the output terminal(s) of an activated function.



(5.3.1) A small circle(s) at the input(s) to any element (logical or non-logical) indicates that the relatively LOW (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively HIGH (H) input signal activates the function.
(5.3.2) A small circle at the symbol output indicates that the output terminal of the activated function is relatively LOW (L), the absence indicates that the output terminal is relatively HIGH (H).
This small circle shall never be drawn by itself on a diagram.

On pages 4 and 5 the terms HIGH and LOW and the translation of logic notations "0" and "1" into HIGH and LOW will be elucidated.

*) See appendix for drawing dimensions.

EXAMPLES

AND (5.1.1)

A	B	X
L	L	L
H	L	L
L	H	L
H	H	H

The output is HIGH if and only if all inputs are HIGH.

(5.4)

A	B	X
L	L	H
H	L	H
L	H	H
H	H	L

The output is LOW if and only if all inputs are HIGH

OR (5.2.1)

A	B	X
L	L	L
H	L	H
L	H	H
H	H	H

The output is HIGH if and only if any one or more of the inputs are HIGH.

(5.5)

A	B	X
L	L	H
H	L	L
L	H	L
H	H	L

The output is LOW if and only if any one or more of the inputs are HIGH.

EXCLUSIVE-OR (5.6.1)

A	B	X
L	L	L
H	L	H
L	H	H
H	H	L

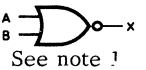
The output is HIGH if and only if any one input is HIGH and all other inputs are LOW.

A	B	X
L	L	H
H	L	L
L	H	L
H	H	H

The output is LOW if and only if any one input is HIGH and all other inputs are LOW.

Table I, (5.7) of MIL-STD-806B, shows two-input AND and OR gate symbols with all the possible combinations of terminals with or without state indicator. It will be noted that the AND-gate symbol in the 1st column has the same function table as the OR-gate symbol in the 2nd column.

Table I

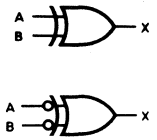
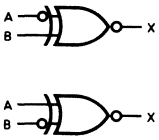
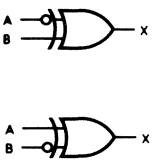
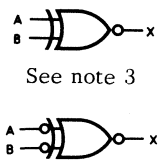
AND	OR	Function Table A	B	X
		H	H	H
		H	L	L
		L	H	L
		L	L	L
		H	H	L
		H	L	L
		L	H	H
		L	L	L
		H	H	L
		H	L	H
		L	H	L
		L	L	L
	 See note 1	H	H	L
		H	L	L
		L	H	L
		L	L	H
		H	H	H
		H	L	H
		L	H	H
		L	L	L
		H	H	H
		H	L	L
		L	H	H
		L	L	H
		H	H	H
		H	L	H
		L	H	L
		L	L	H
 See note 2		H	H	L
		H	L	H
		L	H	H
		L	L	H

Note 1. In literature often described as NOR.
Note 2. In literature often described as NAND.

Although the MIL-STD-806B does not use the expression NAND and NOR they are referred to becaused these terms are commonly used.

Although MIL-STD-806B shows the EXCLUSIVE-OR symbol only without state indicator, for the sake of completeness Table II shows it with all the possible combinations of terminals with or without state indicator. It will be noted from the table that one function table (3rd column) is applicable to four symbols.

Table II

Symbol	Symbol	Function Table
		A B | X H H | L H L | H L H | H L L | L
		A B | X H H | H H L | L L H | L L L | H

See note 3

Note 3. In literature described as BINARY COMPARATOR

HIGH AND LOW

The terms relatively HIGH and relatively LOW are explained with reference to the following three examples

+5 volts = HIGH
+0.5 volts = LOW

+0.5 volts = HIGH
-5 volts = LOW

-5 volts = HIGH
-10 volts = LOW

It can be seen that the more positive voltage is termed relatively HIGH and the less positive is termed relatively LOW. These terms are abbreviated to HIGH (H) and LOW (L) respectively and are used throughout MIL-STD-806B.

LOGICAL "1" AND "0"

In deviation from MIL-STD-806B Appendix B, which for the sake of fully general systems applicability (page 17, fig.5) refrains from establishing any fixed relations between "active-nonactive" and "logical 0-1", we have in the following rules chosen to relate "active" to "1" and "non-active" to "0", as being most suitable when regarding each gate function separately.

"0" at the input always symbolizes the non-activating signal or, at the output, the signal from a non-activated gate;

"1" at the input always symbolizes the activating signal or, at the output, the signal from an activated gate. (The expression activated does not mean that current must flow at the respective terminal(s) but refers to the influence of inputs upon the output(s) of the respective gates.)

The translation from the logic notation into the electrical levels HIGH and LOW is explained with the aid of two examples, one without state indicators and one with. In each case a two-input AND gate truth table is drawn up, and a function table corresponding to the symbol is given so that a direct comparison can be made.

For inputs or outputs	without state indicator	with state indicator
	Logic 1 = HIGH (H)	Logic 1 = LOW (L)
	Logic 0 = LOW (L)	Logic 0 = HIGH (H)

EXAMPLE

Truth Table

Inputs A	Inputs B	Output X
0	0	0
1	0	0
0	1	0
1	1	1

Symbol

Function Table

Inputs A	Inputs B	Output X
L	L	L
H	L	L
L	H	L
H	H	H

Inputs A	Inputs B	Output X
0	0	0
1	0	0
0	1	0
1	1	1

Inputs A	Inputs B	Output X
H	L	H
L	L	H
H	H	H
L	H	L

B. DRAWING PRACTICE

Any of the symbols from Tables I and II may be used in diagrams, bearing in mind the following general rule.
Every signal line shall preferably have at each end
either a state indicator circle,
or no state indicator circle.
An example showing how compliance with this rule can be achieved is given in the following sketch.

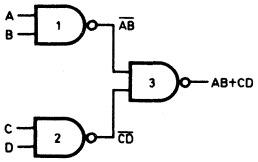


fig. 1

should be drawn as

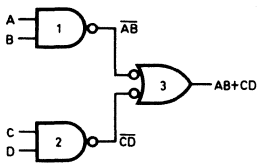


fig. 2

A further advantage of drawing the symbol of gate 3 as in fig. 2 is that it is more apparent that it behaves as an OR function than when drawn as in fig. 1 (cf. table I).

When state indicators are not used no more than four input lines should be drawn at the input side of the symbol (see fig. 3).

When state indicators are used no more than three input lines should be drawn at the input side (see fig. 4).
Following these rules will help to avoid unnecessary crowding of lines in the drawing.
When more input lines are needed the input side of the symbol can be extended in any of the ways indicated in fig. 5.

fig. 3

fig. 4

Equidistant lines

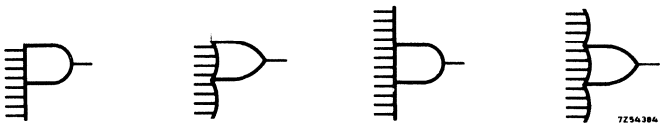


fig. 5

EXTENDED INPUTS

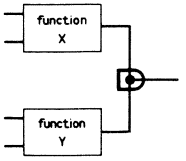
If the number of inputs to an expandable gate is extended by means of an expander circuit, the output line(s) of the expander is (are) connected to the specific expansion input(s) of the gate as drawn below.
The expander symbol shall be drawn to the same dimensions as the gate symbol; however, two filled arrows shall be drawn on each connection line, one arrow close to the expander symbol and another close to the gate symbol.

f = gate
E = expander

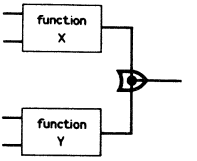
A signal line provided with arrows need not imply the usual logic levels. Generally it should not be connected to "normal" inputs or outputs of gates.

C. **OUTPUT COMBINATIONS** (6.3)

Where functions have the capability of being combined according to the AND (or OR) function, simply by having the outputs connected, that capability shall be shown by enveloping the branched connection with a smaller sized AND or OR symbol .



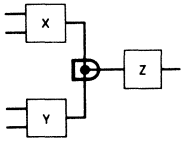
Dot "AND"



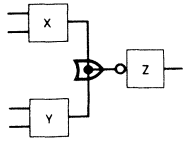
Dot "OR"

Note: These connections of outputs are often described in the literature as "WIRED-OR".

EXAMPLES



The function Z is activated on its input by a HIGH level (because a state indicator is not applied there) if and only if both outputs of functions X and Y are HIGH.
The branched connection shall therefore be enveloped by a small-sized AND symbol.

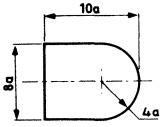


The function Z is activated on its input by a LOW level (because a state indicator is applied there) if and only if one or both outputs of the functions X and Y are LOW.
The branched connection shall therefore be enveloped by a small-sized OR symbol.
It should be noted that it would seem necessary to use state indicators on all terminals of the Dot "OR" symbol for correct interpretation of the circuit. However it is not usual to use state indicators on Dot symbols.

APPENDIX

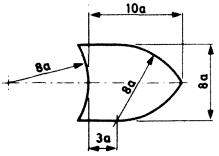
DRAWING DIMENSIONS

Ratio of dimensions of symbols may be derived from the drawings shown.

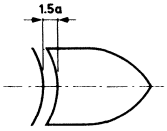


AND

Symbols enveloping a branched connection shall have half the dimensions of the fundamental symbols.



OR

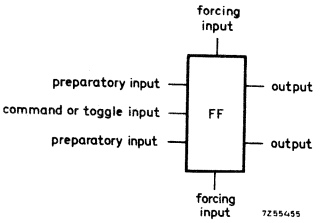


EXCLUSIVE-OR

STATE INDICATOR

FLIP-FLOP SYMBOLS

1. GENERAL SYMBOL



2. DEFINITIONS

Active or "1" state of an input signal.

That state (either a level or a transition from one level to the other) which causes, directly or indirectly, a change of the output state. Conversely, the inactive or "0" state of an input signal is that state which does not cause an output change.

Output state.

There may be one output terminal (Q) or two (Q_1 and Q_2). If there are two, the "output state" refers to the states of the signals at Q_1 and Q_2; since these are normally complementary, the state at Q_1 is usually considered to represent the output state.

Preparatory input terminal (e.g. J, K, D)

An input terminal to which application of an active signal does not directly cause a change of the output state but prepares the circuit for such a change.

Command input terminal (T)

An input terminal to which application of an active signal causes the output to assume the state corresponding to the preparatory inputs. It is also known as the "clock input terminal".

Toggle input terminal (T)

An input terminal at which an active transition from one level to the other directly causes a change of the output state.

Forcing input terminal (S_1 = "direct set", S_2 = "direct reset")

An input terminal at which application of an active signal directly causes the output to assume a specific state, irrespective of the states of other input terminals.

3. LOCATION OF TERMINALS AND USE OF POLARITY STATE INDICATOR, SHOWN BY EXAMPLES

Legend:

H = HIGH level

L = LOW level

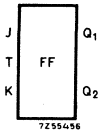
L→H = transition from LOW level to HIGH level

H→L = transition from HIGH level to LOW level

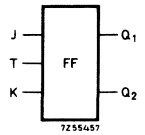
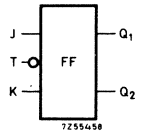
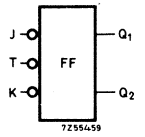
X = state (level or transition) has no influence

? = indeterminate, unless exact timing of relevant input signals (e.g. S_1 and S_2) is known.

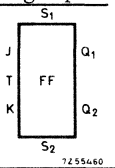
3.1. JK flip-flop without forcing inputs



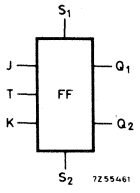
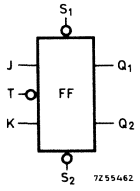
An active ("1") signal at J, together with an inactive ("0") signal at K and an active signal transition at T, causes the "1" state at Q_1 and the "0" state at Q_2.

Symbol	Function table			
	J	K	T	Q_1 Q_2
	H	L	L→H	H L
	L	H	L→H	L H
	H	H	L→H	reversed
	L	L	L→H	no change
	X	X	H→L	no change
	H	L	H→L	H L
	L	H	H→L	L H
	H	H	H→L	reversed
	L	L	H→L	no change
	X	X	L→H	no change
	L	H	H→L	H L
	H	L	H→L	L H
	L	L	H→L	reversed
	H	H	H→L	no change
	X	X	L→H	no change

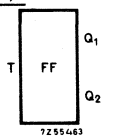
3.2. JK flip-flop with forcing inputs



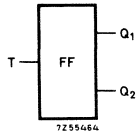
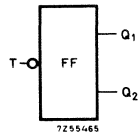
Irrespective of the states at J, K and T: an active ("1") signal at S_1, together with an inactive ("0") signal at S_2, causes Q_1 to assume the "1" and Q_2 the "0" state

Symbol	Function table						
	J	K	T	S_1	S_2	Q_1	Q_2
	X	X	X	H	L	H	L
	X	X	X	L	H	L	H
	X	X	X	H	H	?	?
	H	L	L→H	L	L	H	L
	L	H	L→H	L	L	L	H
	H	H	L→H	L	L	reversed	
	L	L	L→H	L	L	no change	
	X	X	H→L	L	L	no change	
	X	X	X	L	H	H	L
	X	X	X	H	L	L	H
	X	X	X	L	L	?	?
	H	L	H→L	H	H	H	L
	L	H	H→L	H	H	L	H
	H	H	H→L	H	H	reversed	
	L	L	H→L	H	H	no change	
	X	X	L→H	H	H	no change	

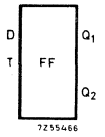
3.3. T flip-flop ("Toggle")



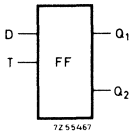
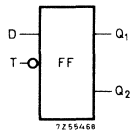
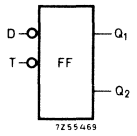
An active ("1") signal transition at T causes the complementary states at Q_1 and Q_2 to reverse.

Symbol	Function table	
	T	Q_1 Q_2
	L→H H→L	reversed no change
	H→L L→H	reversed no change

3.4. Edge-triggered D flip-flop

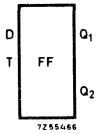


An active ("1") signal transition at T causes Q_1 to assume the same state as D. I.e., if D is in the "1" state during the active transition at T, Q_1 also assumes the "1" state: if D is "0", Q_1 also becomes "0". The output state will remain unchanged until the next active transition at T occurs.

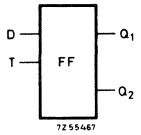
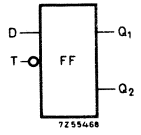
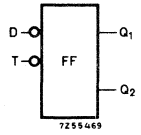
Symbol	Function table			
	D	T		Q_1 Q_2
		level	transition	
	H		L→H	H L
	L		L→H	L H
	X	X		no change
	X		H→L	no change
	H		H→L	H L
	L		H→L	L H
	X	X		no change
	X		L→H	no change
	L		H→L	H L
	H		H→L	L H
	X	X		no change
	X		L→H	no change

3.5. Level-operated ("gated") D flip-flop, or "Bistable latch".

(Graphical symbol equal to 3.4.)

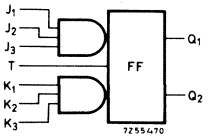


As long as the signal at T is at its active ("1") level, the signal at Q_1 follows the signal at D. When the signal at T changes to its inactive ("0") level, the signal at Q_1 latches (Subsequent changes in D cause no change in Q_1). Q_1 unlatches when the signal at T returns to its active level.

Symbol	Function table			
	D	T		Q_1 Q_2
		level	subsequent transition	
	H	H		H L
	H	H	H→L	H L
	L	H		L H
	L	H	H→L	L H
	X	L		no change
	H	L		H L
	H	L	L→H	H L
	L	L		L H
	L	L	L→H	L H
	X	H		no change
	L	L		H L
	L	L	L→H	H L
	H	L		L H
	H	L	L→H	L H
	X	H		no change

4. MULTIPLE INPUTS

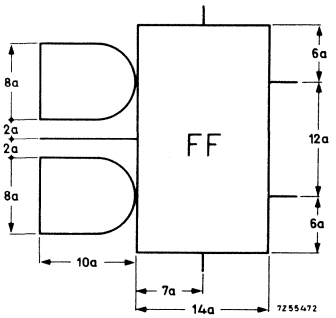
Where inputs are functionally combined by an input gate, the connecting line between the gate symbol and the flip-flop symbol may conveniently be omitted, as shown in the drawing.



5. TIME DELAY CIRCUIT

The following time delay symbol (MIL-STD-806 B, 5.15) is used in some logic flip-flop block diagrams:

6. DRAWING DIMENSIONS (to MIL-STD-806 B)



The ratio of dimensions is given in the drawing above.

For dimensions of gates and state-indicators see "Appendix", page 8.

RATING SYSTEMS

ACCORDING TO I.E.C. PUBLICATION 134

1. DEFINITIONS OF TERMS USED

1.1 Electronic device. An electronic tube or valve, transistor or other semiconductor device.
Note: This definition excludes inductors, capacitors, resistors and similar components.

1.2 Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

1.3 Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

1.4 Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.
Note: Limiting conditions may be either maxima or minima.

1.5 Rating system. The set of principles upon which ratings are established and which determine their interpretation.
Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

2. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

p.t.o.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

3. DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

4. DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

NOTE

It is common use to apply the Absolute Maximum System in semiconductor published data.

LETTER SYMBOLS
FOR DIGITAL INTEGRATED CIRCUITS

(Additional symbols for MOS circuits on page 4)

1. General

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device or the function of the pertinent signal.
In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

2. Terminal designations

D = D input of D type latch flip-flops
E = expander input (if necessary, this letter may be followed by an index, e.g. E_1 or E_2 or by one of the input letters, such as EG = gate expander input)
G = gate input
J, K = J, K input of JK flip-flops
N = negative supply
P = positive supply
Q = output
S = direct SET input
T = trigger (or toggle) input
Ø = common supply return and voltage reference

3. Subscript sequence for voltages and currents

First subscript : terminal designation letter.
Second subscript: H (for HIGH) or L (for LOW), if applicable.
Third subscript : min or max, if applicable.
Examples: V_P, I_{QL}, V_{QHmin}, I_{PH} (in the latter case H denotes that the output level is HIGH).

4. Polarity of current and voltage

A current is defined as positive when its conventional direction of flow is into the device.
Unless otherwise specified, a voltage is measured with respect to the reference terminal (Ø). Its polarity is defined as positive when the potential is higher than that of the reference terminal.

5. Time designations

If required for reasons of unambiguity, the related terminals may be included in the designations given below (e.g. t_{fQ1}).

t_f = fall time (transition from HIGH to LOW, see Fig. 1)

t_H = signal HIGH duration (Fig. 1)

t_L = signal LOW duration (Fig. 1)

t_{pd} = average propagation delay time, defined as $\frac{t_{pdr} + t_{pdf}}{2}$

t_{pdf} = fall propagation delay time (output voltage falling, see Fig. 2)

t_{pdr} = rise propagation delay time (output voltage rising, see Fig. 2)

t_r = rise time (transition from LOW to HIGH, see Fig. 1)

t_{sc} = duration of short circuit (from relevant terminal to common return terminal)

V_{pd} = reference voltage level for propagation delay measurement

Fig. 1.

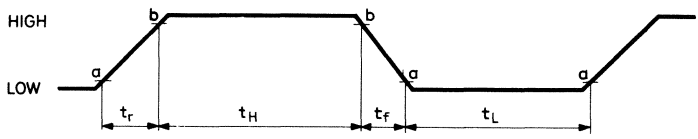
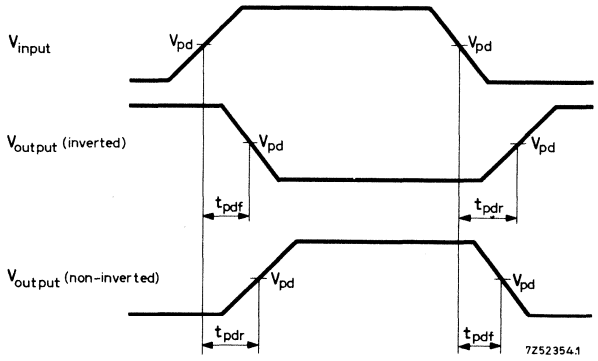


Fig. 2.



6. Other designations

i.c. = internally connected
Terminals with this indication should be left open. Otherwise correct working cannot be ensured; the device may even be damaged

n.c. = not connected internally
It is recommended not to use these terminals for any connection

I_P = supply current
The logic state of the device indicated by H or L is normally referred to the output level, unless otherwise specified

I_{Pmax} = supply current
Maximum d.c. value under defined conditions

M = d.c. noise margin

M_L = d.c. noise margin, signal level LOW
(defined as: $M_L = V_{GLmax} - V_{QLmax}$ under defined loading, temperature and supply voltage conditions)

M_H = d.c. noise margin, signal level HIGH
(calculated from: $M_H = V_{QHmin} - V_{GHmin}$ under defined loading, temperature and supply voltage conditions)

N_a = available d.c. fan-out (defined as: $N_a = \frac{I_{QLmax}}{-I_{GLmax}}$ under defined temperature and supply voltage conditions)

P_H; P_L = power consumption, defined as the product of the supply current(s) and of the corresponding supply voltage(s). The logical state of the device, indicated by a letter index H or L, is normally referred to the output level, unless otherwise specified

P_{av} = average power consumption at 50% duty cycle, unless otherwise specified. It is defined as: $P_{av} = V_P \cdot \frac{I_{PH} + I_{PL}}{2}$

P_{tot} = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account. The logical state of the device indicated by a letter index H or L is normally referred to the output level, unless otherwise specified

T_{amb} = operating ambient temperature, i.e. the temperature of the free air in which the normally operating device is placed without external heat conduction, unless otherwise specified

T_{stg} = storage temperature, i.e. the temperature of the ambient medium in which the non-operating device is stored

V_{GLmax} = input voltage LOW at terminal G. With the specified level applied to the input of an inverting gate the **output level will not be lower than** the specified value V_{QHmin} at given I_{QH}.

V_{GHmin} = input voltage HIGH at terminal G. With the specified level applied to the input of an inverting gate the **output level will not exceed the** specified value V_{QLmax} at given I_{QL}.

ΔV_Q = change of output voltage caused by a specified change of output current

ADDITIONAL SYMBOLS FOR MOS CIRCUITS

2a. Terminal designations

I = shift register input
A = address input or decode matrix input
ϕ = clock input
WC = write control input
D = data input
CD = chip disable input
Q = output
C = chip inhibit input
P_o = common supply return and voltage reference
P_1, P_2, etc. = supply input

3a. Subscript sequence for voltages
First (with or without second) subscript: terminal designation
Second or third subscript: H (HIGH) or L (LOW) if applicable

5a. Time designations

Details are described in the data sheets

6a. Other designations

M_L = d.c. noise margin LOW ($M_L = V_{\text{input L max}} - V_{\text{output L max}}$)
M_H = d.c. noise margin HIGH($M_H = V_{\text{output H min}} - V_{\text{input H min}}$)
R_{QH} = output resistance HIGH
R_{QL} = output resistance LOW
P_{av} = average power consumption

LETTER SYMBOLS FOR LINEAR INTEGRATED CIRCUITS

General

The voltages and currents are normally related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a number. In appropriate cases voltages, currents etc. pertinent to one or more of the circuit elements (transistors, diodes) are given in which case symbols are based on the recommendations as published in I.E.C. Publication 148.

Quantity symbols

1. Instantaneous values of current, voltage and power, which vary with time are represented by the appropriate lower case letter.

   Examples: i, v, p

2. Maximum (peak), average, d.c. and root-mean-square values are represented by the appropriate upper case letter.

   Examples: I, V, P

Polarity of current and voltage

A current is defined to be positive when its conventional direction of flow is into the device.
A voltage is measured with respect to the reference terminal, which is indicated by the subscripts. Its polarity is defined to be positive when the potential is higher than that of the reference terminal.

Subscripts

For currents the number behind the quantity symbol indicates the terminal carrying the current.

Examples: I_2, i_{14}

For voltages normally two number subscripts are used, connected by a hyphen. The first number indicates the terminal at which the voltage is measured and the second subscript the reference terminal.
Where there is no possibility of confusion the second subscript may be omitted.

Examples: V_{2-12}, v_{14-2}, V_5, v_8

To distinguish between maximum (peak), average, d.c. and root-mean-square values the following subscripts are added:

For maximum (peak) values : M or m
For average values : AV or av
For root-mean-square values: (RMS) or (rms)
For d.c. values : no additional subscripts

The upper case subscripts indicate total values.
The lower case subscripts indicate values of varying components:

Examples: I_2, I_{2AV}, $I_{2(rms)}$, $I_{2(RMS)}$

If in appropriate cases quantity symbols are pertinent to single elements of a circuit (transistors or diodes), the normal subscripts for semiconductor devices can be used.

Examples: V_{CBO}, V_{be}, V_{CES}, I_C
V_{DSS}, V_{GS}, I_D

List of subscripts:

E, e	=	Emitter terminal
B, b	=	Base terminal for bipolar transistors, Substrate for MOS devices
C, c	=	Collector terminal
D, d	=	Drain terminal
G, g	=	Gate terminal
S, s	=	Source terminal for MOS devices Substrate for bipolar transistor circuits
(BR)	=	Break-down
M, m	=	Maximum (peak) value
AV, av	=	Average value
(RMS), (rms)	=	R.M.S. value

Electrical Parameter Symbols

1. The values of four pole matrix parameters or other resistances, impedances, admittances, etc., inherent in the device, are represented by the lower case symbol with appropriate subscript.

Examples: h_i, z_f, y_o, k_r

Subscripts for Parameter Symbols

1. The static values of parameters are indicated by upper case subscripts.

Examples: h_{FE}, h_I

2. The small signal values of parameters are indicated by lower case subscripts.

Examples: h_i, z_o

3. The first subscript, in matrix notation identifies the element of the four pole matrix.

   i (for 11) = input
   o (for 22) = output
   f (for 21) = forward transfer
   r (for 12) = reverse transfer

   Examples: $V_1 = h_i I_1 + h_r V_2$

   $I_2 = h_f I_1 + h_o V_2$

The voltage and current symbols in matrix notation are indicated by a single digit subscript.
The subscript 1 = input; the subscript 2 = output.
The voltages and currents in these equations may be complex quantities.

4. A second subscript is used only for separate circuit elements (e.g. transistors) to identify the circuit configuration:

   e = common emitter
   b = common base
   c = common collector

5. If it is necessary to distinguish between real and imaginary parts of the four pole parameters, the following notation may be used:

   R_e (h_i) etc. ... for the real part
   I_m (h_i) etc. ... for the imaginary part

LIST OF LETTER SYMBOLS IN ALPHABETICAL ORDER

Letter symbol	Definition
B	Bandwidth
b_i, b_o	Input, respectively output susceptance
C_i, C_o	Input, respectively output capacitance
CMMR	Common-mode rejection ratio
d	Distortion
F	Noise figure
f	Frequency
f_c	Cut-off frequency
f_o	Centre frequency, intermediate frequency
fm	Modulation frequency
f_T	Transition frequency
g_i, g_o	Input, respectively output conductance
G_p	Power gain
G_{tr}	Transducer gain
G_v	Voltage gain
h_F, h_{FB}, h_{FC}, h_{FE}	DC current gain (output voltage held constant)
h_f, h_{fb}, h_{fc}, h_{fe}	Small signal current gain (output short-circuited to a.c.)
I_3, I_B, I_C, I_E, I_D, I_Q, I_S	Total d.c. current
i_3, i_B, i_C, i_E, i_D, i_G, i_S	Instantaneous total value of the current
I_{3AV}, I_{BAV}, I_{CAV}, I_{EAV}	Total average current
I_{3M}, I_{BM}, I_{CM}, I_{EM}	Maximum (peak) value of the total current
I_{3m}, I_{bm}, I_{cm}, I_{em}	Maximum (peak) value of the varying component of the current
I_{CBO}	Collector cut-off current (open emitter)
I_{CS}	Collector-substrate leakage current
I_{DSS}	Drain cut-off current (source short-circuited to gate)

Letter symbol	Definition
I_{EBO}	Emitter cut-off current
I_I, I_i	Input current of a specified circuit
I_{io}	Input offset current
I_O, I_o	Output current of a specified circuit
I_{OM}	Peak value of output current
$I_{o(p-p)}$	Peak to peak value of output current
I_{tot}	Total supply current
K_f	Small signal voltage gain
K_o	Output impedance (see K parameters)
K_r	Reverse current transfer ratio
M	Modulation depth
P_i, P_o	Input, respectively output power of a specified circuit
P_{tot}	Total power dissipation in the device
R_i, R_o	Input, respectively output resistance of a specified circuit
R_L	Load resistance
R_S	Source resistance
R_{th}	Thermal resistance
SVRR	Supply voltage rejection ratio
T_{amb}	Ambient temperature
T_{case}	Case temperature
T_{stg}	Storage temperature
V_3, V_{3-4}, V_{BE}, V_{CB}	Total value of the voltage (d.c.)
v_3, v_{3-4}, v_{BE}, v_{CB}	Instantaneous value of the total voltage
V_{BEsat}, V_{CEsat}	Saturation voltage at specified bottoming conditions
$V_{(BR)CBO}$, $V_{(BR)CEO}$, $V_{(BR)EBO}$	Breakdown voltage between the terminal of the first subscript and the reference terminal (second subscript) when the third terminal is open circuited
$V_{(BR)CS}$	Collector to substrate breakdown voltage
V_{CBO}, V_{CEO}, V_{EBO}, V_{CS}, V_{1-3}	Voltage of the terminal indicated with respect to the reference terminal (second subscript)

Letter symbol	Definition
V_i, V_o	Input, respectively output voltage of a specified circuit
V_{io}	Input offset voltage
$V_{i\ lim}$	Input voltage at which limiting starts
V_N	Negative supply voltage
V_P	Positive supply voltage
V_n	Noise voltage
y_i, y_f, y_o, y_r	Input, transfer, output and feedback admittance
Z_i, Z_o	Input, respectively output impedance
η	Efficiency
φ_i, φ_f, φ_o, φ_r	Phase angle of input, transfer, output and feedback admittance

D T L FC family

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

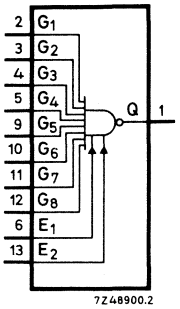
NAND GATES

	non-R_c	R_c
Single 8-input NAND gate	FCH101	FCH111
Dual 4-input NAND gate	FCH121	FCH131
Triple 3-3-2-input NAND gate	FCH141	FCH161
Triple 3-input NAND gate	FCH151	FCH171
Quadruple 2-input NAND gate	FCH181	FCH191
Sextuple inverter	FCH201	FCH211

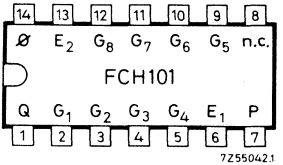
QUICK REFERENCE DATA				
Supply voltage		V_P	6.0 ± 5%	V
Operating ambient temperature range		T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C		t_{pd}	typ. 30	ns
Available d.c. fan out T_{amb} = 0 to +75 °C		N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C		M_L	typ. 1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	non-R_c gate	P_{av}	typ. 7	mW
	R_c gate	P_{av}	typ. 11	mW

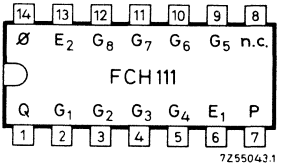
The FC family includes twelve NAND packages offering a wide selection of circuit configurations. It includes gate types with as well as without a collector resistor, ensuring optimum equipment design.
The fan-in of the circuits can easely be expanded by means of a diode array.
The outputs of these gates may be interconnected to perform the AND-OR-NOT function.

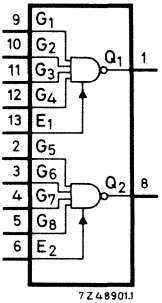
PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)



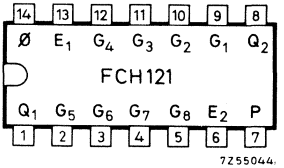
FCH101 (non-R_C)
FCH111 (R_C)

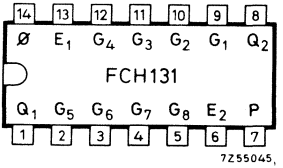


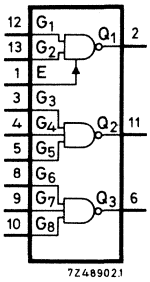




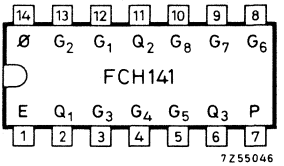
FCH121 (non-R_C)
FCH131 (R_C)

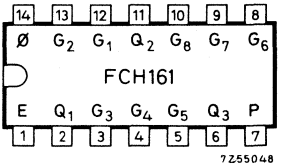


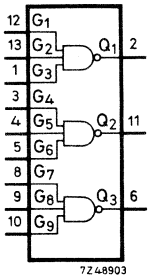




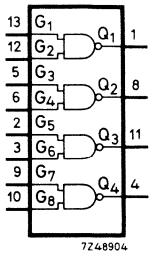
FCH141 (non-R_C)
FCH161 (R_C)



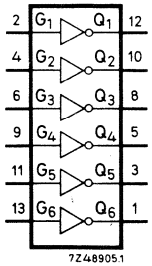




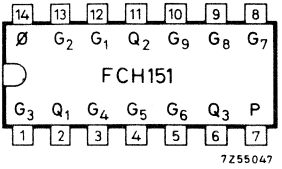
FCH151 (non-R_C)
FCH171 (R_C)

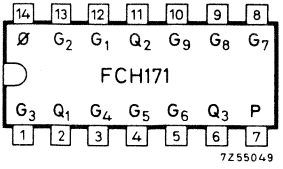


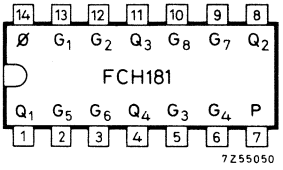
FCH181 (non-R_C)
FCH191 (R_C)

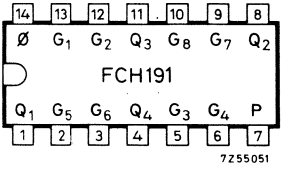


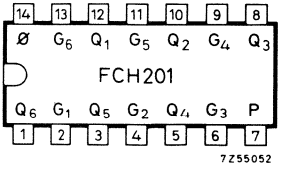
FCH201 (non-R_C)
FCH211 (R_C)

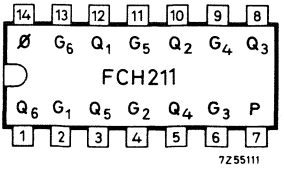






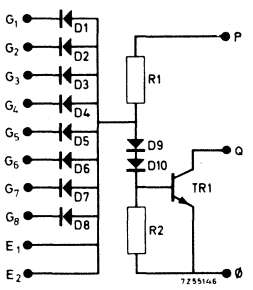




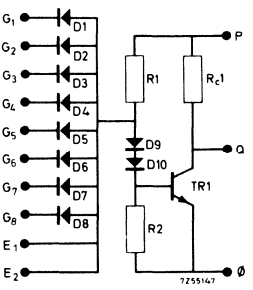


CIRCUIT DIAGRAMS

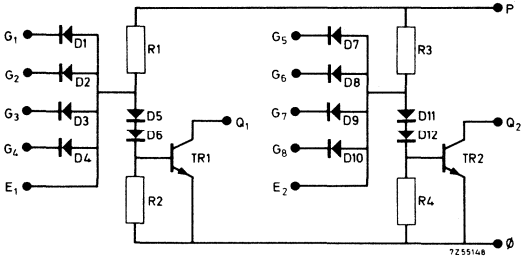
FCH101



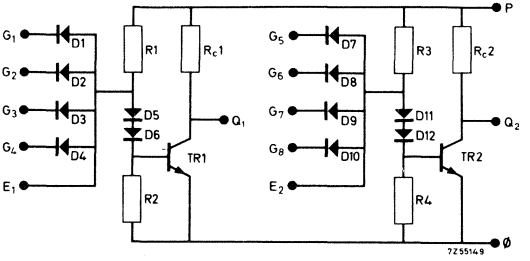
FCH111



FCH121

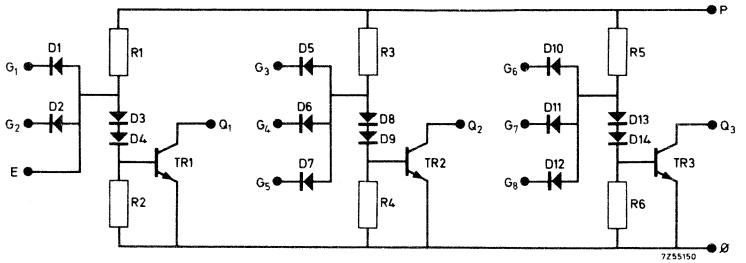


FCH131

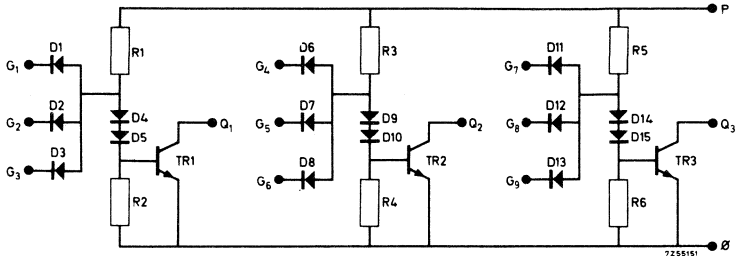


CIRCUIT DIAGRAMS (continued)

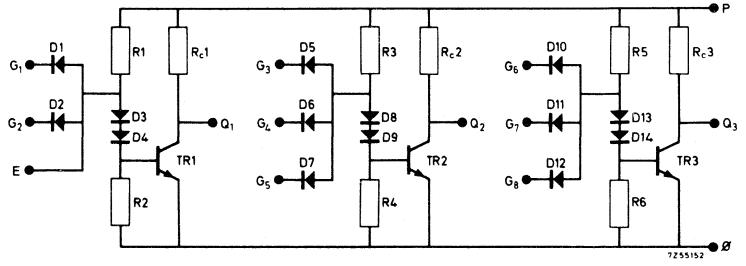
FCH141



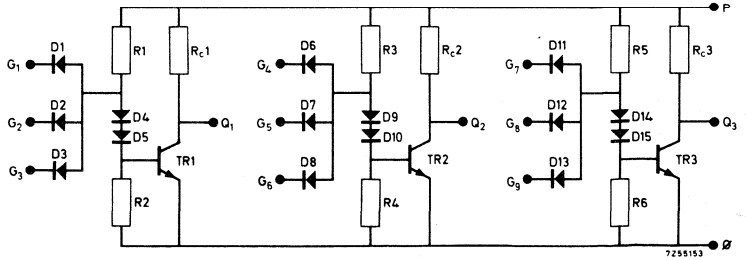
FCH151



FCH161

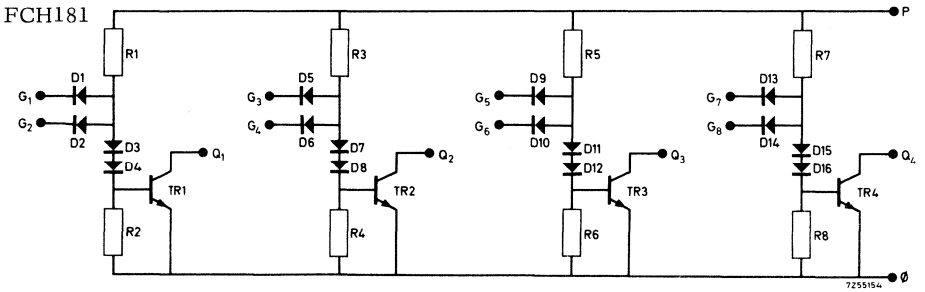


FCH171

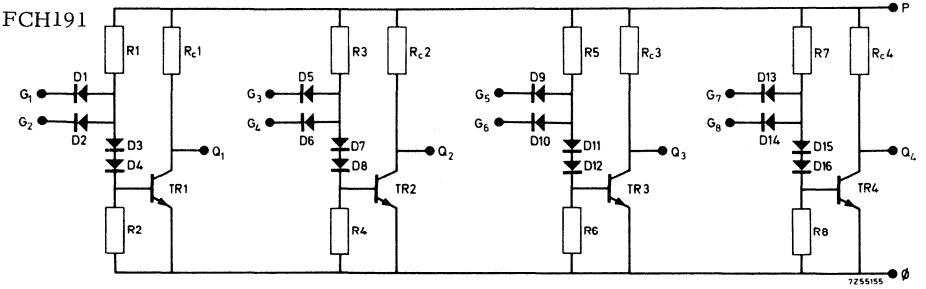


CIRCUIT DIAGRAMS (continued)

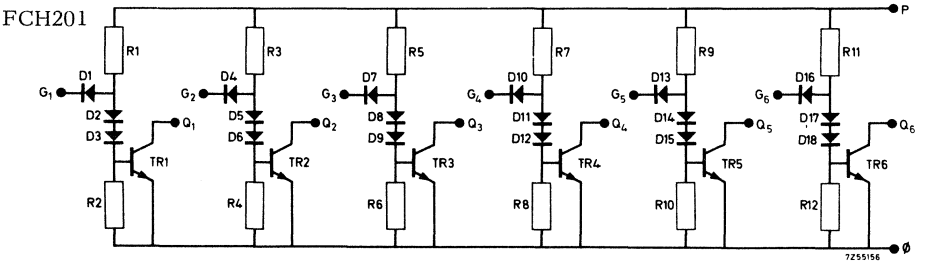
FCH181



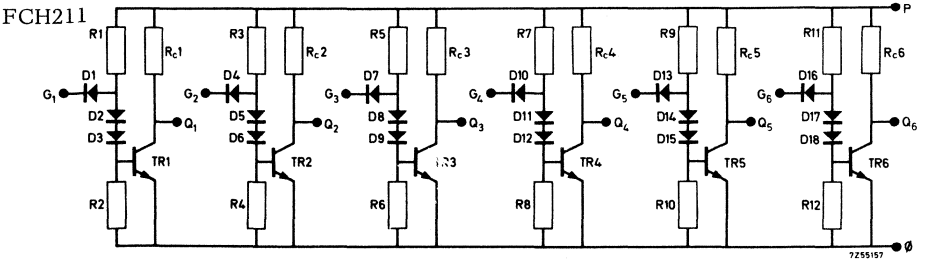
FCH191



FCH201



FCH211



LOGIC FUNCTION

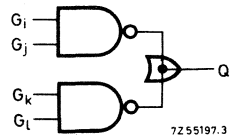
1. Individual gate operation

$Q = \overline{G_i \cdot G_j}$ for positive logic

Function table

G_i	G_j	Q
L	X	H
X	L	H
H	H	L

2. Commoned gate operation



Function table

G_i	G_j	G_k	G_l	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

$Q = (\overline{G_i \cdot G_j}) \cdot (\overline{G_k \cdot G_l}) = \overline{(G_i \cdot G_j) + (G_k \cdot G_l)}$ for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

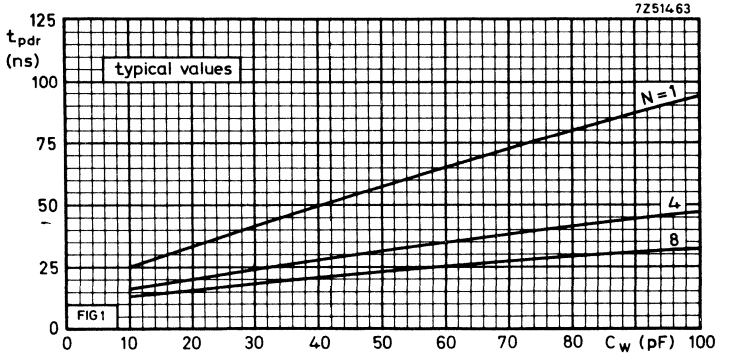
RATINGS (Limiting values) [1]

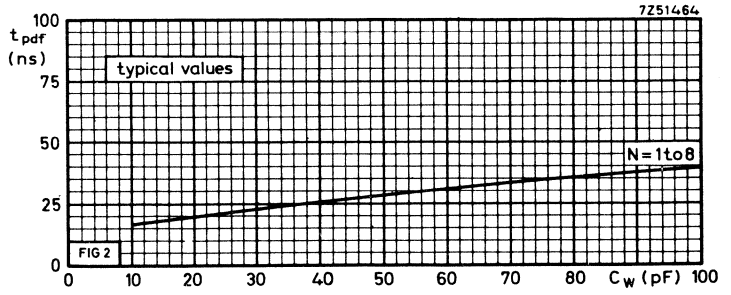
Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages				
with respect to supply	$V_P - V_E$	max.	8.0	V
with respect to other inputs	$V_G - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

[1] Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2] For negative output voltage.
[3] At this limit, input voltage type.: −1.5 V.

SYSTEM DESIGN DATA (both non-R_c and R_c)

Uniform system temperature		T_{amb}	0 to +75	°C
Uniform system supply voltage		V_P	5.7 to 6.3	V
Available d.c. fan out		N_a	≥ 8	
D.C. noise margin		M_L	min. 0.4	V
		M_H	min. 1.8	V
Average propagation delay time		t_{pd}	max. 75	ns
Equivalent input capacitance		C_G	typ. 4	pF
Equivalent output capacitance		C_Q	typ. 10	pF
Supply current per gate (duty cycle 50%)	non-R_c	I_{Pav}	typ. 1.20	mA
	R_c	I_{Pav}	typ. 1.75	mA
Power dissipation at T_{amb} = 75 °C (each gate)	non-R_c	P_{tot}	max. 17.5	mW
	R_c	P_{tot}	max. 22	mW





CHARACTERISTICS of non-R_c gates

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	16.0 18.0	15.1 17.0	14.2 16.0	mA mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Output current HIGH	I_{QHmax}	70	70	70	μA	5.7 and 6.3	V_Q = 5.3 V
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Supply current [1]	I_{Pmax}	2.0	1.9	1.8	mA	6.3	G inputs LOW
DYNAMIC DATA							
Rise propagation delay time	t_{pdrmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdrmax}	-	70	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF ←
Fall propagation delay time	t_{pdfmax}	-	65	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdfmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF ←

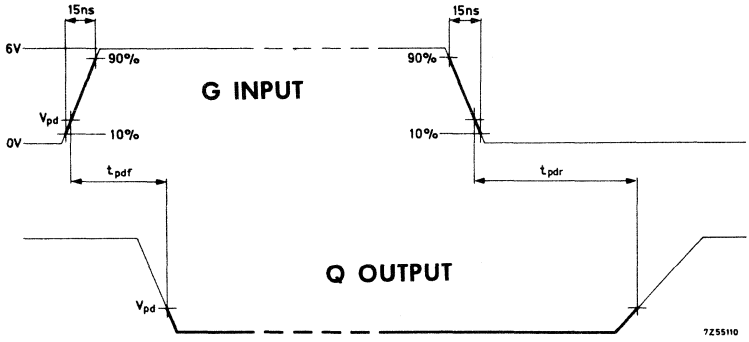
[1] per gate

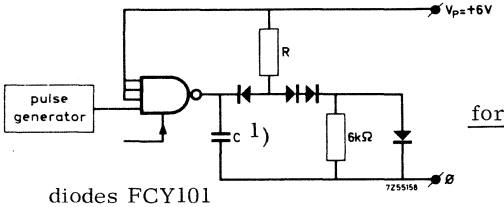
CHARACTERISTICS of R_C-gates

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
		16.0	15.2	14.4	mA	6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	I_Q = 0
		4.1	4.1	3.9	V	5.7	I_Q = −200 μA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75	1.65	1.55	mA	5.7	V_G = 0.4 V; other inputs floating
		2.0	1.9	1.8	mA	6.3	
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Output current LOW (AND-OR-NOT function)	$-I_{QLLmax}$	2.2	2.1	2.0	mA	6.3	$V_G = V_{QLmax}$ Output forced LOW externally to V_Q = 0.4 V
Supply current	I_{Pmax}	4.2	3.8	3.6	mA	6.3	G inputs HIGH
DYNAMIC DATA							
Rise propagation delay time	t_{pdrmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdrmax}	-	70	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF ←
Fall propagation delay time	t_{pdfmax}	-	65	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdfmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF ←

CHARACTERISTICS (continued)

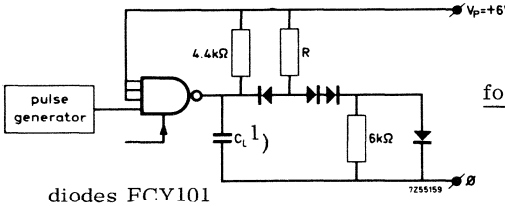
DYNAMIC DATA





diodes FCY101

for R_C gates



diodes FCY101

for non-R_C gates

Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf}.

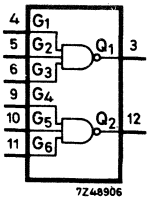
Equivalent load for N = 1 and C_L = 40 pF when R = 4 kΩ

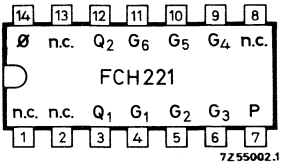
N = 6 and C_L = 60 pF when R = 670 Ω

1) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 3-INPUT LINE DRIVER NAND GATE



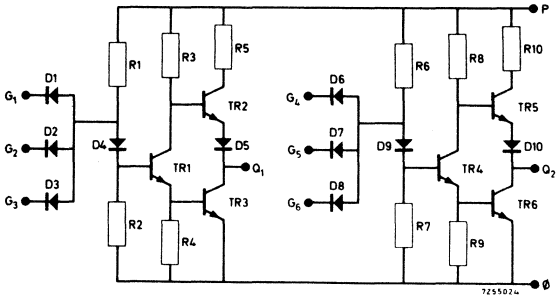


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 15, C_w = 250 pF, T_{amb} = 25 °C	t_{pd}	typ. 35	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	≥ 14	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 11	mW

The FCH221 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

G_1 G_4	G_2 G_5	G_3 G_6	Q_1 Q_2
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

$$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3}$$
$$Q_2 = \overline{G_4 \cdot G_5 \cdot G_6}$$
for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1])

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2])	$-I_Q$	max.	20	mA
Input current [3])	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C
Output short-circuit duration; duty cycle 10% (either output, or both)	t_{Qsc}	max.	60	ms

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2]) For negative output voltage in LOW state
[3]) At this limit input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75	°C
Uniform system supply voltage	V_P	5.7 to 6.3	V
Available d.c. fan out	N_a	⩾ 14	
D.C. noise margin	M_L	min. 0.4	V
	M_H	min. 1.1	V
Average propagation delay time	t_{pd}	max. 113	ns
Equivalent input capacitance	C_G	typ. 7	pF
Supply current (duty cycle 50 %) [1]	I_{Pav}	typ. 3.6	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max. 65	mW

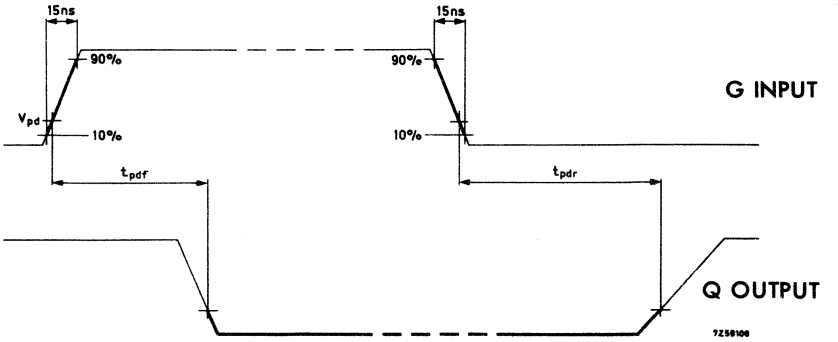
[1]) Both gates together; outputs not short-circuited.

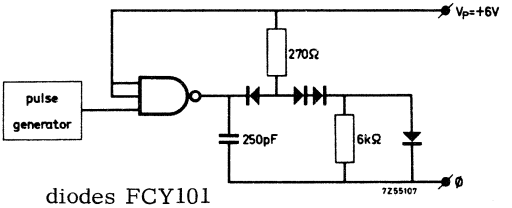
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	25 28	27 27	26 26	mA mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	3.4 2.2	3.6 2.5	3.9 2.9	V V	5.7 5.7	I_Q = −30 μA I_Q = −5 mA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	$V_G = V_{QHmin}$ other inputs 0 V
Output short circuit current	$-I_{Qsc}$	16.5	19.5	18.0	mA	5.7	$V_G = V_{GLmax}$ V_Q = 0 V
Supply current (both gates together)	I_{Pmax}	–	7.5	–	mA	6.3	G inputs HIGH
DYNAMIC DATA							
Rise propagation delay time	$t_{pdr\,max}$	130	105	130	ns	6.0	V_{pd} = 1.5 V N = 15; C_L = 250 pF
Fall propagation delay time	$t_{pdf\,max}$	95	80	95	ns	6.0	V_{pd} = 1.5 V N = 15; C_L = 250 pF

CHARACTERISTICS (continued)

DYNAMIC DATA





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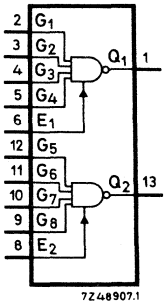
Equivalent load for N = 15 and C_L [1]) = 250 pF

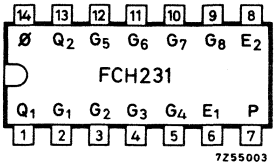
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 4-INPUT LINE DRIVER NAND GATE



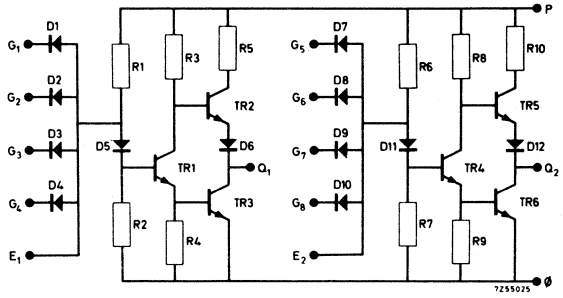


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 20, C_W = 250 pF, T_{amb} = 25 °C	t_{pd}	typ. 35	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 20	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 11	mW

The FCH231 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving very high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A).(See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

G_1 G_5	G_2 G_6	G_3 G_7	G_4 G_8	Q_1 Q_2
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

$$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot E_1}^{\,*}$$
$$Q_2 = \overline{G_5 \cdot G_6 \cdot G_7 \cdot G_8 \cdot E_2}^{\,*}$$

for positive logic

* When provided with diode

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages				
with respect to supply	$V_P - V_E$	max.	8.0	V
with respect to other inputs	$V_G - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C
Output short-circuit duration; duty cycly 10% (either output, or both)	t_{Qsc}	max.	60	ms

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out	N_a	⩾	20	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.2	V
Average propagation delay time	t_{pd}	max.	113	ns
Equivalent input capacitance	C_G	typ.	7	pF
Supply current (duty cycle 50%) [4]	I_{Pav}	typ.	3.6	mA
Power dissipation at T_{amb} = 75 °C [4]	P_{tot}	max.	73	mW

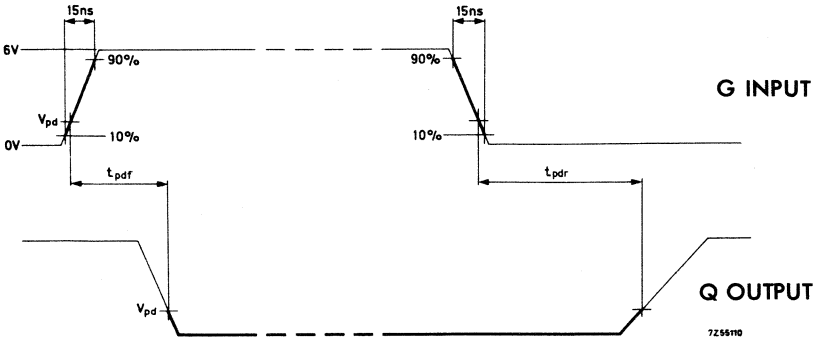
1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage in LOW state.
3) At this limit, input voltage typ. : −1.5V.
4) Both gates together; outputs not short-circuited.

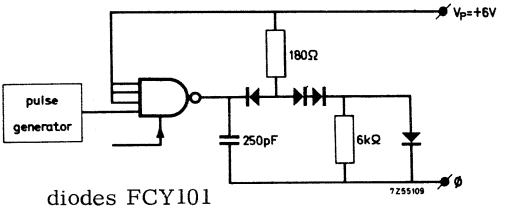
CHARACTERISTICS

		T_{amb} (°C)			Conditions and references	
		0	+25	+75	V_P (V)	
STATIC DATA						
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4 V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	35 40	33 38	31 mA 36 mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1 V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	3.5 2.6	3.7 2.8	4.0 V 2.9 V	5.7 5.7	I_Q = −30 μA I_Q = −5 mA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8 V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 mA 1.8 mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25 μA	5.7	$V_G = V_{QHmin}$ other inputs 0 V
Output short circuit current	$-I_{Qscmin}$	16.5	19.5	18.0 mA	5.7	$V_G = V_{GLmax}$ V_Q = 0 V
Supply current (both gates together)	I_{Pmax}	–	7.5	– mA	6.3	G inputs HIGH
DYNAMIC DATA						
Rise propagation delay time	t_{pdrmax}	80	85	120 ns	6.0	V_{pd} = 1.5 V N = 20; C_L = 250 pF
Fall propagation delay time	t_{pdfmax}	55	50	55 ns	6.0	V_{pd} = 1.5 V N = 20; C_L = 250 pF

CHARACTERISTICS (continued)

DYNAMIC DATA





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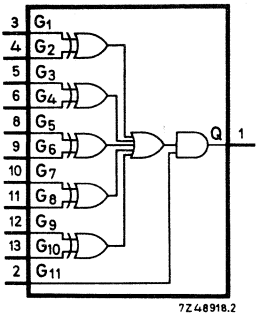
Equivalent load for N = 20 and C_L [1]) = 250 pF

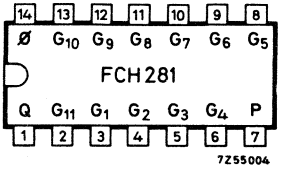
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 5-BIT COMPARATOR



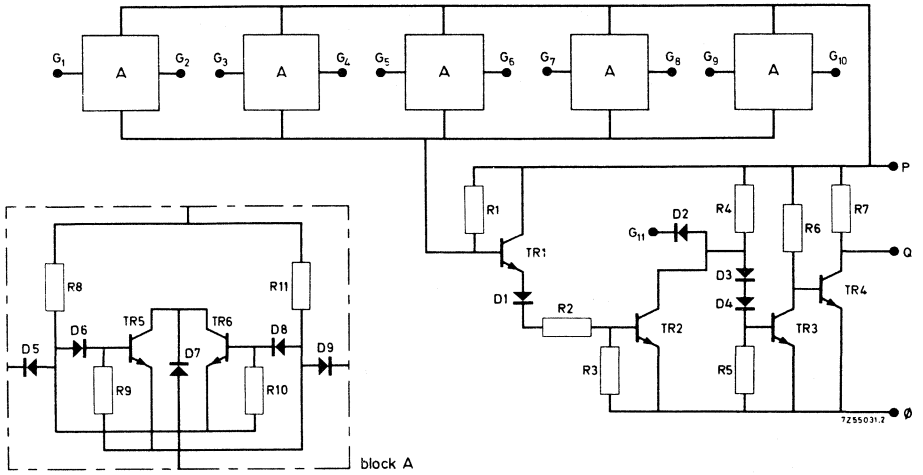


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C	t_{pd}	typ. 150	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 50	mW

The FCH281 comprises five exclusive-OR functions, an OR gate, and an AND gate. If on one or more pairs (G_1-G_2, --- G_9-G_{10}) one input is LOW and the other HIGH then the output will be HIGH provided G_{11} is HIGH. Otherwise the output will be LOW.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

$G_1\,G_2$	$G_3\,G_4$	$G_5\,G_6$	$G_7\,G_8$	$G_9\,G_{10}$	G_{11}	Q
Equal	Equal	Equal	Equal	Equal	H	L
Unequal	X	X	X	X	H	H
X	Unequal	X	X	X	H	H
X	X	Unequal	X	X	H	H
X	X	X	Unequal	X	H	H
X	X	X	X	Unequal	H	H
X	X	X	X	X	L	L

G_1	G_2	
L	L	Equal
L	H	Unequal
H	L	Unequal
H	H	Equal

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC FUNCTION (continued)

$$Q = \Big[\overline{(\overline{G}_1 \cdot \overline{G}_2 + G_1 \cdot G_2)} + \overline{(\overline{G}_3 \cdot \overline{G}_4 + G_3 \cdot G_4)} + \overline{(\overline{G}_5 \cdot \overline{G}_6 + G_5 \cdot G_6)} + \\ + \overline{(\overline{G}_7 \cdot \overline{G}_8 + G_7 \cdot G_8)} + \overline{(\overline{G}_9 \cdot \overline{G}_{10} + G_9 \cdot G_{10})}\Big] \cdot G_{11}.$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20	mA[1])
Input current	$-I_G$	max.	20	mA[2])
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

[1]) For negative output voltage.
[2]) At this limit input voltage typ. : −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out	N_a	⩾	8	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	250	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	10	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	90	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	see note 1
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	see note 1
		16.0	15.2	14.4	mA	6.3	see note 1
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7 and 6.3	I_Q = 0 (see note 1)
	V_{QHmin}	4.7	4.7	4.5	V	5.7	I_Q = −200 μA
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	3.0	2.8	2.5	V	5.7 and 6.3	
Input current LOW	$-I_{G1\ to\ 10\ Lmax}$	1.75	1.65	1.55	mA	5.7	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G1\ to\ 10\ Lmax}$	2.0	1.9	1.8	mA	6.3	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G11\ Lmax}$	1.2	1.1	1.05	mA	5.7	V_{G11} = 0.4 V
	$-I_{G11\ Lmax}$	1.35	1.25	1.20	mA	6.3	V_{G11} = 0.4 V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Supply current	I_{Pmax}	15.3	14.5	13.5	mA	6.3	G inputs LOW

Note 1

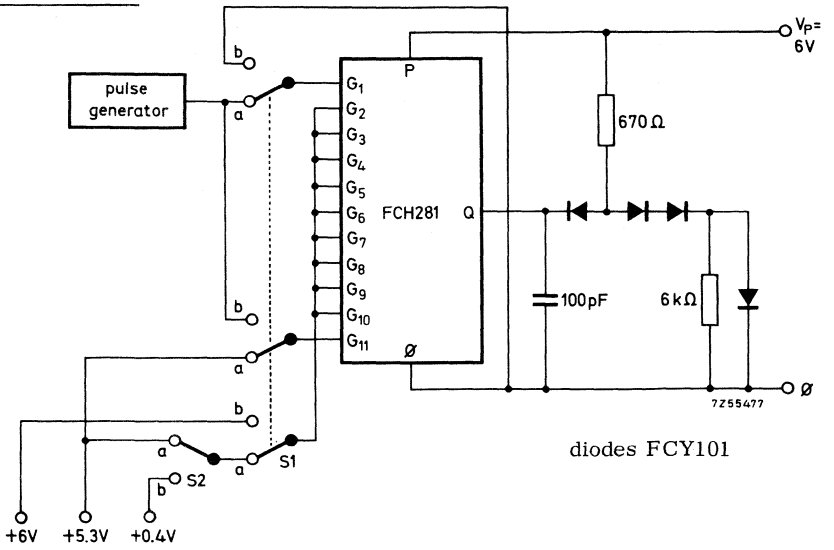
For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

		T_{amb} (°C)			Conditions and references		
		0	+25	+75	V_P (V)		Fig.
DYNAMIC DATA							
Propagation delay times from one G (G_1 to G_{10}) to Q							
Rise propagation delay time	t_{pdrmax}	-	200	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF all other inputs (including G_{11}) at V_G = 5.3 V	1; 2
Fall propagation delay time	t_{pdfmax}	-	200	- ns	6.0		
Rise propagation delay time	t_{pdrmax}	-	250	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF all other inputs (excluding G_{11}) at V_G = 0.4 V $V_{G_{11}}$ = 5.3 V	1; 3
Fall propagation delay time	t_{pdfmax}						
Propagation delay times from G_{11} to Q							
Rise propagation delay time	t_{pdrmax}	-	100	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF V_{G_1} = 0 V all other inputs at V_G = 6.0 V	1; 3
Fall propagation delay time	t_{pdfmax}	-	120	- ns	6.0		

CHARACTERISTICS (continued)

DYNAMIC DATA



diodes FCY101

Fig. 1 Equivalent load for N = 6; C_L [1] = 80 pF

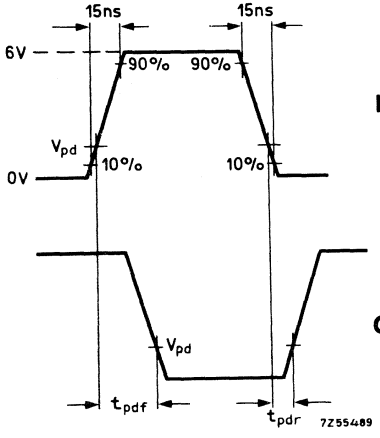


Fig. 2 Switch S1 in position a
Switch S2 in position a

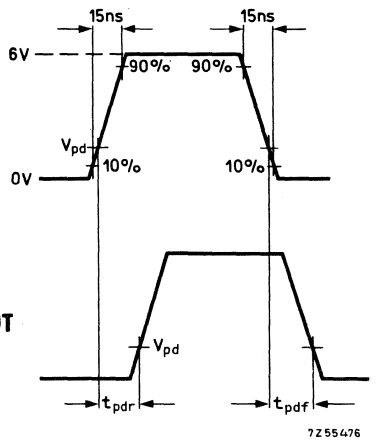


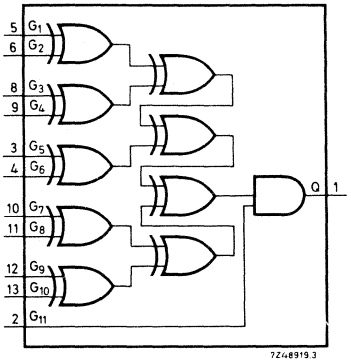
Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b
Switch S2 immaterial

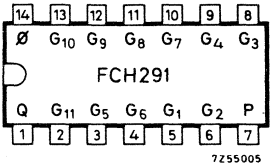
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 10-BIT PARITY CHECKER



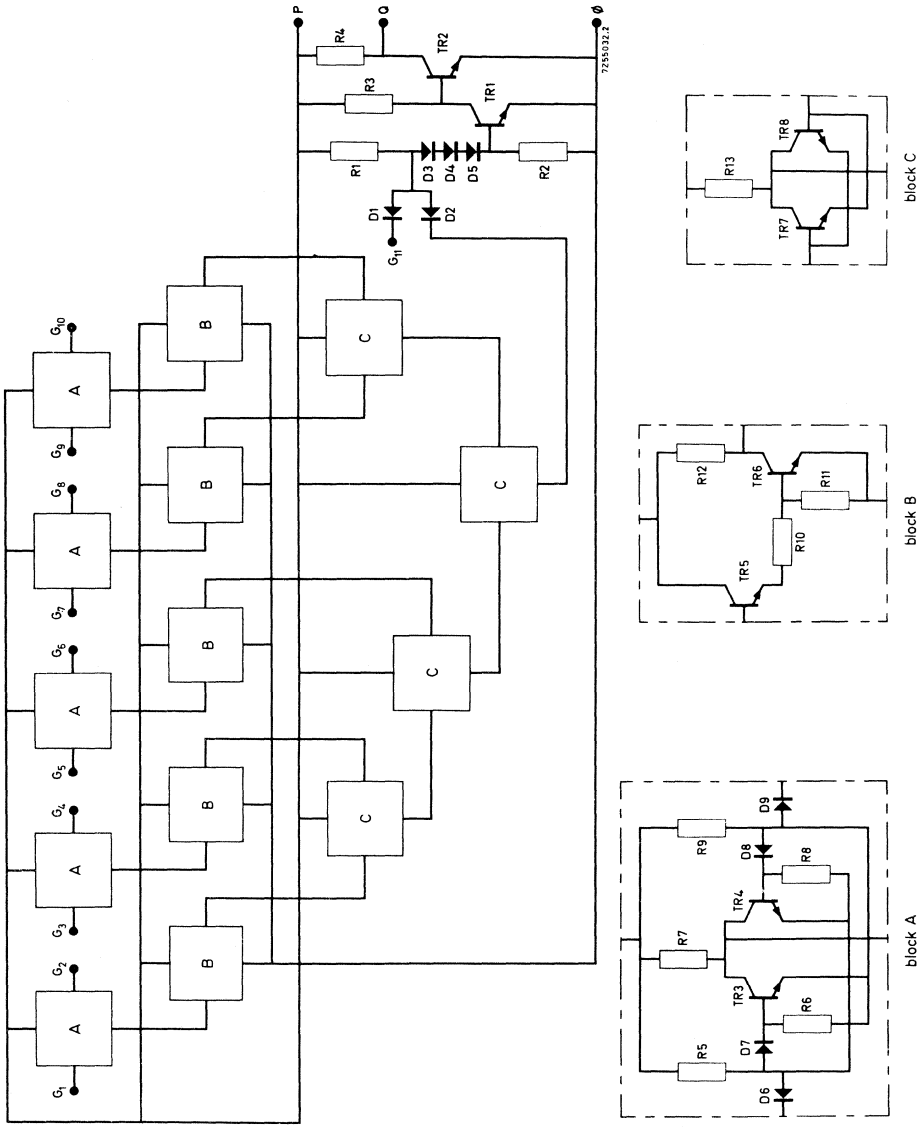


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C	t_{pd}	typ. 150	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 7	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 110	mW

The FCH291 comprises nine exclusive-OR functions followed by an AND gate. If an odd number of inputs (G_1 to G_{10}) are HIGH the output will be HIGH, provided G_{11} is HIGH. If an even number of inputs (G_1 to G_{10}) are HIGH the output will be LOW, provided G_{11} is HIGH. If G_{11} is LOW the output will be LOW regardless the condition of other inputs.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8	G_9	G_{10}	G_{11}	Q
Even number of inputs HIGH										H	L
Odd number of inputs HIGH										H	H
X	X	X	X	X	X	X	X	X	X	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20	mA[1]
Input current	$-I_G$	max.	20	mA[2]
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) For negative output voltage.
2) At this limit input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan-out	N_a	⩾	7	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	0.8	V
Average propagation delay time	t_{pd}	max.	250	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	21	mA
Power dissipation at T_{amb} = +75 °C	P_{tot}	max.	190	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	see note 1
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	see note 1
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7 and 6.3	I_Q = 0 (see note 1)
	V_{QHmin}	4.7	4.7	4.5	V	5.7	I_Q = −200 μA
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	3.8	3.8	3.4	V	5.7 and 6.3	
Input current LOW	$-I_{G1\ to\ 10\ Lmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	$V_{G1\ to\ 10}$ = 0.4 V $V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G11max}$	1.9 2.1	1.8 2.0	1.7 1.9	mA mA	5.7 6.3	V_{G11} = 0.4 V V_{G11} = 0.4 V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Supply current	I_{Pmax}	32.0	30.5	28.0	mA	6.3	G inputs LOW

Note 1

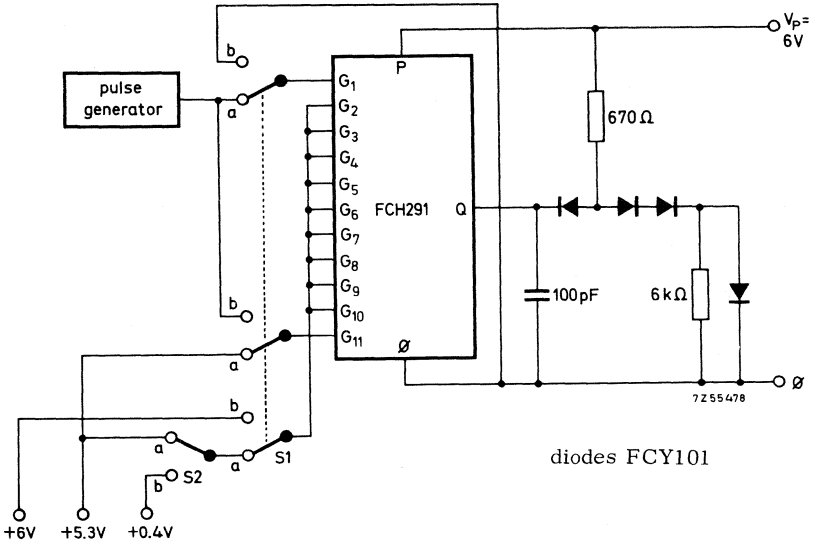
For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

		T_{amb} (°C) 0 +25 +75			V_P (V)	Conditions and references	Fig.
DYNAMIC DATA							
Propagation delay times from one G (G_1 to G_{10}) to Q							
Rise propagation delay time	t_{pdrmax}	-	200	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF all other inputs (including G_{11}) at V_G = 5.3 V	1; 2
Fall propagation delay time	t_{pdfmax}	-	200	- ns	6.0		
Rise propagation delay time	t_{pdrmax}	-	250	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF all other inputs (excluding G_{11}) at V_G = 0.4 V $V_{G_{11}}$ = 5.3 V	1; 3
Fall propagation delay time	t_{pdfmax}						
Propagation delay times from G_{11} to Q							
Rise propagation delay time	t_{pdrmax}	-	100	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF V_{G_1} = 0 V all other inputs at V_G = 6.0 V	1; 3
Fall propagation delay time	t_{pdfmax}	-	120	- ns	6.0		

CHARACTERISTICS (continued)

DYNAMIC DATA



diodes FCY101

Fig. 1 Equivalent load for N = 6; C_L [1]) = 100 pF

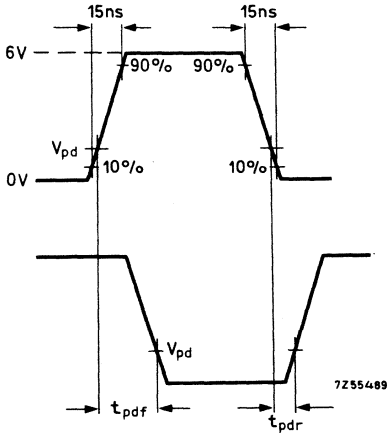


Fig. 2 Switch S2 in position a
Switch S1 in position a

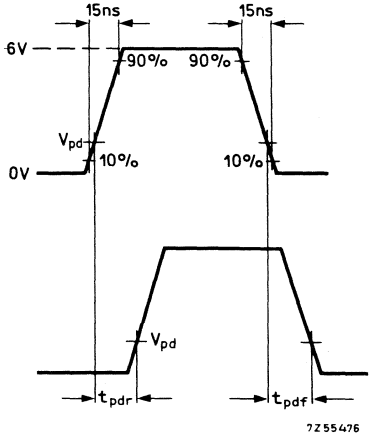


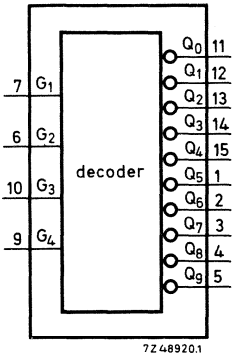
Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b
Switch S2 immaterial

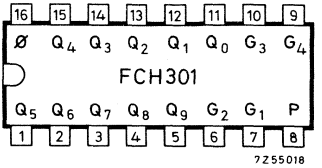
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 4-BIT DECODER



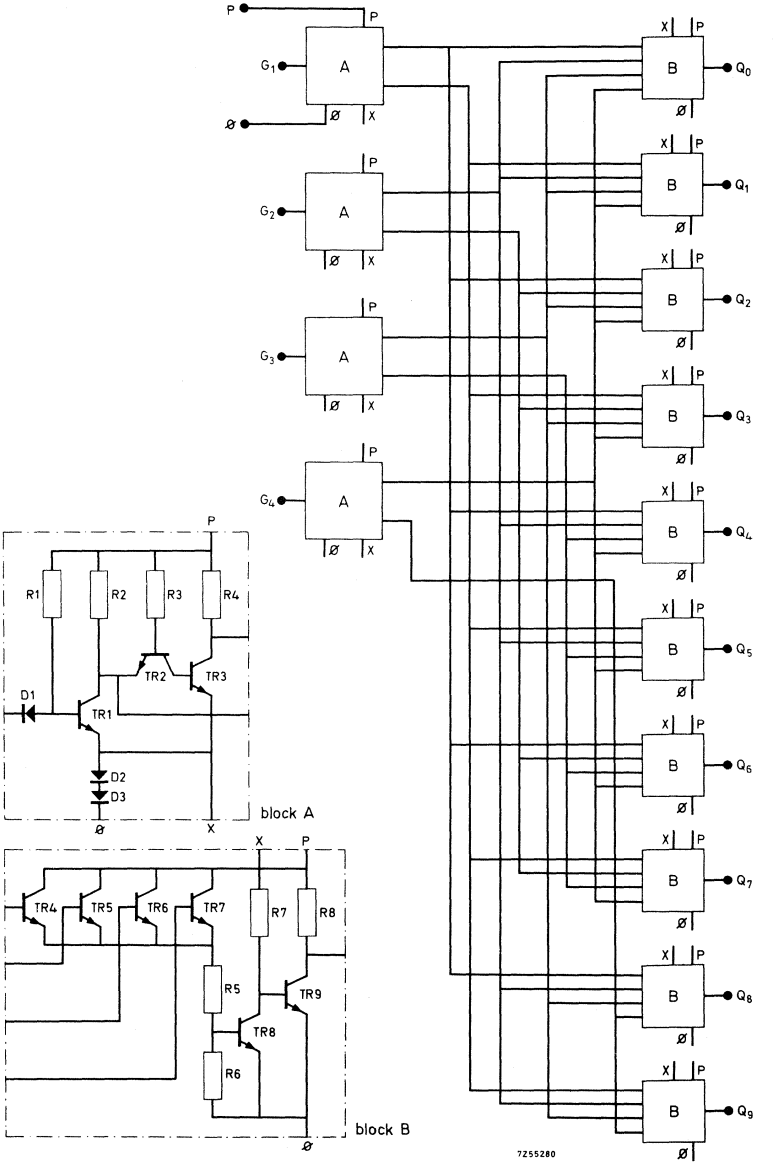


PACKAGE OUTLINE
16 lead plastic dual in-line (type A)
(See General Section)

QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 1, C_W = 40 pF, T_{amb} = 25 °C	t_{pd}	⩽ 100	ns
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 9	
D.C. noise margin T_{amb} = 25 °C	M_L	⩾ 0.6	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 250	mW

The FCH301 is a fast binary (8-4-2-1) to decimal decoder formed by 18 gate functions. All outputs except the decoded one stay HIGH. If the input does not conform to the 8-4-2-1 code, all outputs remain HIGH.

CIRCUIT DIAGRAMS



FUNCTION TABLE

G_4	G_3	G_2	G_1	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC FUNCTIONS

$$Q_0 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_1 = \overline{G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_2 = \overline{\overline{G_1} \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_3 = \overline{G_1 \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_4 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}}$$

$$Q_5 = \overline{G_1 \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}}$$

$$Q_6 = \overline{\overline{G_1} \cdot G_2 \cdot G_3 \cdot \overline{G_4}}$$

$$Q_7 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot \overline{G_4}}$$

$$Q_8 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4}$$

$$Q_9 = \overline{G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4}$$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage at T_{amb}: max. 40 °C	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Input current 1)	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−35 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) At this limit, input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Operating ambient temperature	T_{amb}		0 to +75	°C
Uniform system voltage	V_P		5.7 to 6.3	V
Available d.c. fan out	N_a		9	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	2.9	V
Average propagation delay time	t_{pd}		100	ns
Equivalent input capacitance	C_G	typ.	4	pF
Power dissipation	P_{tot}	max.	300	mW

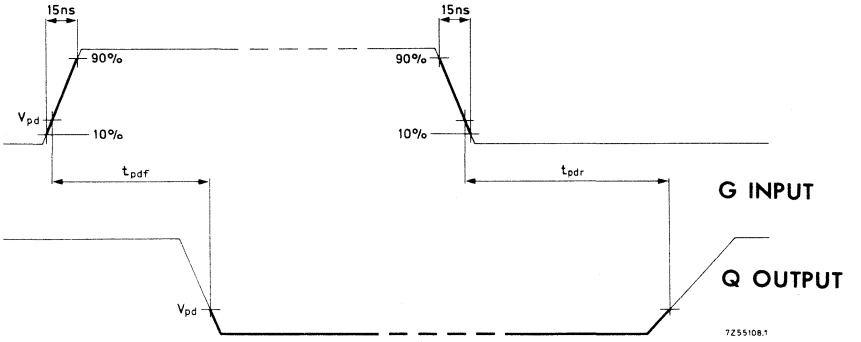
CHARACTERISTICS

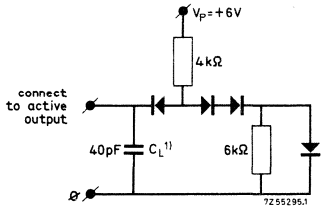
		T_{amb} (°C)				Conditions and References	
		0	25	75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	For the proper combination of inputs to be HIGH or LOW see Function Table
at:							
Output current LOW	I_{QLmax}	15.8	14.9	14.0	mA	5.7	
	I_{QLmax}	18.0	17.1	16.2	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.2	5.2	5.2	V	5.7	$-I_Q = 0$
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	2.6	2.5	2.4	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75	1.65	1.55	mA	5.7	$V_G = 0.4$ V
	$-I_{GLmax}$	2.0	1.9	1.8	mA	6.3	$V_G = 0.4$ V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA		$V_G = 6.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	–	48	mA	6.3	G inputs 0 V

CHARACTERISTICS (continued)

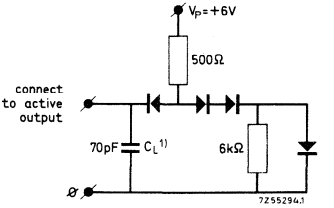
		T_{amb} (°C)				Conditions and References	
		0	25	75		V_P (V)	
DYNAMIC DATA*)							
Rise propagation delay time	t_{pdr} max	–	110	–	ns		V_{pd} = 1.5 V; N = 1; C_L = 40 pF
	t_{pdr} max	–	30	–	ns		V_{pd} = 1.5 V; N = 8; C_L = 70 pF
Fall propagation delay time	t_{pdf} max	–	85	–	ns		V_{pd} = 1.5 V; N = 1; C_L = 40 pF
	t_{pdf} max	–	100	–	ns		V_{pd} = 1.5 V; N = 8; C_L = 70 pF

*) See figures below





N = 1



N = 8

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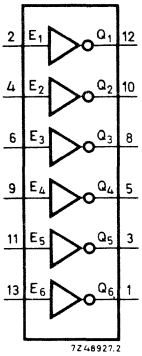
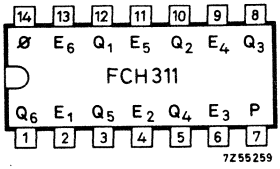
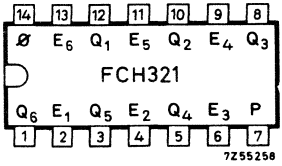
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.







	non-R_C	R_C
Sextuple inverter	FCH311	FCH321

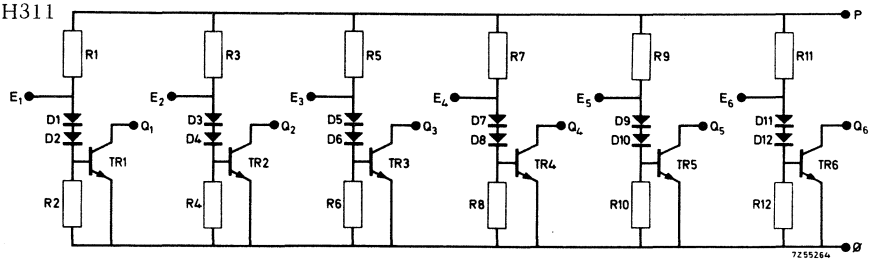
QUICK REFERENCE DATA				
Supply voltage		V_P	6.0 ± 5%	V
Operating ambient temperature range		T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C		t_{pd}	typ. 30	ns
Available d.c. fan out to FC gates T_{amb} = 0 to +75 °C		N_a	≥ 8	
Power consumption per inverter 50% duty cycle, T_{amb} = 25 °C	non-R_C	P_{av}	typ. 7	mW
	R_C	P_{av}	typ. 11	mW

The fan-in of the circuits can easily be expanded by means of a diode array.
The outputs of these inverters may be interconnected to perform the AND-OR-NOT function.

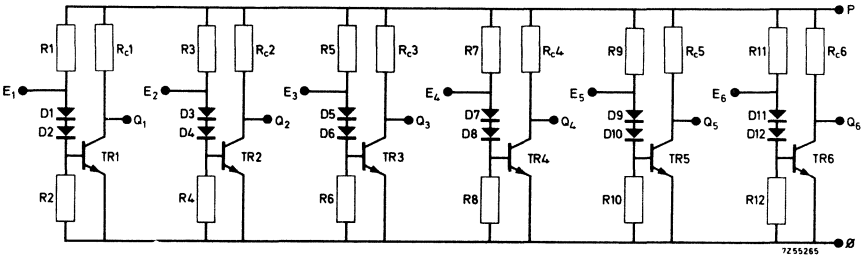
PACKAGE OUTLINES: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAMS

FCH311



FCH321



LOGIC FUNCTION

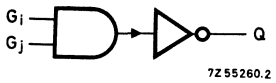
1. Individual inverter operation

$Q = \overline{E_i}$ for positive logic

Function table

E_i	Q
L	H
H	L

2. Individual gate operation



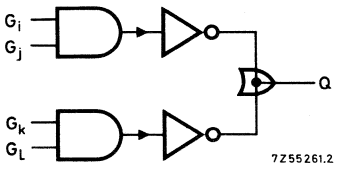
$Q = \overline{G_i \cdot G_j}$ for positive logic

Function table

G_i	G_j	Q
L	X	H
X	L	H
H	H	L

LOGIC FUNCTION (continued)

3. Commoned gate operation



Function table

G_i	G_j	G_k	G_l	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

$Q = (\overline{G_i.G_j}) \,.\, (\overline{G_k.G_l}) = \overline{(G_i.G_j) + (G_k.G_l)}$ for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

The AND-function is obtained by connecting a diode array to the E input.

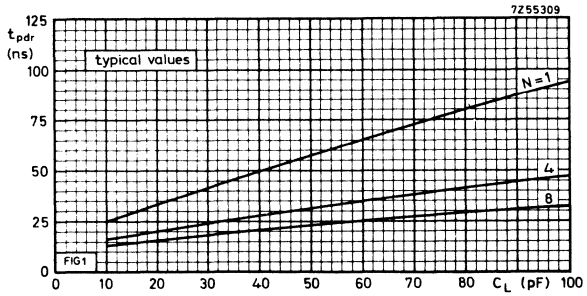
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage (HIGH state)	V_Q	max.	8.0	V
Output current [1])	$-I_Q$	max.	20	mA
Expander input voltages with respect to supply	V_P-V_E	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

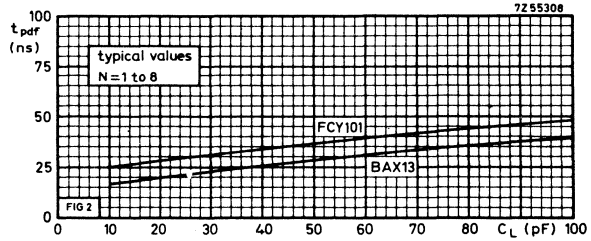
[1]) For negative output voltage.

SYSTEM DESIGN DATA (both non-R_c and R_c)

Uniform system temperature		T_{amb}	0 to +75		°C
Uniform system supply voltage		V_p	5.7 to 6.3		V
Available d.c. fan out to FC gates		N_a	≥	8	
Averaged propagation delay time with BAX13 diode		t_{pd}	max.	75	ns
Increase of t_{pdf} with increasing expander capacitance for C_w = 0 to 100 pF		Δt_{pdf}	typ.	1.4	ns/pF
Equivalent output capacitance		C_Q	typ.	10	pF
Supply current (duty cycle 50%)	non-R_c	I_{Pav}	typ.	7.2	mA
	R_c	I_{Pav}	typ.	10.5	mA
Power dissipation at T_{amb} = 75 °C	non-R_c	P_{tot}	max.	100	mW
	R_c	P_{tot}	max.	171	mW



t_{pdr} versus C_L for both BAX13 and FCY101 as input diode



t_{pdf} versus C_L for BAX13 and FCY101 as input diode

CHARACTERISTICS of FCH311 (non R_C)

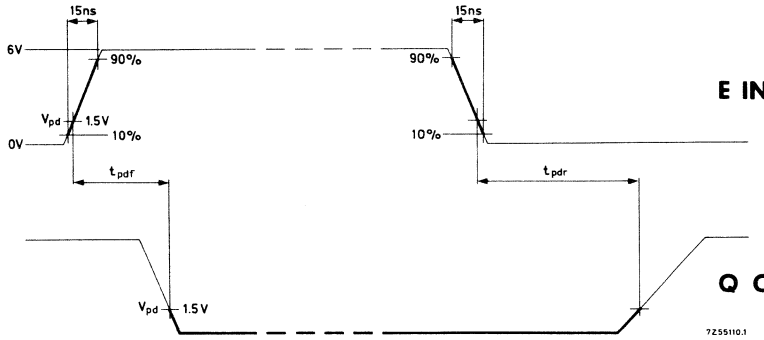
		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	$-I_E$ = 50 μA
at:							
Output current LOW	I_{QLmax}	16.0 18.0	15.1 17.0	14.2 16.0	mA mA	5.7 6.3	
Expander input voltage HIGH	V_{EHmax}	3.0	2.8	2.6	V	5.7 and 6.3	I_{QL} = I_{QL} max $-I_E$ = 50 μA
Input current LOW	$-I_{ELmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	
at:							
Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Output current HIGH	I_{QHmax}	70	70	70	μA	5.7 and 6.3	V_Q = 5.3 V
at:							
Expander input voltage LOW	V_{ELmax}	1.8	1.7	1.4	V	5.7 and 6.3	
Supply current	I_{PHmax}	12.0	11.4	10.8	mA	6.3	
at:							
Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Supply current	I_{PLmax}	11.4	10.2	10.2	mA	6.3	Expander inputs floating
DYNAMIC DATA see also page 7							
	t_{pdr} max	–	85	–	ns	6.0	R = 4 kΩ C_L = 40 pF
Rise propagation delay time	t_{pdr} max	–	70	–	ns	6.0	R = 670 Ω C_L = 60 pF
	t_{pdf} max	–	65	–	ns	6.0	R = 4 kΩ C_L = 40 pF
Fall propagation delay time	t_{pdf} max	–	85	–	ns	6.0	R = 670 Ω C_L = 60 pF

CHARACTERISTICS of FCH321 (R_c)

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	$-I_E$ = 50 μA
at:							
Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
		16.0	15.2	14.4	mA	6.3	
Expander input voltage HIGH	V_{EHmax}	3.0	2.8	2.6	V	5.7 and 6.3	I_{QL} = I_{QL} max; $-I_E$ = 50 μA
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	I_Q = 0
at:		4.1	4.1	3.9	V	5.7	I_Q = −200 μA
Expander input voltage LOW	V_{ELmax}	1.8	1.7	1.4	V	5.7 and 6.3	
Input current LOW	$-I_{ELmax}$	1.75	1.65	1.55	mA	5.7	
at:		2.0	1.9	1.8	mA	6.3	
Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Output current LOW (AND-OR-NOT function)	$-I_{QLLmax}$	2.2	2.1	2.0	mA	6.3	Expander inputs LOW Output forced LOW externally to V_Q = 0.4 V
Supply current	I_{PLmax}	25.2	22.8	21.6	mA	6.3	Expander inputs floating
DYNAMIC DATA see also page 7							
Rise propagation delay time	$t_{pdr\ max}$	–	85	–	ns	6.0	R = 4 kΩ, C_L = 40 pF
	$t_{pdr\ max}$	–	70	–	ns	6.0	R = 670 Ω, C_L = 60 pF
Fall propagation delay time	$t_{pdf\ max}$	–	65	–	ns	6.0	R = 4 kΩ, C_L = 40 pF
	$t_{pdf\ max}$	–	85	–	ns	6.0	R = 670 Ω, C_L = 60 pF

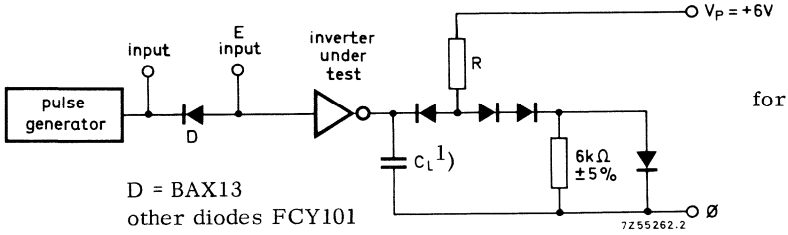
CHARACTERISTICS (continued)

DYNAMIC DATA



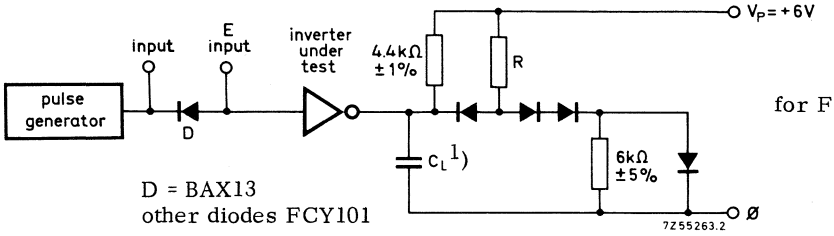
E INPUT

Q OUTPUT



D = BAX13
other diodes FCY101

for FCH321



D = BAX13
other diodes FCY101

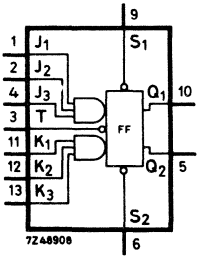
for FCH311

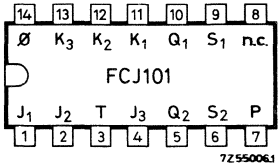
Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK FLIP-FLOP



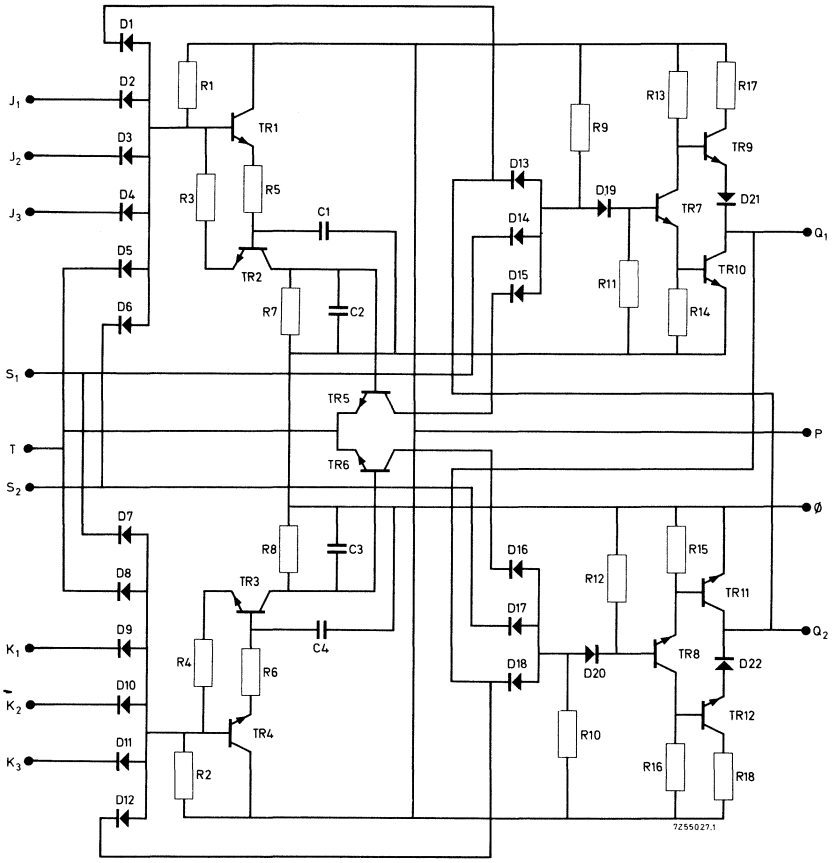


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 10	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 36	mW

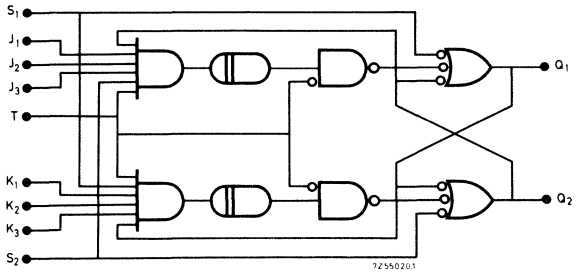
The FCJ101 performs the JK flip-flop operation. Three J and three K inputs permit an additional AND operation. Triggering occurs at the falling edge of a T signal. The direct-set inputs (overriding any other inputs) are active at the LOW level. The circuitry incorporates bi-directional outputs for driving capacitive loads. Typical applications are in high speed counters and shift registers.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the flip-flop by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 and S_2 should be HIGH or floating.

$J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$ } for positive logic

2. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage in LOW state.
3) At this limit input voltage typ. : −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	4	
to G input	N_{aG}	⩾	8	
Available a.c. fan out				
to T input	N_{aT}	⩾	2	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	0.2	V
to J or K input	M_L	min.	0.5	V
	M_H	min.	0.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	0.2	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	85	ns
Maximum clock rate	f_c	⩾	6	MHz
Equivalent input capacitances				
for T input	C_T	typ.	30	pF
for J or K input	$C_J = C_K$	typ.	20	pF
for S input	C_S	typ.	25	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	6.0	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	56	mW

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references	
		0	+25	+75	V_P (V)	
STATIC DATA						
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4 V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 mA 14.4 mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1 V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0 V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5 mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75 2.0	1.65 1.9	1.55 mA 1.8 mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	3.5 4.0	3.3 3.8	3.1 mA 3.6 mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{SLmax}$	3.5 4.0	3.3 3.8	3.1 mA 3.6 mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	$-I_{JHmax}$, $-I_{KHmax}$	1	1	25 μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50 μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50 μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	9	– mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	3.6	3.3	3.0	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH	t_{THmin}	50	50	50	ns			1
followed by:	$(-\frac{dt}{dV})_{Tmax}$	18	18	18	ns/V			1
T-input slope	$(-\frac{dt}{dV})_{Tmin}$	4	4	4	ns/V			1
to: T-input voltage LOW	V_{TLmax}	0.7	0.7	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
JK-input voltage LOW during:	V_{JLmax} V_{KLmax}	1.1	1.0	0 9	V		J and K turning LOW after T and J and/or K having	2
JK-input time LOW	t_{JLmin} t_{KLmin}	100	100	160	ns		been HIGH simultaneously	2
Clock skew protection								
Hold time LOW	$t_{holdLmax}$	15	15	15	ns			2
Hold time HIGH	$t_{holdHmax}$	7	10	10	ns			3
Set or Reset								
S-input voltage LOW	V_{SLmax}	1.0	0.9	0.7	V		active $t_{SLmin} = t_{pdf}$	4
S-input voltage HIGH	V_{SHmin}	3.6	3.3	3.0	V		inactive	
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	70	–	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 60 pF	5
Fall propagation delay time	$t_{pdf\,max}$	–	100	–	ns	6.0	V_{pd} = 1.5 V N = 8; C_L = 60 pF other output N = 1 C_L = 60 pF	5

CHARACTERISTICS (continued)

DYNAMIC DATA

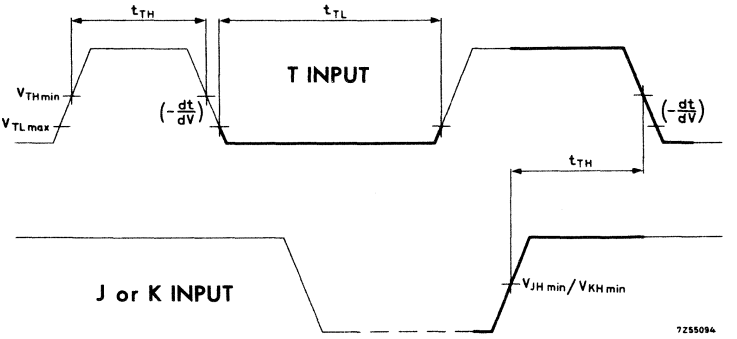


Fig.1. Waveforms illustrating conditions for change of state.

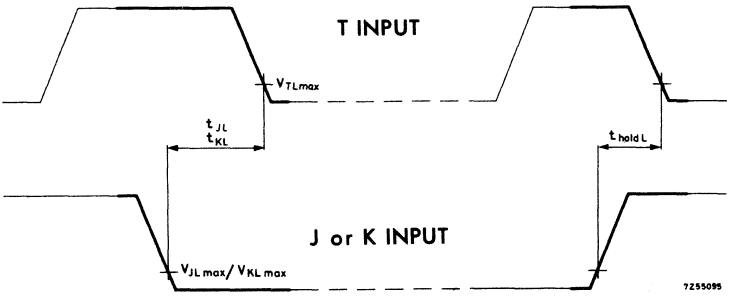


Fig.2. Waveforms illustrating conditions for no change of state.

For no change of state to result:

a. the time between J or K reaching V_{JLmax}, V_{KLmax} (going LOW) and T reaching V_{TLmax} (going LOW) must be at least t_{JLmin}, t_{KLmin}.

b. the time between J or K reaching V_{JLmax}, V_{KLmax} (going HIGH) and T reaching V_{TLmax} (going LOW) must be less than t_{holdL}.

CHARACTERISTICS (continued)

DYNAMIC DATA

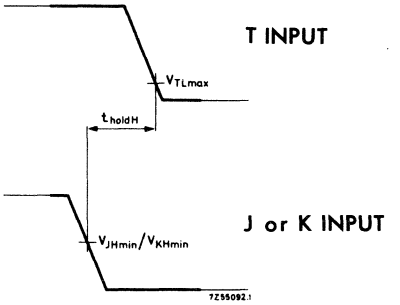


Fig.3. Waveforms illustrating conditions for change of state.
For a change of state still to result, the time between J or K reaching V_{JHmin}, V_{KHmin} (going LOW) and T reaching V_{TLmax} (going LOW) must be less than t_{holdH}

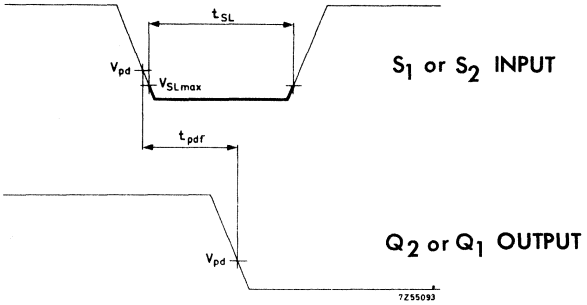
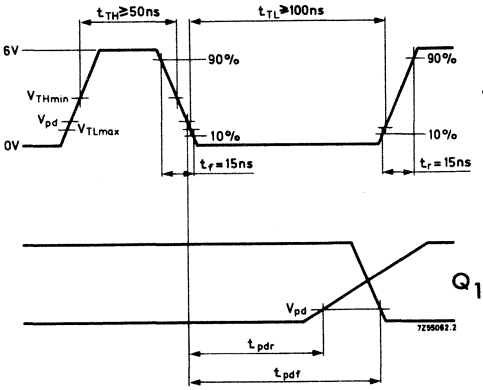
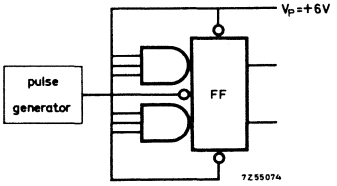


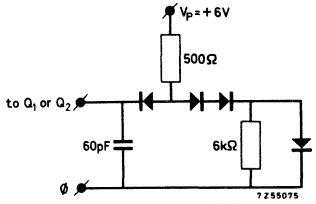
Fig.4. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

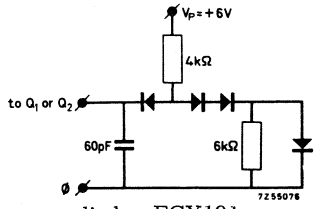






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 60 pF



diodes FCY101

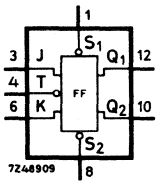
Equivalent load for N = 1 and C_L[1]) = 60 pF

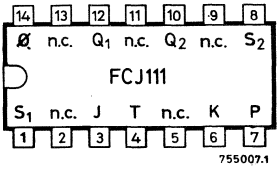
Fig. 5. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



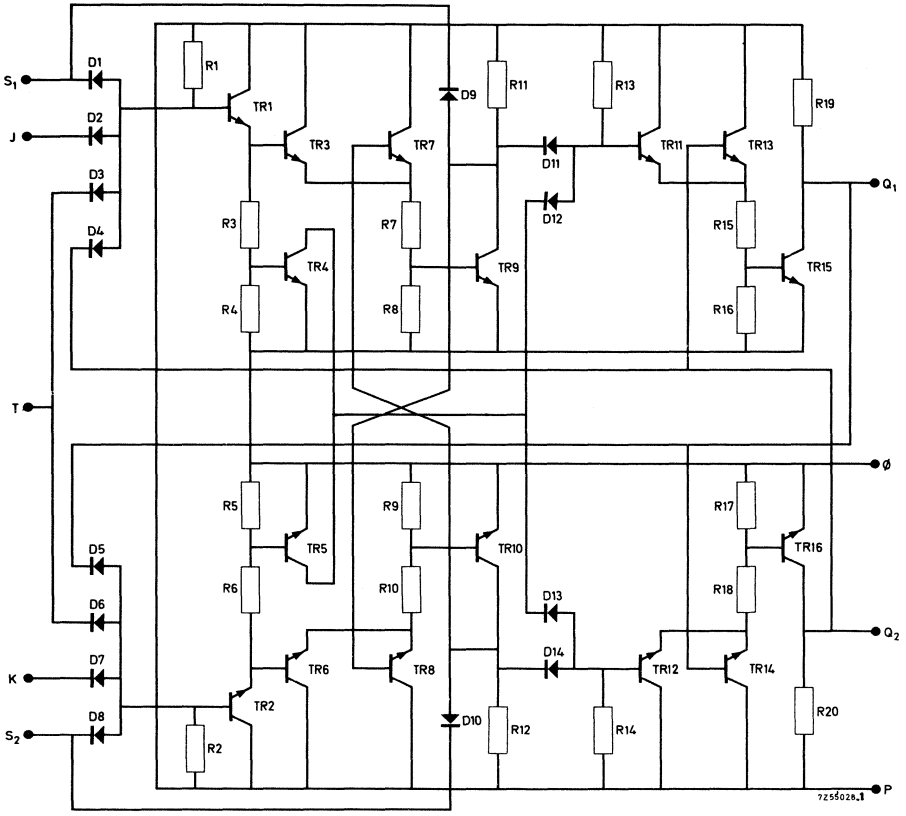


QUICK REFERENCE DATA			
Supply voltage	V_P	$6.0 \pm 5\%$	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 5	MHz
Available d.c. fan-out T_{amb} = 0 to 75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 67	mW

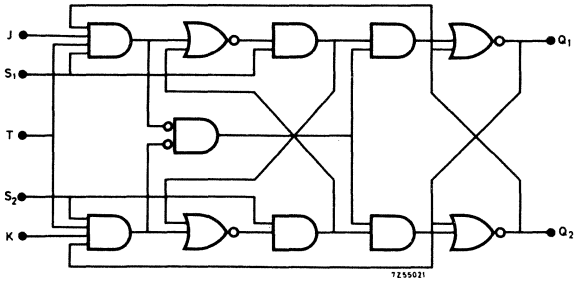
The FCJ111 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set-inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 or S_2 should be HIGH or floating.

2. Trigger action via J and K terminals

J	K	Q_1	Q_2
H→L	X	H	L
X	H→L	L	H
H→L	H→L	reversed	

If J or K go LOW with T HIGH, Q_1 and Q_2 assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q_1 and Q_2 are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K. S_1 and S_2 should be HIGH or floating.

3. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	indeterminate	
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the flip-flop.
In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

[1] For negative output voltage.
[2] At this limit input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	4	
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	5	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.5	V
	M_H	min.	1.9	V
to J or K input	M_L	min.	0.9	V
	M_H	min.	1.9	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	2.3	V
Average propagation delay time	t_{pd}	max.	150	ns
Maximum clock rate	f_c	⩾	3	MHz
Equivalent input capacitances				
for T input	C_T	typ.	8	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	11.2	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	110	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
		16.0	15.2	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.4	5.3	V	5.7	$I_Q = 0$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.9	3.5	2.8	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	350	450	550	μA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75	1.65	1.55	mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		2.0	1.9	1.8	mA	6.3	
	$-I_{TLmax}$	3.5	3.3	3.1	mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.0	3.8	3.6	mA	6.3	
	$-I_{SLmax}$	2.7	2.6	2.4	mA	5.7	$V_S = 0.4$ V; other inputs floating
		3.0	2.9	2.7	mA	6.3	
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	20	–	mA	6.3	J, K, S, T inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references		
		0	+25	+75	V_P (V)		fig.
DYNAMIC DATA					5.7 and 6.3		
Change of state							
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	3.1	2.9	2.5 V		HIGH level at T and J and/or K to be present simultaneously	1
during: T-input time HIGH to: Input voltage LOW	t_{THmin}	100	100	100 ns			1
	V_{TLmax}	1.3	1.1	0.9 V		$t_{TLmin} = t_{pdr}$	1
No change of state							
JK input voltage LOW	V_{JLmax} V_{KLmax}	1.8	1.6	1.3 V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection							
Hold time	$t_{holdmax}$	20	20	20 ns			2
Set or Reset							
S input voltage LOW	V_{SLmax}	1.2	1.0	0.8 V		active $t_{SLmin} = t_{pdr}$	3
S input voltage HIGH	V_{SHmin}	3.1	2.9	2.5 V		inactive	
DYNAMIC DATA							
Propagation delay times from T to Q							
Rise propagation delay time	t_{pdrmax}	-	200	- ns		$V_{pd} = 1.5$ V; N = 1; C_L = 60 pF other output N = 8; C_L = 56 pF	4
Fall propagation delay time	t_{pdfmax}	-	100	- ns		$V_{pd} = 1.5$ V; N = 8; C_L = 56 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

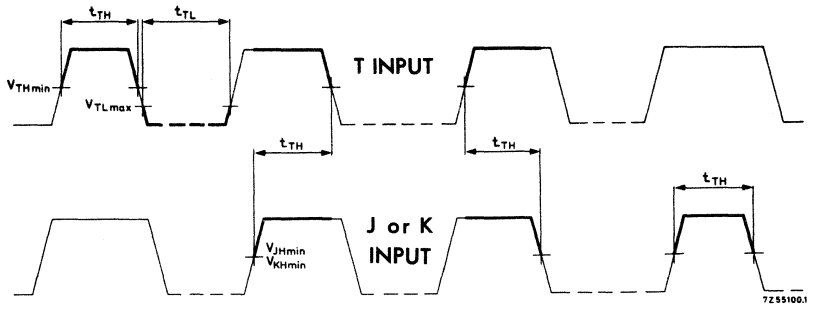


Fig. 1. Waveforms illustrating conditions for change of state.

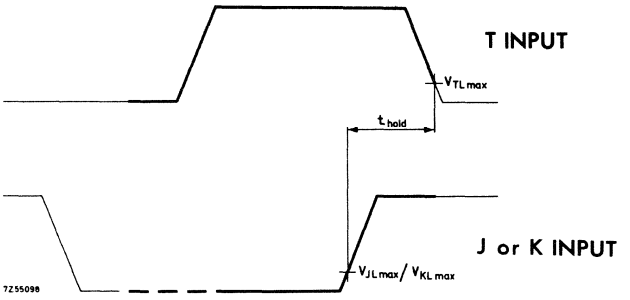


Fig. 2. Waveforms illustrating conditions for no change of state.

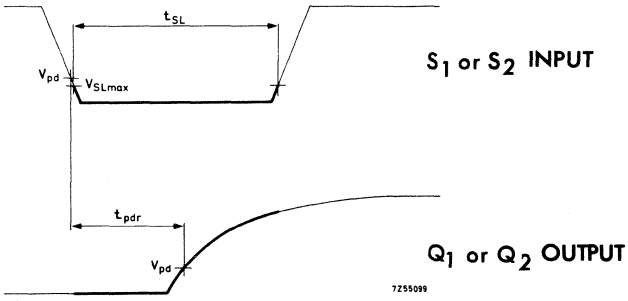
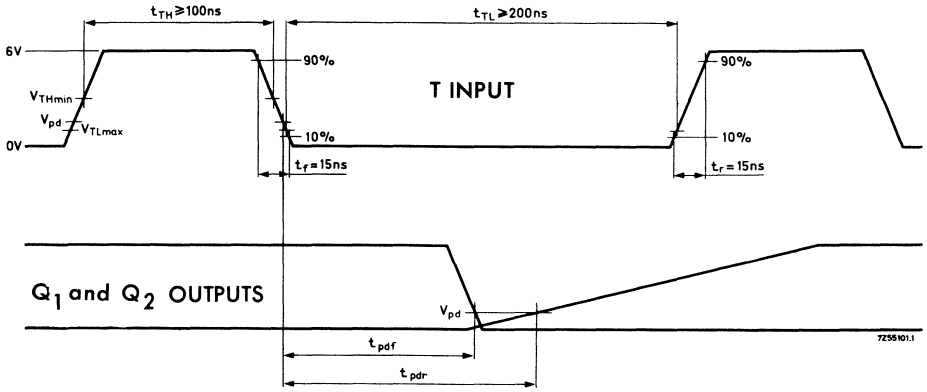
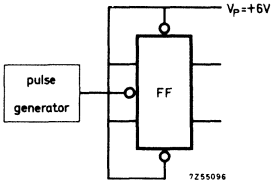


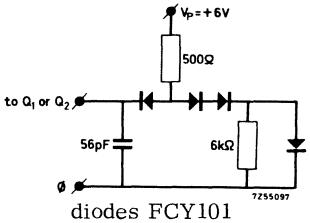
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

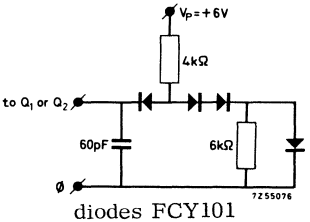






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 56 pF



diodes FCY101

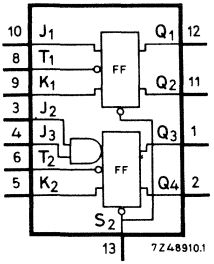
Equivalent load for N = 1 and C_L[1]) = 60 pF

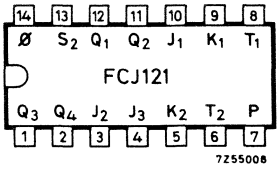
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



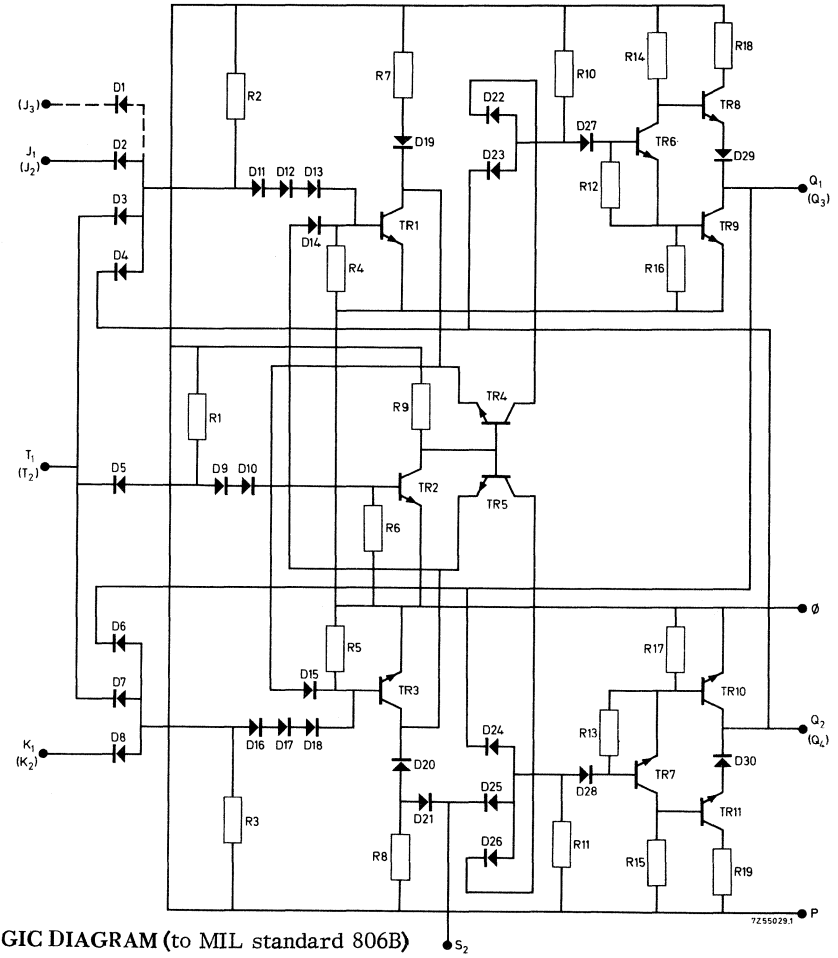


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C (each flip-flop)	P_{av}	typ. 50	mW

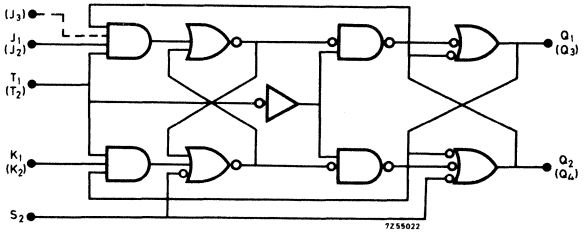
The FCJ121 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals including trigger signals are immaterial. The common set-input (overriding any other inputs) is active at the LOW level. Typical applications are in medium speed counters.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J_2	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Input S_2 should be HIGH or floating.

For the flip-flop with two J-inputs: $J = J_2 \cdot J_3$ for positive logic

2. Set or Reset via S_2 terminal (both flip-flops)

S_2 S_4	Q_1 Q_3	Q_2 Q_4
L	L	H
H	no change	

The set input overrides the other inputs and directly determines the outputs of both flip-flops.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

[1] Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

[2] For negative output voltage in LOW state.

[3] At this limit input voltage typ. : −1.5 V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_F	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS}	⩾	2	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	16	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QL}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible) at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	4.0 4.5	3.8 4.2	3.5 3.9	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{SLmax}$	5.7 6.6	5.5 6.3	5.2 5.8	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	V_{pd} = 1.5 N = 8; C_L = 60 pF other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS(continued)

DYNAMIC DATA

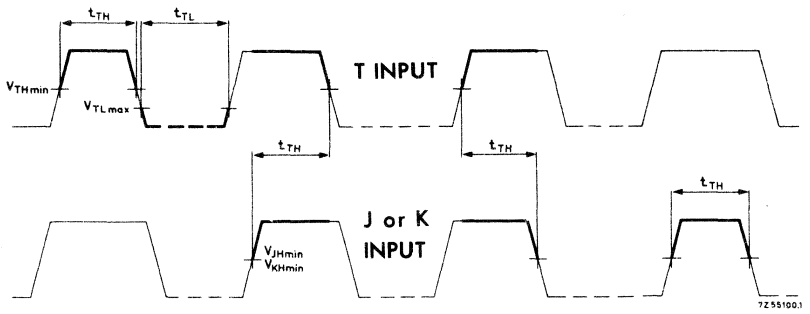


Fig. 1. Waveforms illustrating conditions for change of state.

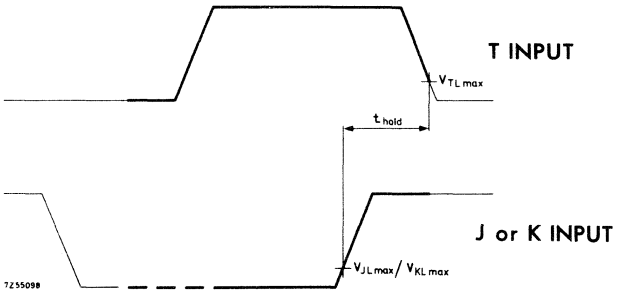


Fig. 2. Waveforms illustrating conditions for no change of state.

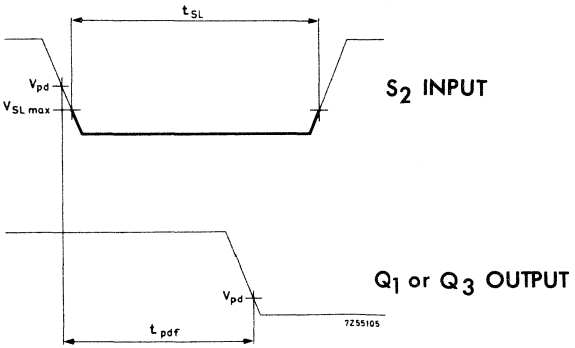
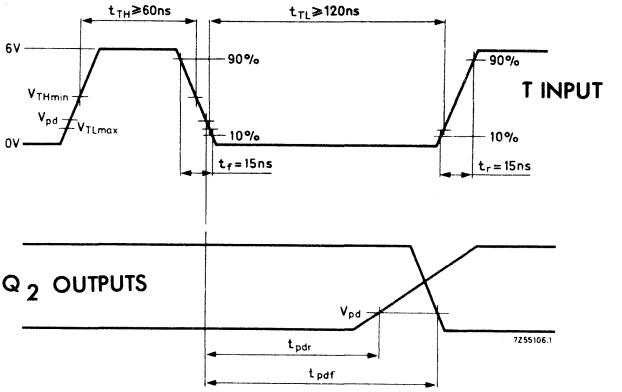
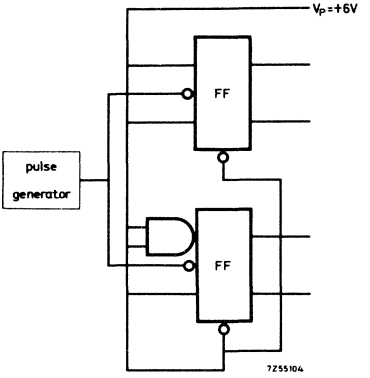


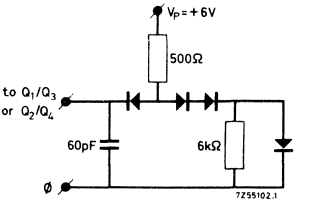
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

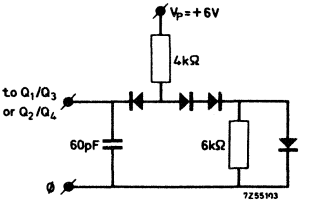






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 60 pF



diodes FCY101

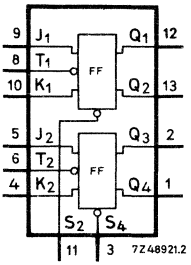
Equivalent load for N = 1 and C_L[1]) = 60 pF

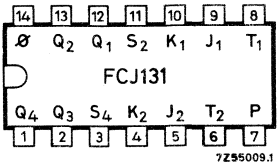
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP FLOP



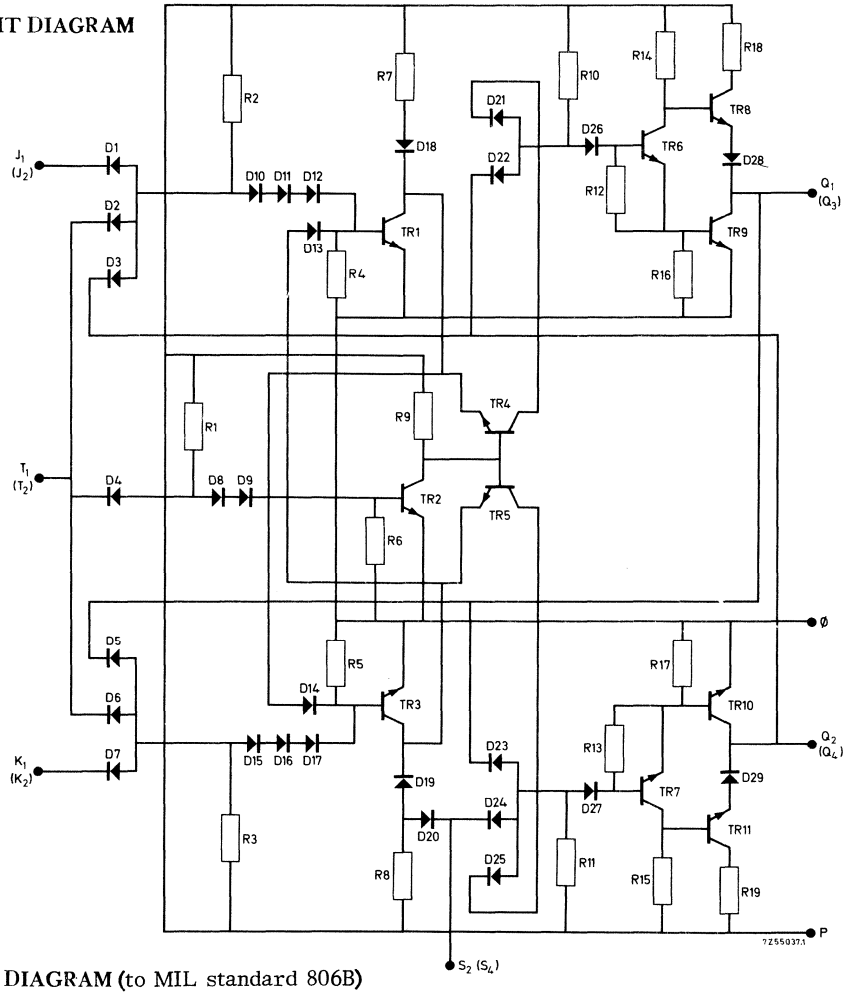


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

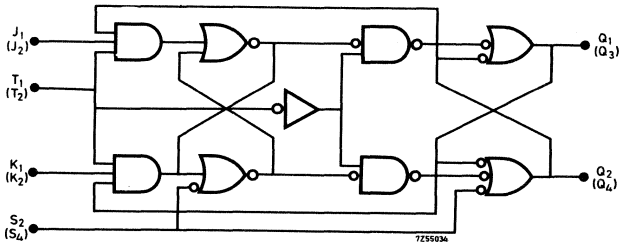
The FCJ131 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signals, are immaterial. The separate set inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J_2	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_2 and S_4 should be HIGH or floating.

2. Set or reset via S terminals (each flip-flop)

S_2 S_4	Q_1 Q_3	Q_2 Q_4
L	L	H
H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1])	$-I_Q$	max.	20	mA
Input current [2])	$-I_J$, $-I_K$, $-I_T$, $-I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

[1]) For negative output voltage in LOW state.
[2]) At this limit input voltages typ. : −1.5V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS}	⩾	4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	4.0 4.5	3.8 4.2	3.5 3.9	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{SLmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T inputs LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	$V_{pd} = 1.5$ V N = 1; $C_L = 60$ pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	$V_{pd} = 1.5$ N = 8; $C_L = 60$ pF other output: N = 1; $C_L = 60$ pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

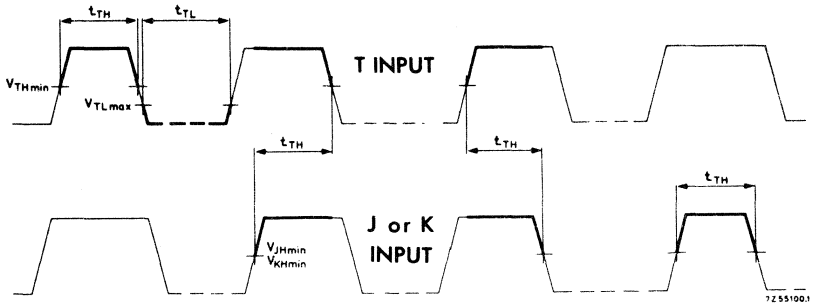


Fig. 1. Waveforms illustrating conditions for change of state.

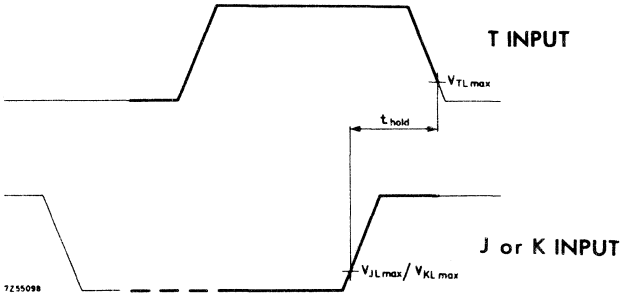


Fig. 2. Waveforms illustrating conditions for no change of state.

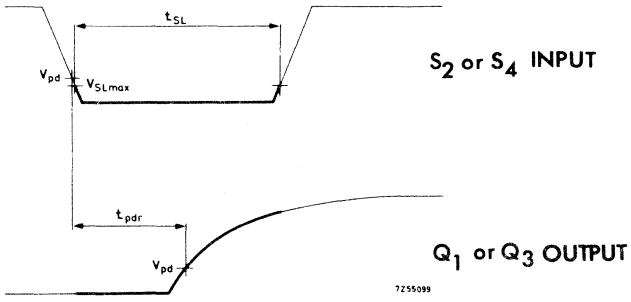
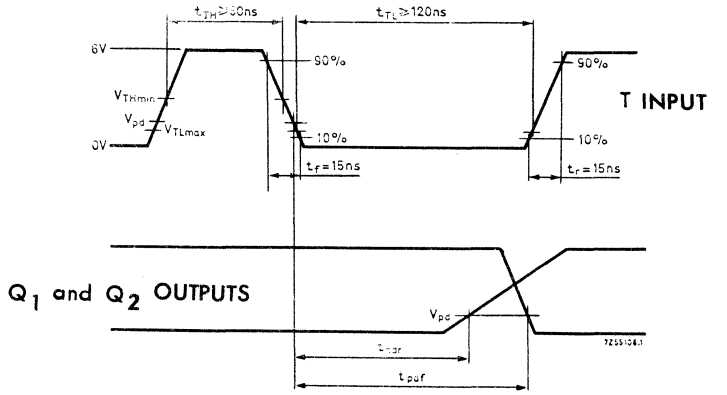
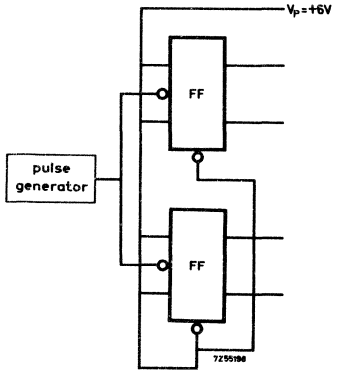


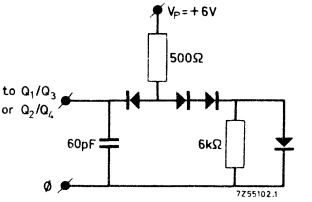
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

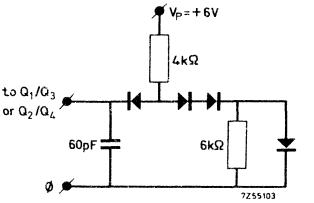
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and C_L[1]) = 60 pF



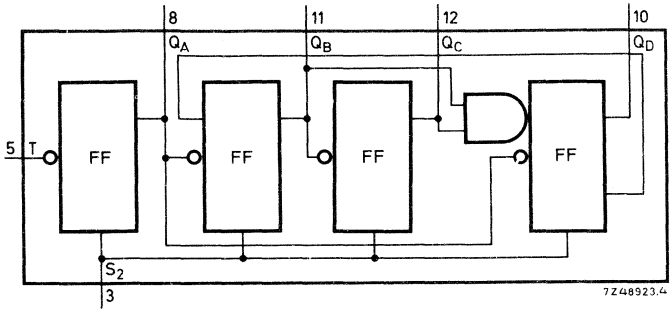
Diodes FCY101
Equivalent load for N = 1 and C_L[1]) = 60 pF

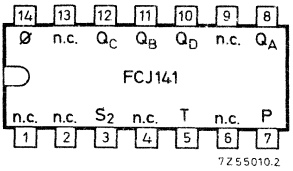
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE ASYNCHRONOUS 10-COUNTER



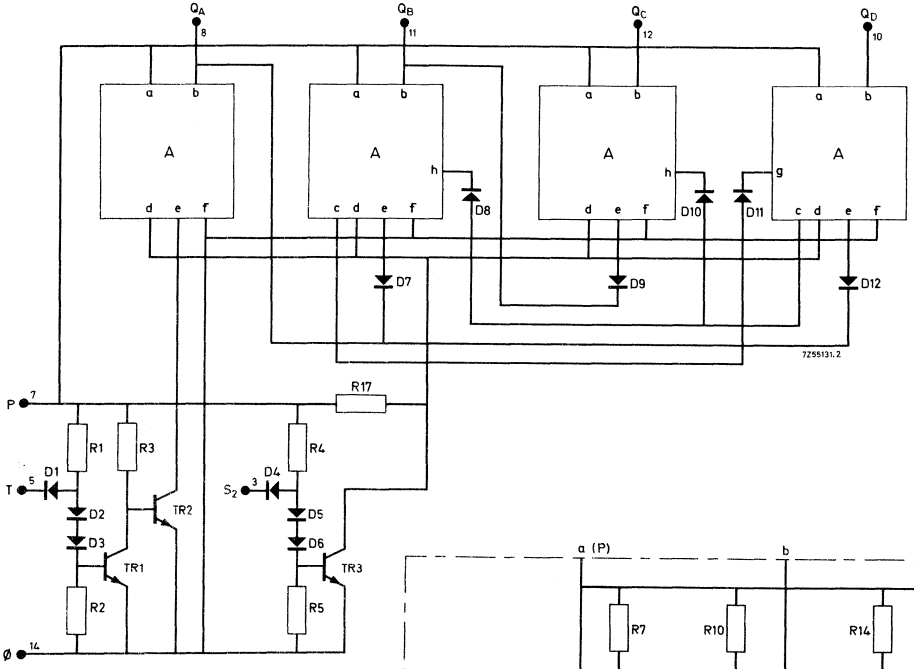


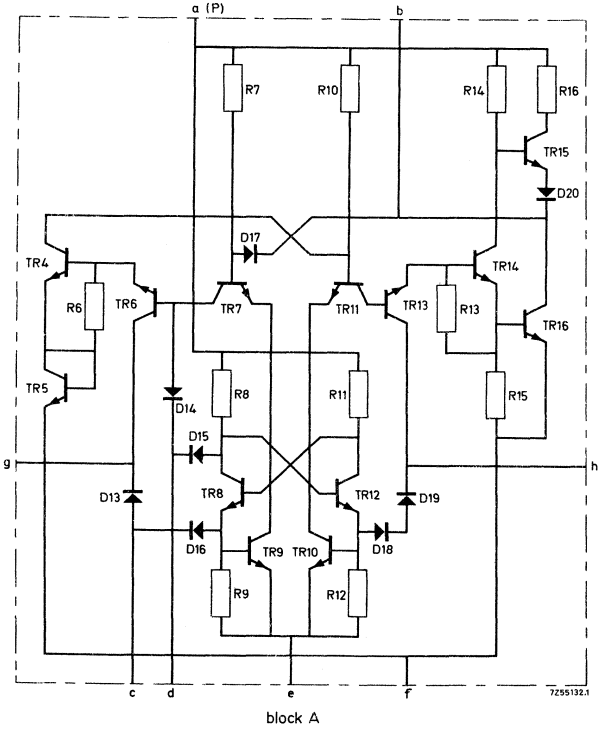
QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 180	mW

The FCJ141 is four master-slave flip-flops interconnected to form an a-synchronous decade counter in the 8-4-2-1 code. The information is transferred to the master when the trigger signal is HIGH (the first flip-flop is triggered by the count input at T). When the trigger signal is LOW the information is transferred to the slaves and appears at the outputs. A common reset input S_2 directly resets the outputs and overrides the T input.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS





block A

FUNCTION TABLES

Count	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

S_2	Q_D	Q_C	Q_B	Q_A
L	count			
H	L	L	L	L

Input S when being at the HIGH state overrides the count input and directly resets all outputs in the LOW state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Input voltage	V_T; V_S	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input current [1]	$-I_S$; $-I_T$	max.	20	mA
Output current [2]	$-I_Q$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−35 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) At this limit, input voltage typ. −1.5 V.

2) For negative output voltage in LOW state.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out	N_a	≥	8	
D.C. noise margin				
to T input	M_L	min.	0.4	V
	M_H	min.	1.6	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.6	V
Average propagation delay time T input to Q_3 output	t_{pd}	typ.	200	ns
Clock rate	f_c	max.	3.5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	4	pF
for S input	C_S	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	max.	46	mA
Power dissipation at $T_{amb} = 75\,^{o}C$	P_{tot}	max.	270	mW

CHARACTERISTICS

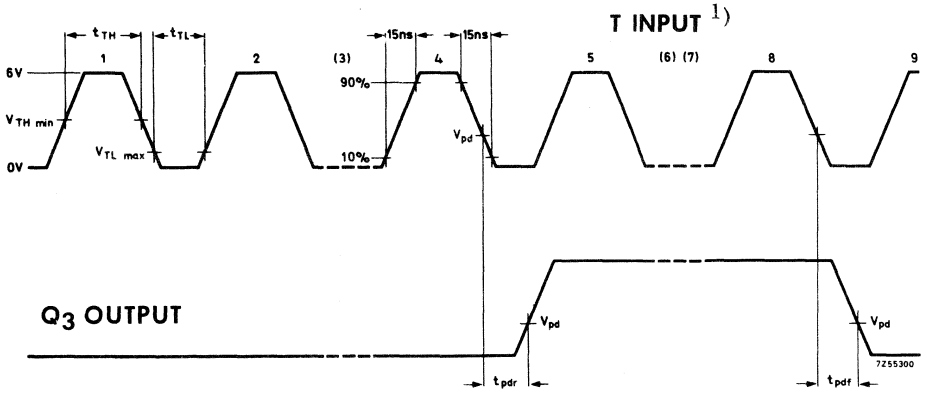
		T_{amb}(°C)				Conditions and references	
		0	25	75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QL} max.	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
	I_{QLmax}	16.0	15.2	14.4	mA	6.3	
Output voltage HIGH	V_{QH} min.	3.8	3.9	4.1	V	5.7	
at: Output current HIGH	$-I_{QH}$	100	100	100	µA	5.7	
Output voltage HIGH (lowest permissible)	V_{QHP} min.	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{TL}$ max.	1.75	1.65	1.55	mA	5.7	$V_T = V_S = 0.4$ V
	$-I_{SL}$ max.	1.75	1.65	1.55	mA	5.7	
	$-I_{TL}$ max.	2.0	1.9	1.8	mA	6.3	
	$-I_{SL}$ max.	2.0	1.9	1.8	mA	6.3	
Input current HIGH	I_{TH} max. I_{SH} max.	1.0	1.0	25.0	µA	5.7	$V_T = V_S = 5.3$ V
Supply current	I_{Pmax}	–	45	40	mA	6.3	$V_T = 0$ V, V_S = floating

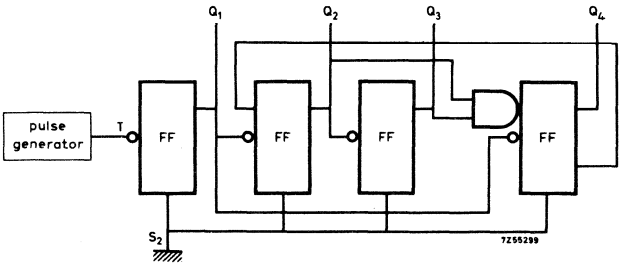
CHARACTERISTICS (continued)

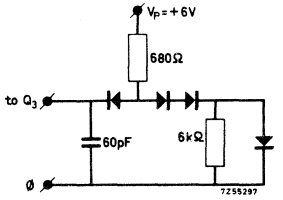
STATIC AND DYNAMIC DATA		T_{amb} (°C) 0	25	75		Conditions and references V_P (V)	
Reset input active HIGH level at S	V_{SHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
to be present during	t_{SHmin}	100	100	140	ns		
Reset input inactive LOW level at S	V_{SLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Change of state of the master of the lowest order flip-flop HIGH level at T	V_{THmin}	2.3	2.2	2.1	V	5.7 and 6.3	
to be present during	t_{THmin}	-	100	-	ns		
Change of state of the slave of the lowest order flip-flop							
Slope of falling edge at T	$(-\frac{dt}{dV})_{Tmax}$	1	1	1	µs/V		
LOW level at T	V_{TLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
to be present during	t_{TLmin}	100	100	140	ns		
Propagation delay times from T to Q3							
Propagation delay reference level	V_{pd}		1.5		V		
Rise propagation delay time	$t_{pdr\ max}$	-	200	-	ns	6.0	
Fall propagation delay time	$t_{pdf\ max}$	-	200	-	ns	6.0	

CHARACTERISTICS (continued)

DYNAMIC DATA



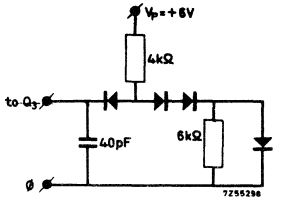




diodes FCY101

C_L 2) = 60 pF

Equivalent load for N = 6



diodes FCY101

C_L 2) = 40 pF

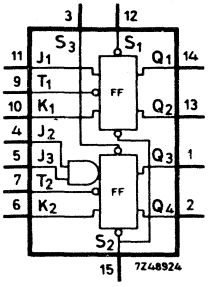
Equivalent load for N = 1

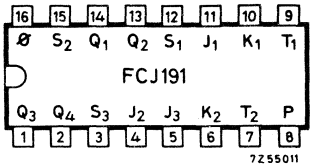
1) The falling edge of the T input signals is max. 1 μs/V

2) Including jig and probe capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



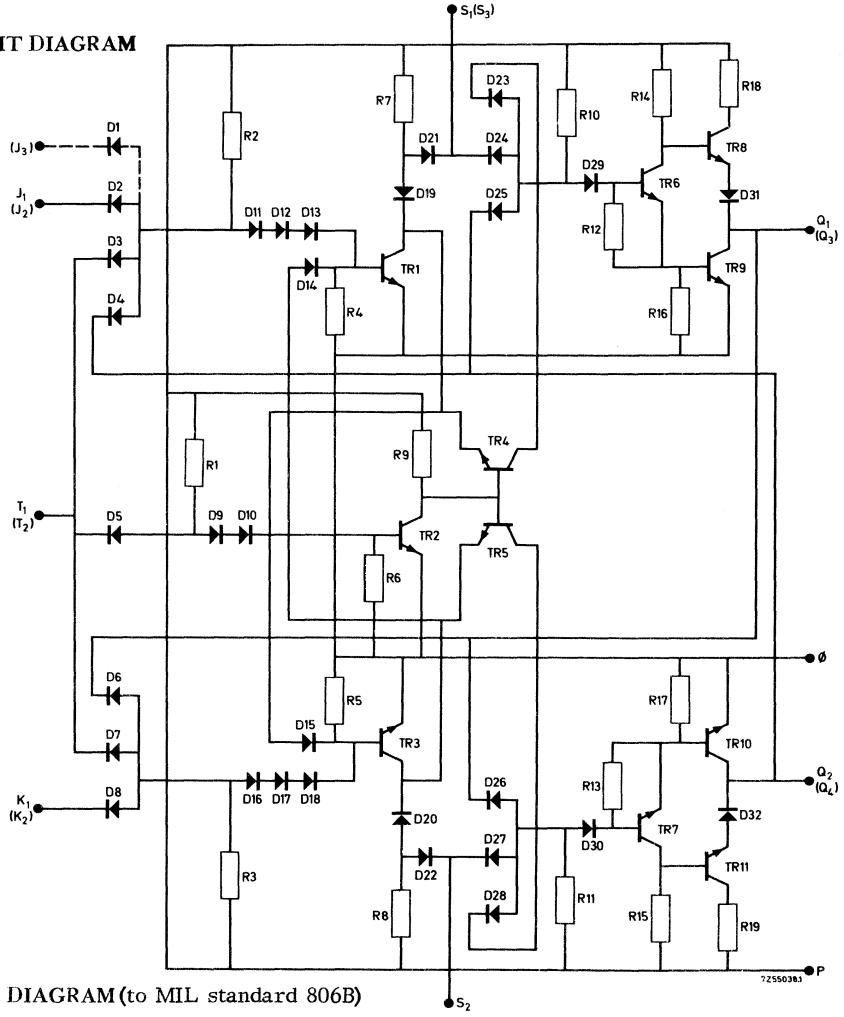


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

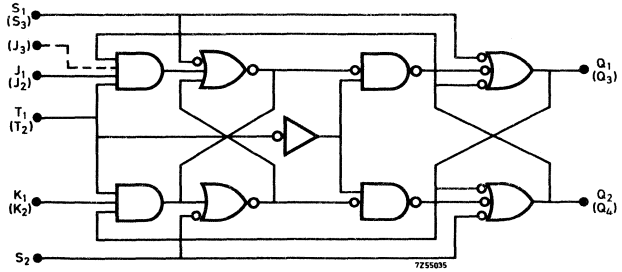
The FCJ191 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, e.g. rise and fall times of all input signals including the trigger signal are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 16 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1, S_2 and S_3 should be HIGH or floating.

For the flip-flop with two J-inputs is $J = J_2 \cdot J_3$ for positive logic

2. Set or reset via S terminals

S_1 S_3	S_2 S_2	Q_1 Q_3	Q_2 Q_4
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

1) For negative output voltage in LOW state.
2) At this limit input voltage typ. : −1.5 V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS2}	⩾	2	
	$N_{aS1} = N_{aS3}$	⩾	4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_{S2}	typ.	16	pF
	$C_{S1} = C_{S3}$	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	4.0 4.5	3.8 4.2	3.5 3.9	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{S2Lmax}$	5.7 6.6	5.5 6.3	5.2 5.8	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
	$-I_{S1Lmax}$ $-I_{S3Lmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{S2Hmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
	I_{S1Hmax} I_{S3Hmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	$V_{pd} = 1.5$ V N = 1; $C_L = 60$ pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	$V_{pd} = 1.5$ N = 8; $C_L = 60$ pF other output: N = 1; $C_L = 60$ pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

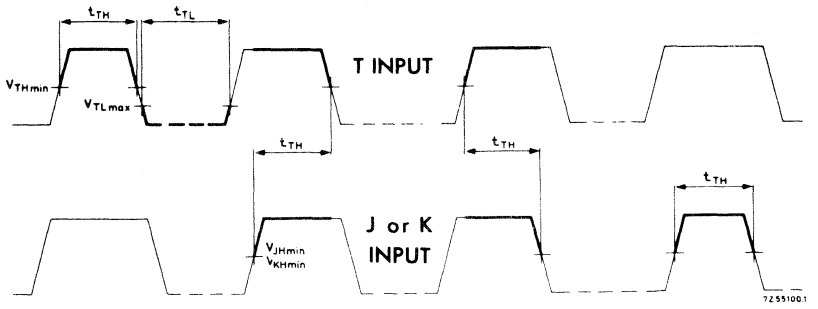


Fig. 1. Waveforms illustrating conditions for change of state.

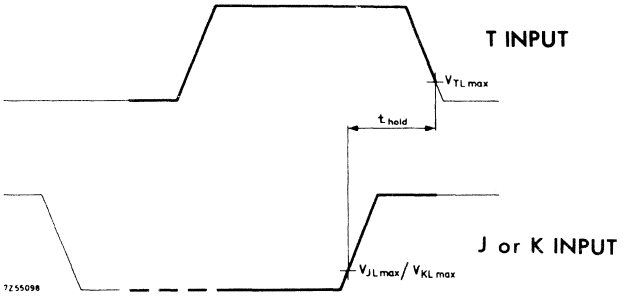


Fig. 2. Waveforms illustrating conditions for no change of state.

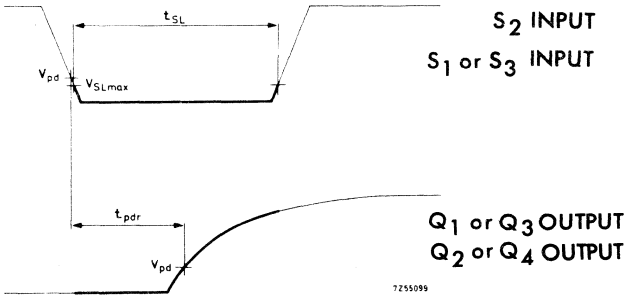
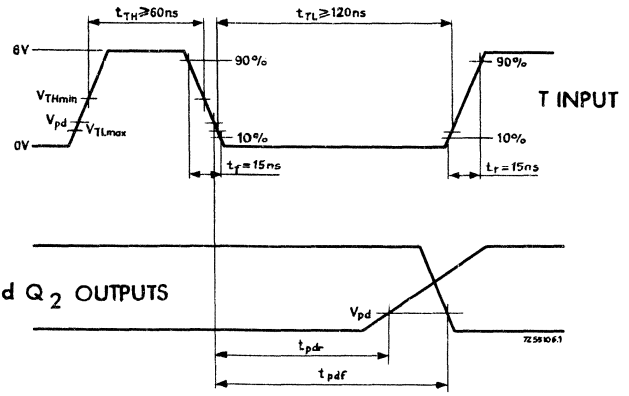
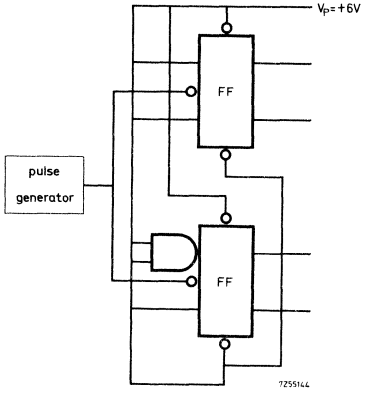


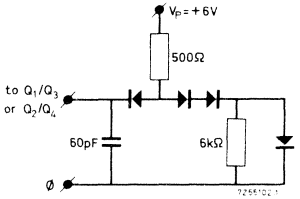
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

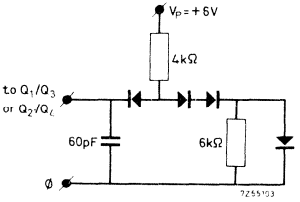
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and C_L[1]) = 60 pF



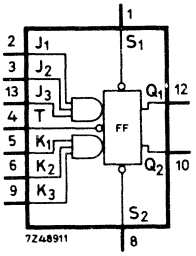
Diodes FCY101
Equivalent load for N = 1 and C_L[1]) = 60 pF

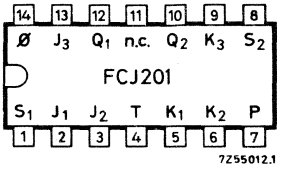
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



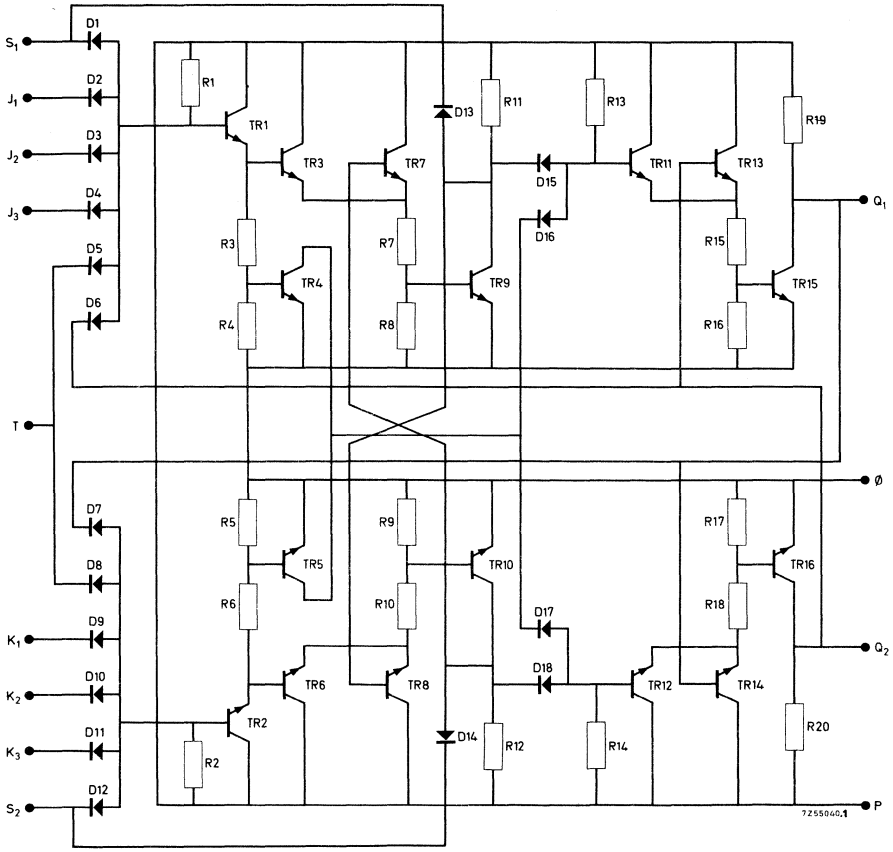


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 5	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 67	mW

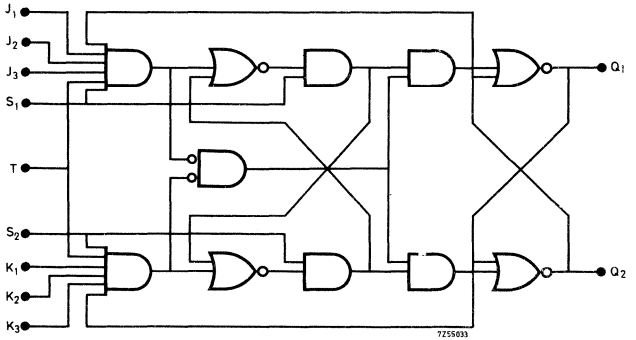
The FCJ201 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 and S_2 should be HIGH or floating.

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$ (for positive logic)

2. Trigger action via J and K terminals

J	K	Q_1	Q_2
H→L	X	H	L
X	H→L	L	H
H→L	H→L	reversed	

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$ (for positive logic)

If J or K go LOW with T HIGH, Q_1 and Q_2 assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q_1 and Q_2 are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K. S_1 and S_2 should be HIGH or floating.

3. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	indeterminate	
H	H	no change	

The set inputs override the other inputs and directly determine the output of the flip-flop.
In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage.
3) At this limit input voltage type.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	4	
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	5	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.5	V
	M_H	min.	1.9	V
to J or K input	M_L	min.	0.9	V
	M_H	min.	1.9	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	2.3	V
Average propagation delay time	t_{pd}	max.	150	ns
Maximum clock rate	f_c	⩾	3	MHz
Equivalent input capacitances				
for T input	C_T	typ.	8	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	11.2	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	110	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.4	5.3	V	5.7	$I_Q = 0$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.9	3.5	2.8	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	350	450	550	μA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	3.5 4.0	3.3 3.8	3.1 3.6	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{SLmax}$	2.7 3.0	2.6 2.9	2.4 2.7	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	20	–	mA	6.3	J, K, S, T inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references		
		0	+25	+75	V_P (V)		fig.
DYNAMIC DATA					5.7 and 6.3		
Change of state							
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	3.1	2.9	2.5 V		HIGH level at T and J and/or K to be present simultaneously	1
T-input time HIGH to:	t_{THmin}	100	100	100 ns			1
Input voltage LOW	V_{TLmax}	1.3	1.1	0.9 V		$t_{TLmin} = t_{pdr}$	1
No change of state							
JK input voltage LOW	V_{JLmax} V_{KLmax}	1.8	1.6	1.3 V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection							
Hold time	$t_{holdmax}$	20	20	20 ns			2
Set or Reset							
S input voltage LOW	V_{SLmax}	1.2	1.0	0.8 V		active $t_{SLmin} = t_{pdr}$	3
S input voltage HIGH	V_{SHmin}	3.1	2.9	2.5 V		inactive	
DYNAMIC DATA							
Propagation delay times from T to Q							
Rise propagation delay time	t_{pdrmax}	-	200	- ns		$V_{pd} = 1.5$ V; N = 1; C_L = 60 pF other output N = 8; C_L = 56 pF	4
Fall propagation delay time	t_{pdfmax}	-	100	- ns		$V_{pd} = 1.5$ V; N = 8; C_L = 56 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

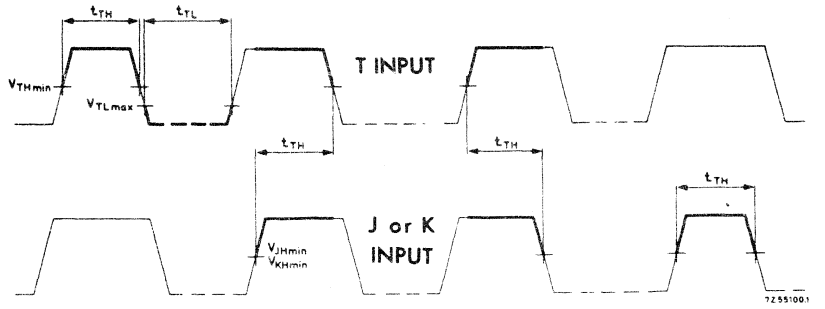


Fig. 1. Waveforms illustrating conditions for change of state.

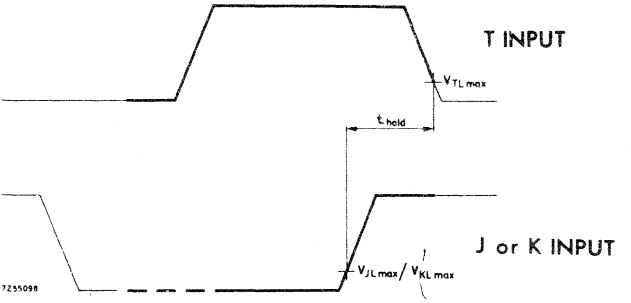


Fig. 2. Waveforms illustrating conditions for no change of state.

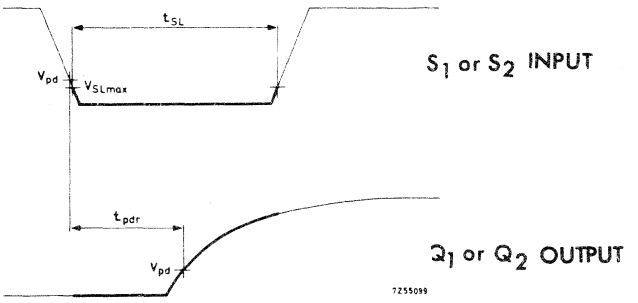
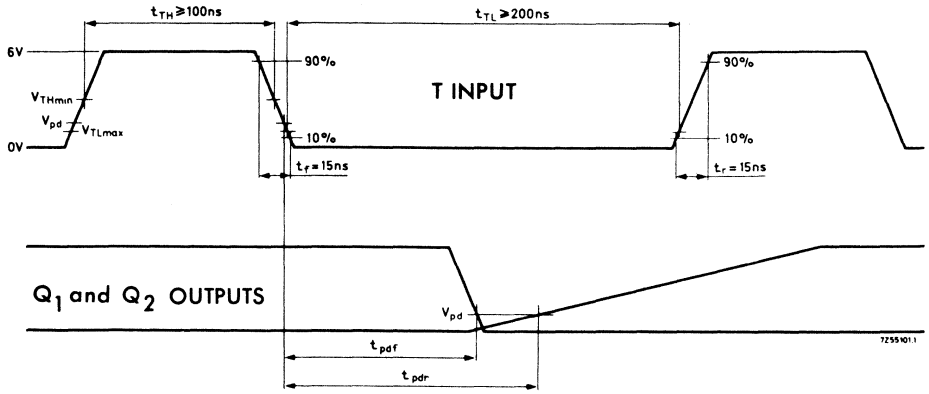
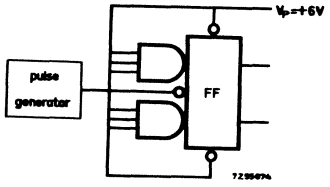


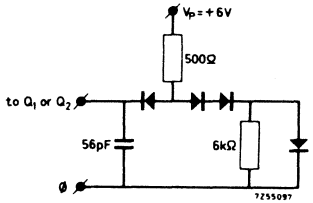
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

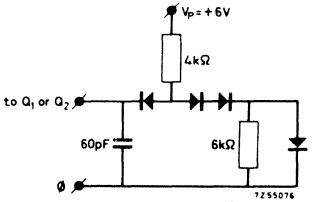






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 56 pF



diodes FCY101

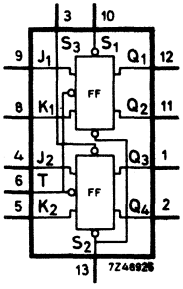
Equivalent load for N = 1 and C_L[1]) = 60 pF

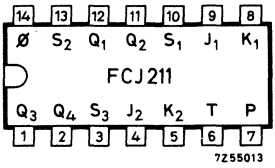
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER SLAVE FLIP-FLOP



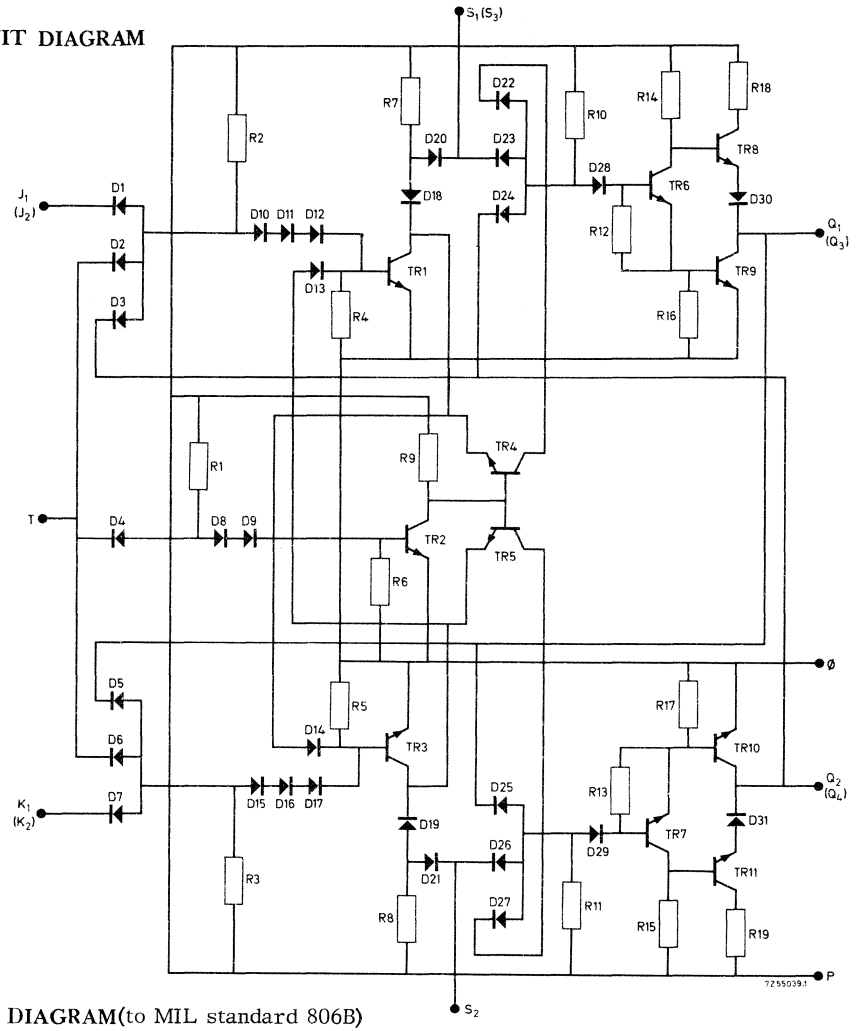


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

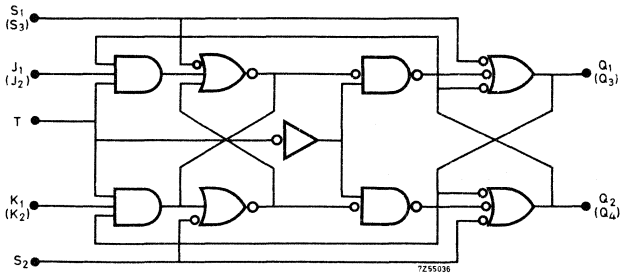
The FCJ211 comprises two independent direct-coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including trigger signals, are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include synchronous counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1, S_2 and S_3 should be HIGH or floating.

2. Set or reset via S terminals

S_1 S_3	S_2 S_4	Q_1 Q_3	Q_2 Q_4
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) For negative output voltage in LOW state.
2) At this limit input voltage typ. −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	1	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS2}		2	
	$N_{aS1} = N_{aS3}$		4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	24	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_{S2}	typ.	16	pF
	$C_{S1} = C_{S3}$	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	I_Q = −100 μA
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	8.0 9.0	7.6 8.4	7.0 7.8	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{S2Lmax}$	5.7 6.6	5.5 6.3	5.2 5.8	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
	$-I_{S1Lmax}$, $-I_{S3Lmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	6	6	150	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{S2Hmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
	$-I_{S1Hmax}$ $-I_{S3Hmax}$	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	$V_{pd} = 1.5$ V N = 1; $C_L = 60$ pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	$V_{pd} = 1.5$ N = 8; $C_L = 60$ pF other output: N = 1; $C_L = 60$ pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

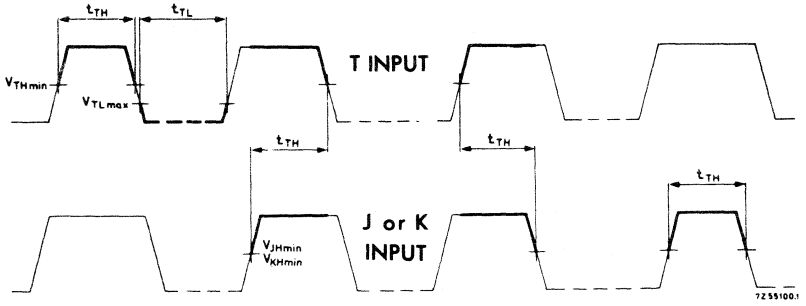


Fig. 1. Waveforms illustrating conditions for change of state.

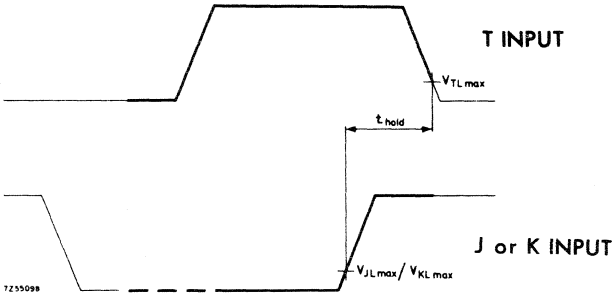


Fig. 2. Waveforms illustrating conditions for no change of state.

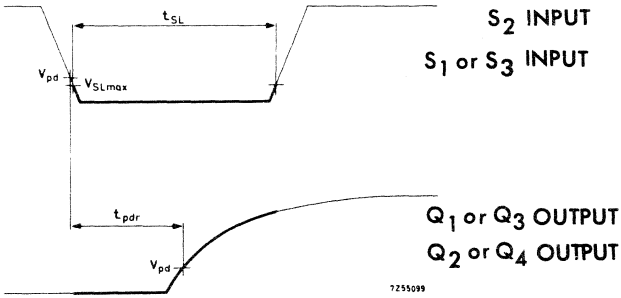
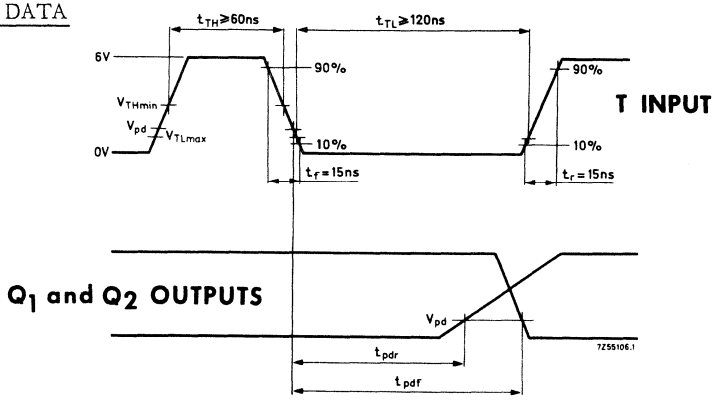
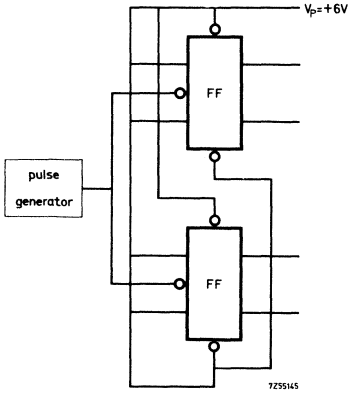


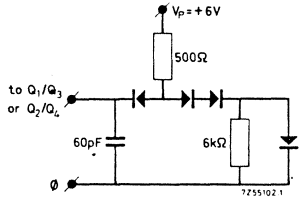
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

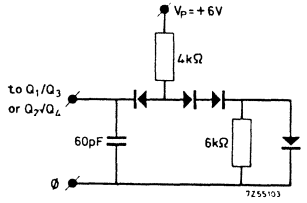
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and C_L[1]) = 60 pF



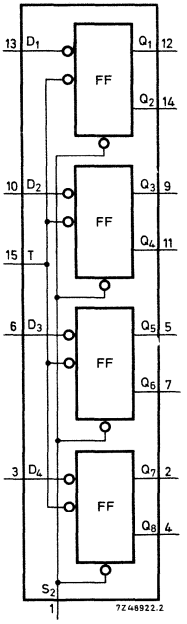
Diodes FCY101
Equivalent load for N = 1 and C_L[1]) = 60 pF

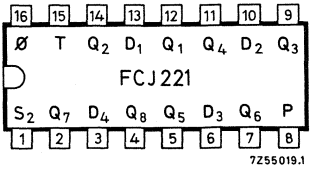
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

QUADRUPLE LATCH FLIP-FLOP



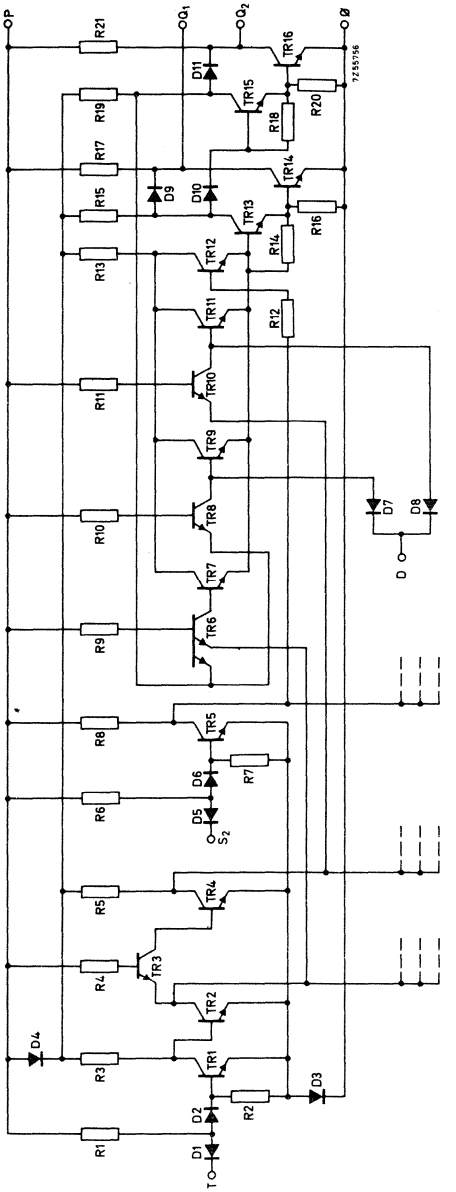


PACKAGE OUTLINE
16 lead plastic dual in-line (type A)
See General Section

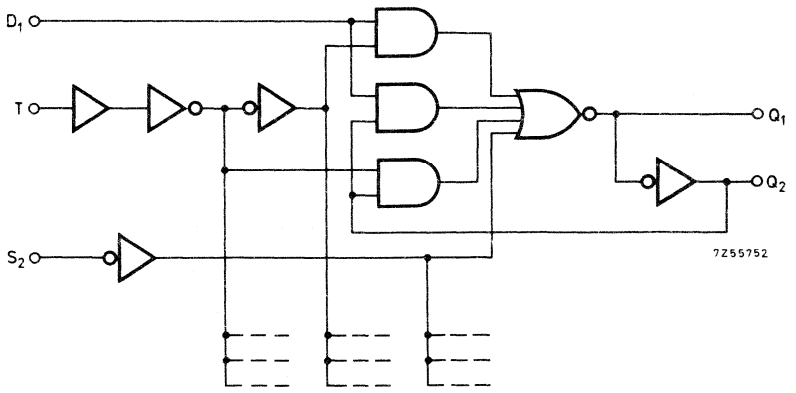
QUICK REFERENCE DATA				
Supply voltage	V_P	6.0	±5%	V
Operating ambient temperature range	T_{amb}	0 to	+75	°C
Clock rate at T_{amb} = 25 °C	f_c	typ.	5	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	≥	10	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	250	mW

The FCJ221 is a quadruple latch flip-flop with D inputs, a common clock (T) and a reset input (S_2).
A LOW input signal at D arrives after the last T signal goes HIGH at output Q_1.
The information follows after a LOW signal at the T input.
It is possible to influence the output state of the flip-flop.

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

Function tables

t_n	t_{n+1}
D	Q_1
H	L
L	H

S2	Q_1
H	H
L	X

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after trigger pulse
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at $T_{amb} < 40\ ^oC$	V_P	max.	8	V
Output voltage	V_Q	max.	8	V
Input voltage	V_G	max.	8	V
Input current	$-I_D$; $-I_T$; $-I_{S2}$	max.	20	mA [1]
Storage temperature	T_{stg}	−55 to	+125	^oC
Operating ambient temperature	T_{amb}	0	+75	^oC

[1]) At negative input voltage

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+75	°C
Uniform system supply voltage	V_P	5.7 to	6.3	V
Available d.c. fan-out	N_a	≥	10	
D.C. noise margin to D input	M_{DL}	min.	0.2	V
	M_{DH}	min.	3.0	V
to T, S_2 input	M_{TL}; M_{S2L}	min.	0.3	V
	M_{TH}; M_{S2H}	min.	3.1	V
Supply current	I_{Pav}	max.	47	mA[1])
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	300	mW

[1]) Input open and V_D = 0 V

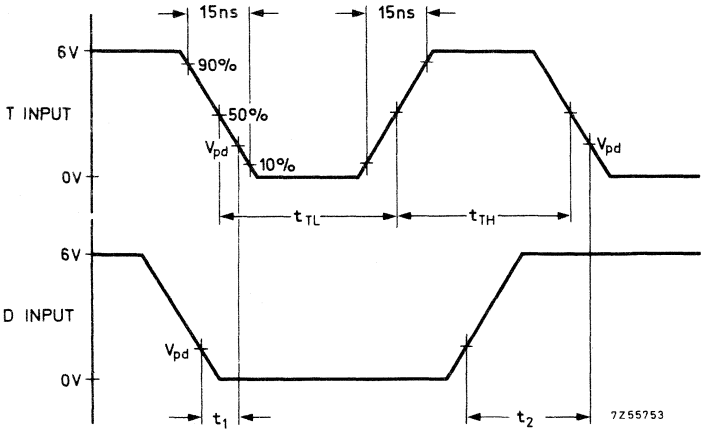
CHARACTERISTICS

STATIC DATA		T_{amb} (°C)				Conditions and references	
		0	25	75		V_P (V)	
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at:							
Output current LOW	I_{QLmax}	17.5 20.0	16.5 19.0	15.5 18.0	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	$-I_Q = 0$
Input voltage LOW							
D	V_{DLmax}	0.9	0.8	0.6	V	5.7 and 6.3	
T; S_2	V_{TLmax} V_{S2Lmax}	1.0	0.9	0.7	V	5.7 and 6.3	
Input voltage HIGH							
D	V_{DHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
T; S_2	V_{THmin} V_{S2Hmin}	2.2	2.1	2.0	V	5.7 and 6.3	
Input current LOW							
D	$-I_{DLmax}$	2.55	2.5	2.45	mA	5.7	$V_D = 0.4$ V
T; S_2	$-I_{TLmax}$ $-I_{S2Lmax}$	1.75	1.65	1.55	mA	5.7	$V_T = V_{S2} = 0.4$ V
D	$-I_{DLmax}$	2.85	2.8	2.75	mA	6.3	$V_D = 0.4$ V
T; S_2	$-I_{TLmax}$ $-I_{S2Lmax}$	2.0	1.9	1.8	mA	6.3	$V_T = V_{S2} = 0.4$ V
Input current HIGH							
D	I_{DHmax}	2	2	50	µA	6.3	$V_D = V_P$
T; S_2	I_{THmax} I_{S2Hmax}	1	1	25	µA	6.3	$V_T = V_{S2} = V_P$
Output current changing output state							
Q_1	$-I_{Q1max}$	4.2	4.05	3.75	mA	6.3	$V_Q = 0.4$ V
Q_2	$-I_{Q2max}$	6.3	6.1	5.65	mA	6.3	$V_Q = 0.4$ V
Supply current	I_{Pmax}	–	–	47	mA	6.3	$V_D = 0$ V; T and S_2 inputs open

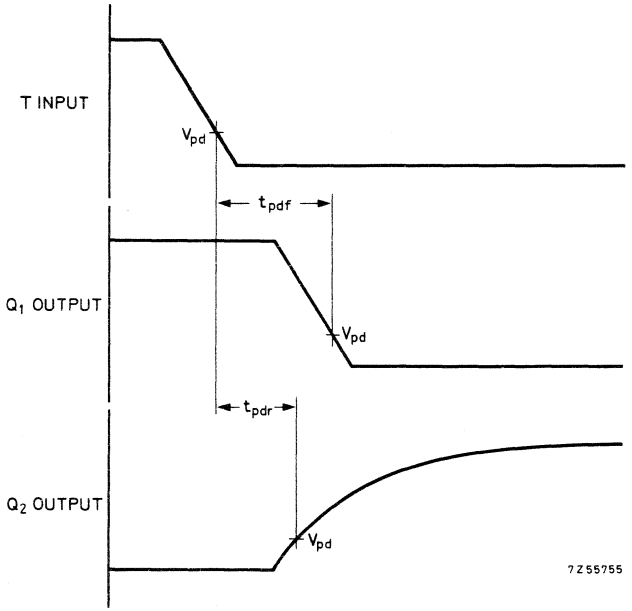
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	75		V_P (V)	
STATIC DATA							
D.C. noise margin							
LOW: D	M_{DLmin}	0.5	0.4	0.2	V		
T; S_2	M_{TLmin} / M_{S2Lmin}	0.6	0.5	0.3	V		
HIGH: D	M_{DHmin}	3.0	3.1	3.2	V		
T; S_2	M_{THmin} / M_{S2Hmin}	3.1	3.2	3.3	V		
DYNAMIC DATA							
Input time LOW							
T	t_{TLmin}	–	100	–	ns	5.7 and 6.3	
Input time HIGH							
T	t_{THmin}	–	70	–	ns	5.7 and 6.3	
Input time LOW							
S_2	t_{S2Lmin}	–	100	–	ns	5.7 and 6.3	
S_2 (changing output state)	t_{S2Lmin}	–	100	–	ns	5.7 and 6.3	
Set-up times:							
t_1	t_{su1min}	–	0	–	ns	5.7 and 6.3	
t_2	t_{su2min}	–	30	–	ns		
Propagation delay times:							
Rise propagation delay times							
$T \rightarrow Q_1$	t_{pdrmax}	–	95	–	ns	6.0	N = 1; C_L = 40 pF; V_{pd} = 1.5 V
$T \rightarrow Q_2$	t_{pdrmax}	–	105	–	ns	6.0	
$S_2 \rightarrow Q_2$	t_{pdrmax}	–	85	–	ns	6.0	
Fall propagation delay times							
$T \rightarrow Q_1$	t_{pdfmax}	–	60	–	ns	6.0	N = 8; C_L = 70 pF; V_{pd} = 1.5 V
$T \rightarrow Q_2$	t_{pdfmax}	–	120	–	ns	6.0	
$S_2 \rightarrow Q_2$	t_{pdfmax}	–	60	–	ns	6.0	

CHARACTERISTICS (continued)

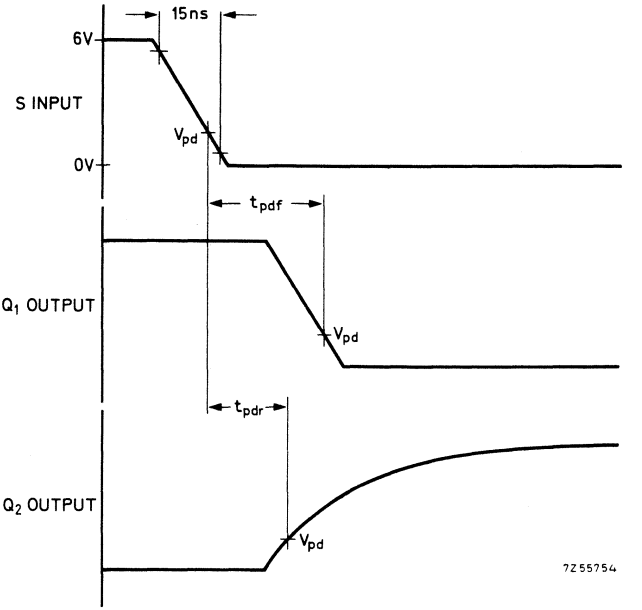


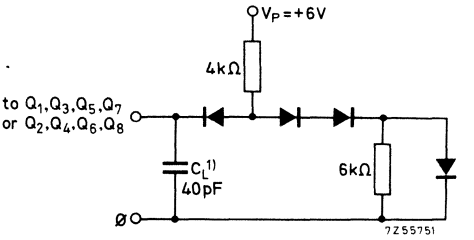
Waveform illustrating conditions for change of state



Waveforms illustrating t_{pdr} and t_{pdf}

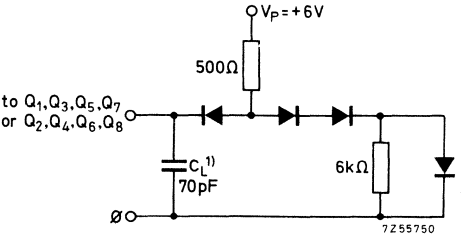
CHARACTERISTICS (continued)





diodes FCY101

N = 1



diodes FCY101

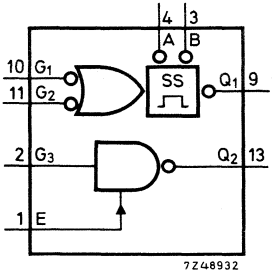
N = 8

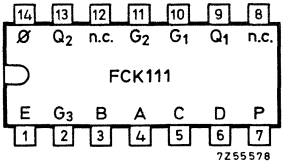
Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

1) Including jig and probe capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

MONOSTABLE MULTIVIBRATOR





QUICK REFERENCE DATA				
Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to +75	°C
Propagation delay time $G_1 \rightarrow Q_1$	t_{pdf}	typ.	70	ns
T_{amb} = 25 °C at V_{pd} = 1.5 V $G_3 \rightarrow Q_2$	t_{pdf}	typ.	40	ns
Output pulse width:				
R_t = 10 kΩ ± 1%; C_t = 160pF ± 1%	t_{Q1L}	typ.	1.0	µs
Available d.c. fan-out Q_1	N_a	≥	14	
T_{amb} = 0 to +75 °C Q_2	N_a	≥	14	
A	N_a	=	1	
D.C. noise margin				
T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption				
50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	58	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

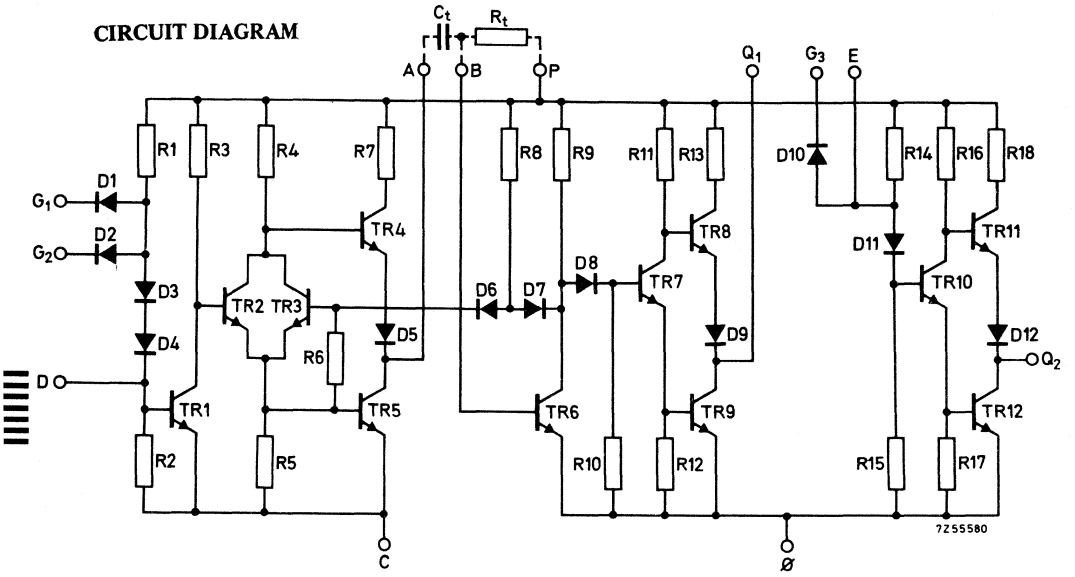
The FCK111 comprises a threshold triggered monostable circuit and an independent expandable inverter.

The monostable function is obtained by an externally connected resistor and capacitor. Each time one of the inputs G_1 or G_2 is going LOW a negative going pulse appears at output Q_1.

The pulse width is adjustable over a very wide range by varying the resistor and capacitor values.

If the input (G_3) of the inverter is connected to A a positive going pulse is obtained at the output Q_2, almost coinciding and practically having the same width as the output pulse Q1, provided that the width of the input pulse does not exceed the width of the output pulse. The outputs Q_1 and Q_2 are bi-directional and have a high fan-out drive capability.

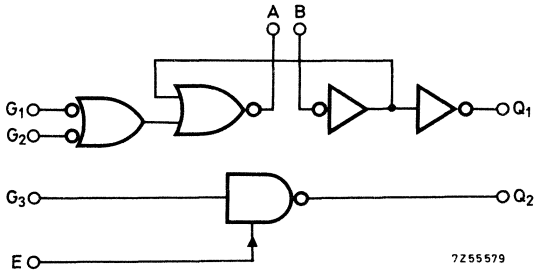
CIRCUIT DIAGRAM



Notes

1. Terminals C and D make the circuit compatible with the FCK101.
2. To ensure conformity with the characteristics given in the data sheets, terminal C must be connected to terminal ϕ.
   If terminals C and ϕ are not interconnected, the output pulse can be shortened by connecting a diode or a voltage source to C (positive to ϕ); however, this will alter a number of characteristics, including special input levels and output level A.
3. The noise margin for a.c. disturbances at the trigger inputs G_1 and G_2 can be increased by connecting a capacitor between terminals C and D, but this reduces the minimum operating frequency.

LOGIC DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20.0	mA [1]
Input current	$-I_G$	max.	20.0	mA [2]
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages:				
– with respect to supply	V_P-V_E	max.	8.0	V
– with respect to other inputs	V_G-V_E	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C
Output short circuit duration (duty cycle 10%, either output, or both)	t_{Qsc}	max.	60	ms
Timing resistor (R_t connected to 6.3 V)	R_t	min.	5	kΩ
		max.	20	kΩ
Timing capacitor	C_t	max.	160	μF
		min.	30	pF [3]

[1]) for negative output voltage in LOW state.

[2]) at this limit, input voltage typ: − 1.5 V.

[3]) C_t min 30 pF is not a rating, but is to be considered as the minimum value at which the circuit still performs its function.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.5	V
Available d.c. fan-out Q_1	N_a	≥	14	
Available d.c. fan-out Q_2	N_a	≥	14	
Available d.c. fan-out A	N_a	=	1	
D.C. noise margin FCK111 → gate	M_L	min.	0.4	V
	M_H	min.	1.2	V
gate → FCK111	M_L	min.	0.4	V
	M_H	min.	1.8	V
Propagation delay time: $G_1 \rightarrow Q_1$	t_{pdf}	max.	170	ns
$G_1 \rightarrow Q_2$	t_{pdr}	max.	200	ns
$G_3 \rightarrow Q_2$	t_{pdr}	max.	120	ns
$G_3 \rightarrow Q_2$	t_{pdf}	max.	55	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50 %)	I_{Pav}	typ.	10.9	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	98	mW
Relative change of output pulse width vs supply voltage	see page 10			
Output pulse width vs timing capacitor (C_t)	see page 10			

CHARACTERISTICS : (pin C connected to pin ϕ)

STATIC DATA		T_{amb} (°C) 0	25	75	V_P (V)	Conditions and References
Output Q_1						
Output voltage LOW at:	V_{Q1L} max	0.4	0.4	0.4 V	5.7 and 6.3	V_B (pin 3) at 0 V
Output current LOW	I_{Q1L} max	25 28	27 27	26 mA 26 mA	5.7 6.3	
Output voltage HIGH	V_{Q1H}min	3.5 2.6	3.7 2.8	4.0 V 2.9 V	5.7 5.7	$-I_{Q1H}$ = 30 µA $-I_{Q1H}$ = 5 mA } and B (pin 3) connected to V_P via 20 kΩ (± 1 %)
Output short circuit current	$-I_{Q1sc}$ min	16.5	19.5	18.0 mA	5.7	B (pin 3) connected to V_P via 20 kΩ (± 1 %) (max. duration 60 ms; duty cycle 10 %)
Output Q_2						
Output voltage LOW at:	V_{Q2L} max	0.4	0.4	0.4 V	5.7 and 6.3	
Output current LOW	I_{Q2L} max	25 28	27 27	26 mA 26 mA	5.7 6.3	
and Input voltage HIGH G_3	V_{GH} min	2.3	2.2	2.1 V	5.7 and 6.3	
Output voltage HIGH at:	V_{Q2H} min	3.5 2.6	3.7 2.8	4.0 V 2.9 V	5.7 5.7	$-I_{Q2H}$ = 30 µA $-I_{Q2H}$ = 5 mA
Input voltage LOW G_3	V_{GL} max	1.0	1.0	0.8 V	5.7 and 6.3	
Output short circuit current	$-I_{Q2sc}$ min	16.5	19.5	18.0 mA	5.7	V_{GL} max (max. duration 60 ms; duty cycle 10 %)

CHARACTERISTICS (continued)

STATIC DATA (continued)		T_{amb} (°C) 0	25	75	Conditions and references V_P (V)	
Output A						
Output voltage LOW	V_{AL} max	0.4	0.4	0.4 V	5.7 and 6.3	
at:						
Output current LOW	I_{AL} max	2.0	2.0	2.0 mA	5.7 and 6.3	see note
and Input voltage LOW; G_1, G_2 or V_B (pin 3) at 0 V	V_{GL} max	1.0	1.0	0.8 V	5.7 and 6.3	
Output voltage HIGH	V_{AH} min	3.9	4.0	4.1 V	5.7	$-I_{AH}$ = 30 µA
		3.2	3.4	3.4 V	5.7	$-I_{AH}$ = 5 mA
at: Input voltage HIGH	V_{GH} min	2.3	2.2	2.1 V	5.7 and 6.3	
or: B (pin 3) connected to V_P via 20 kΩ (± 1%)						
Output short circuit current	$-I_{Asc}$ min	30	30	25 mA	5.7	B (pin 3) connected to V_P via 20 kΩ (± 1%) (max. duration 60 ms; duty cycle 10%)

Note

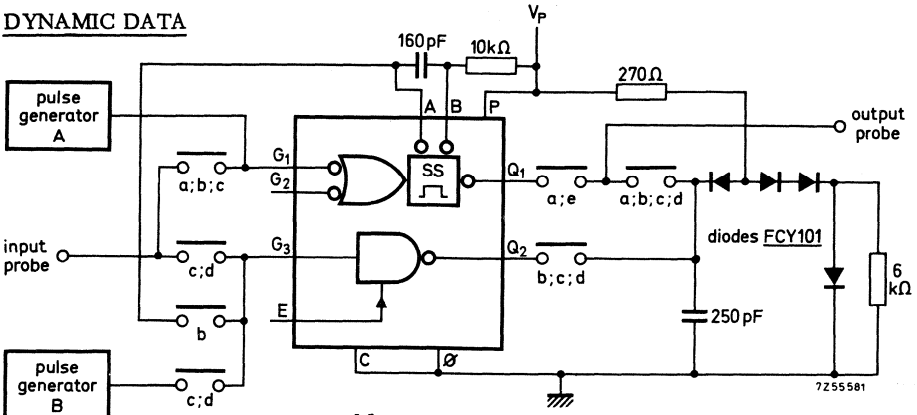
I_{AL} max is an extra static current, which can be applied to output A under both static and dynamic conditions without dusturbing the output pulse width.

CHARACTERISTICS (continued)

STATIC DATA (continued)		T_{amb} (°C) 0	25	75		V_P (V)	Conditions and references
Input current LOW	$-I_{GL}$ max	1.75	1.65	1.85	mA	5.7	V_G = 0.4 V; other inputs
		2.00	1.90	1.80	mA	6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GH} max	1.0	1.0	25.0	µA	5.7	V_G = 5.3 V, other inputs at V_G = 0 V
Supply current (unloaded)							current flow in R_t not included
output Q_1 HIGH } output Q_2 LOW }	I_{PH} typ	8.3	8.0	7.5	mA	6.0	
output Q_1 LOW } output Q_2 LOW }	I_{PL} typ	13.5	11.3	10.3	mA	6.0	
	I_{PL} max	17.3	16.6	15.6	mA	6.3	
Average supply current	I_{Pav}	14.7	14.1	13.2	mA	6.3	duty cycle 50 %
DYNAMIC DATA							
Propagation delay times							
Rise : $G_1 \rightarrow Q_2$	t_{pdr} max	170	150	200	ns	6.0	V_{pd} = 1.5 V; N = 15; C_L = 250 pF; $t_f = t_r$ = 15 ns
$G_3 \rightarrow Q_2$	t_{pdr} max	80	85	120	ns	6.0	
Fall : $G_1 \rightarrow Q_1$	t_{pdf} max	170	130	170	ns	6.0	
$G_3 \rightarrow Q_2$	t_{pdf} max	55	50	55	ns	6.0	
Pulse width	t_{Q1L}max		1.10		µs	6.0	R_t = 10 kΩ ± 1 %; C_t = 160 pF ± 1 %
	t_{Q1L}typ		1.00		µs	6.0	
	t_{Q1L}min		0.90		µs	6.0	
Duration input LOW	t_{GL} min	30	30	40	ns	5.7 and 6.3	

CHARACTERISTICS (continued)

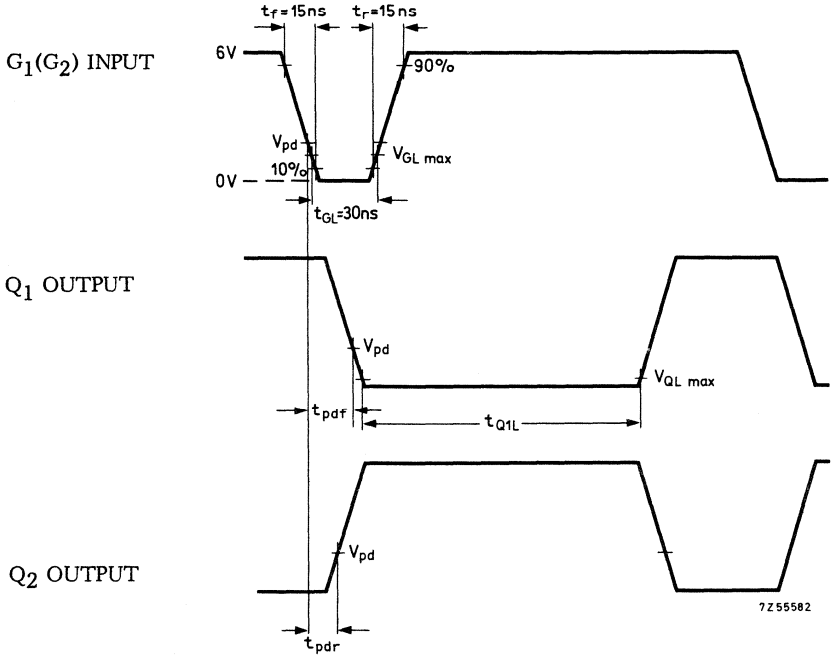
DYNAMIC DATA



Measurement set-up

a = t_{pdf} : $G_1 \rightarrow Q_1$ c = t_{pdf} : $G_3 \rightarrow Q_2$ e = t_{Q1L}

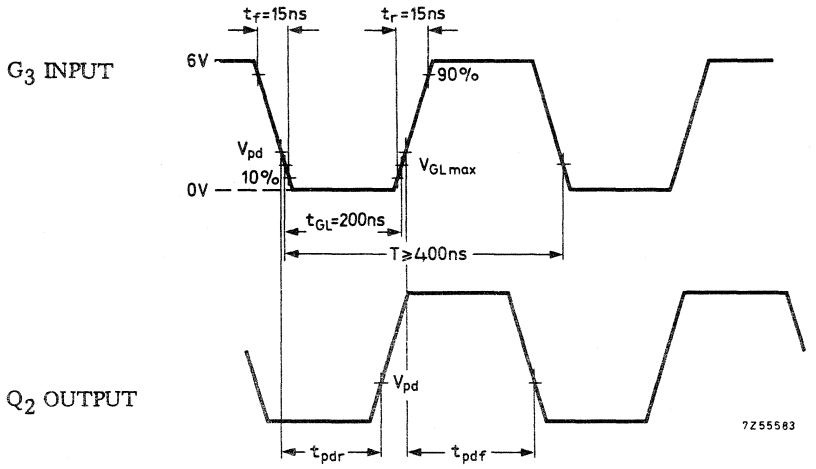
b = t_{pdr} ; $G_1 \rightarrow Q_2$ d = t_{pdr} ; $G_3 \rightarrow Q_2$



Waveform illustrating measurement of t_{pdr}, t_{pdf}, t_{GL} and t_{Q1L} for A pulse generator.

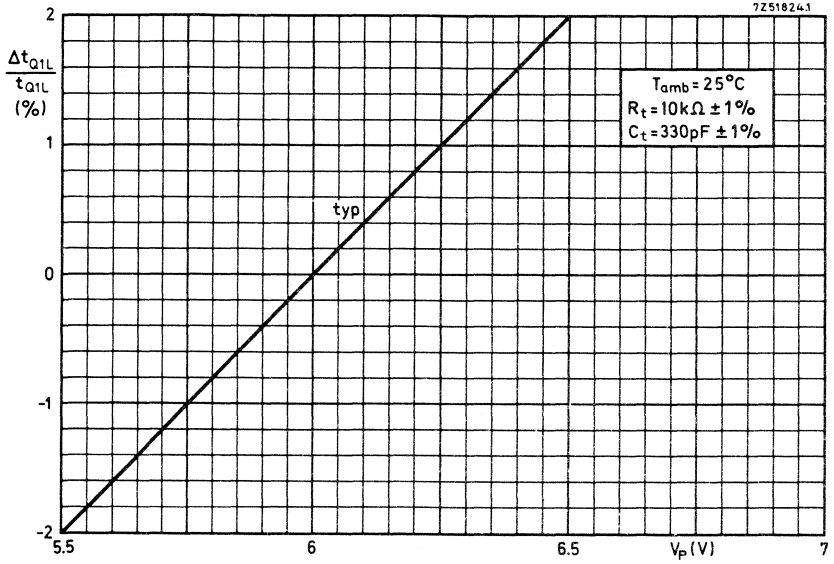
CHARACTERISTICS (continued)

DYNAMIC DATA

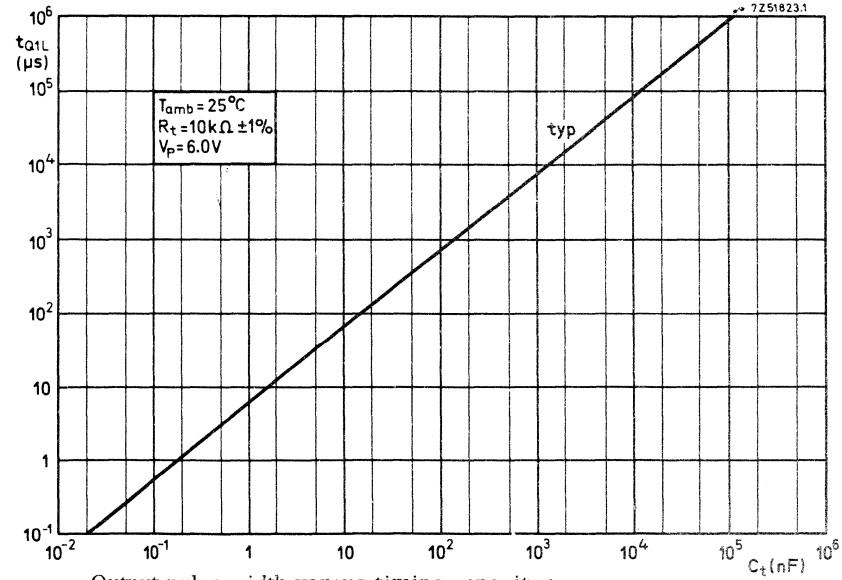


Waveforms illustrating measurement of t_{pdr}, t_{pdf} and t_{GL} for B pulse generator.

CHARACTERISTICS (continued)



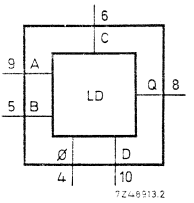
Relative change of output pulse width versus supply voltage.

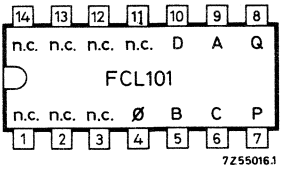


Output pulse width versus timing capacitor.

The FC family of DTL silicon monolithic integrated circuit has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

LEVEL DETECTOR



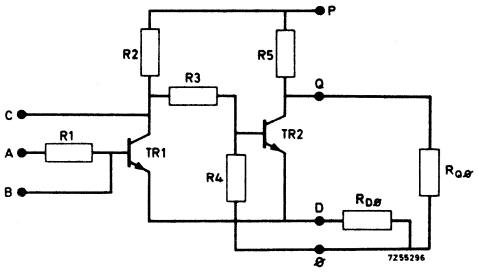


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Input hysteresis voltage $R_{D\emptyset}$ = 100 Ω, T_{amb} = 25 °C	ΔV_{At}	min. 60 max. 200	mV mV
Available output current $R_{D\emptyset}$ = 100 Ω, T_{amb} = 25 °C	I_{QL}	2.7	mA
Operating frequency T_{amb} = 25 °C	f	typ. 5	MHz
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 12	mW

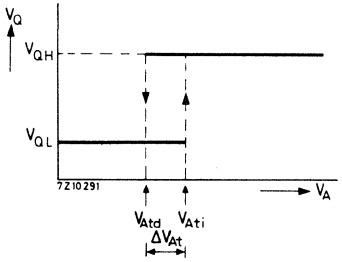
The FCL101 is a non-inverting Schmitt-trigger circuit. Tripping levels are set by an external resistor or zener diode.
Typical applications are discrimination, restoration, level shifting and pulse-shaping (squaring).

PACKAGE OUTLINE 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



VOLTAGE TRANSFER CURVE



Letter symbols:

$R_{Q\emptyset}$ = external resistor between Q and $\emptyset$

$R_{D\emptyset}$ = external resistor between D and $\emptyset$

V_Q = short for $V_{Q\emptyset}$ = voltage at Q with respect to $\emptyset$, the common reference and supply return terminal

V_{Ati} = tripping level for increasing input voltage V_A (short for $V_{A\emptyset}$)

V_{Atd} = tripping level for decreasing input voltage V_A

$\Delta V_{At} = V_{Ati} - V_{Atd}$ = input hysteresis voltage.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_A	max.	8.0	V
with respect to supply voltage	$V_A - V_P$	max.	2.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_A$	max.	0.5	mA
Other terminals	I_B	max.	5	mA
	V_C	max.	5.0	V
	V_D	max.	5.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+75	°C
Uniform system supply voltage	V_P	5.7 to	6.3	V
Output resistance	P_o	max.	7.6	kΩ
Supply current at T_{amb} = 25 °C, V_P = 6 V duty cycle 50%	I_{Pav}	typ.	2.0	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	27	mW

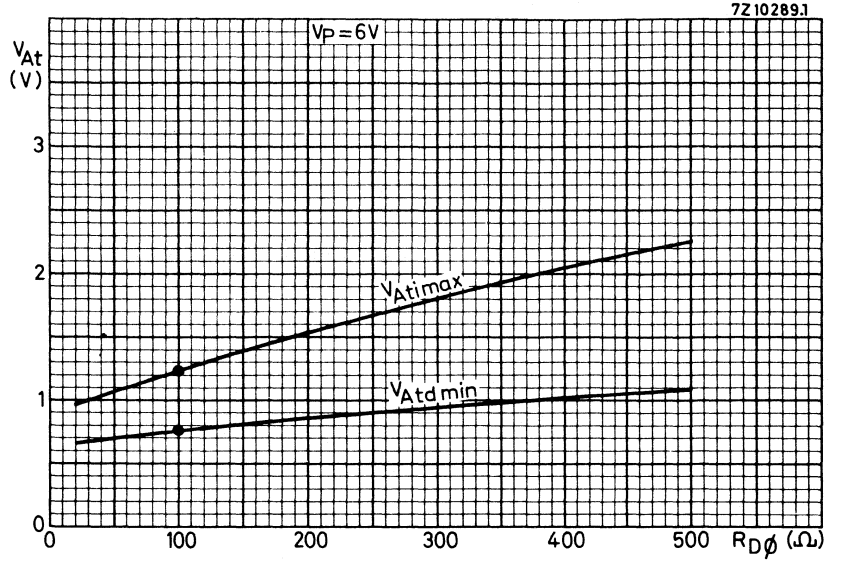
[1]) For negative output voltage.

[2]) Input voltage typ. −9 V when D grounded; no input current protection required for input voltages down to −5 V.

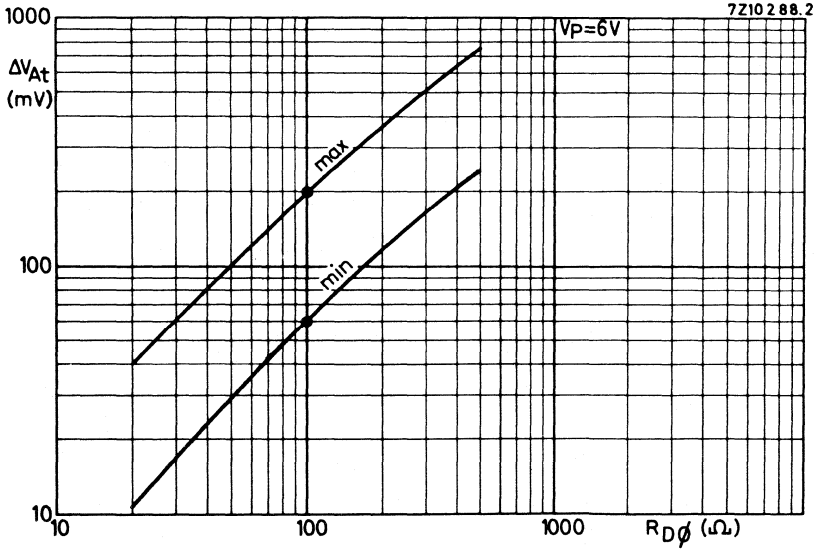
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		$V_{P(V)}$	$R_{D\emptyset(\Omega)}$	
STATIC DATA								
Tripping levels								
- input voltage increasing	V_{Atimax}	1.40	1.25	1.15	V	6.0	100 ± 1%	
- input voltage decreasing	V_{Atdmin}	0.75	0.75	0.60	V	6.0	100 ± 1%	
Input hysteresis voltage	ΔV_{Atmin}	60	60	50	mV	6.0	100 ± 1%	
	ΔV_{Atmax}	220	200	180	mV	6.0	100 ± 1%	
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	0	
at:								
Output current LOW	I_{QLmax}	10	10	7	mA			
and at:								
Input voltage LOW	V_{ALmax}	0.60	0.60	0.45	V			
Output voltage LOW	V_{QLmax}	0.8	0.8	0.8	V	5.7 and 6.3	100 ± 1%	$V_{ALmax} = V_{Atd\,min}$
at:								
Output current LOW	I_{QLmax}	2.5	2.9	1.9	mA	5.7		
		2.1	2.5	1.6	mA	6.3		
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	0	$I_Q = 0$
at:								
Input voltage HIGH	V_{AHmin}	0.95	0.90	0.80	V			
Input current HIGH	I_{AHmax}	2.2	2.0	2.0	mA	5.7 and 6.3	0	$V_A = 2\,V$
Input current HIGH	I_{AHmax}	1.2	1.1	1.2	mA	5.7 and 6.3	100 ± 1%	$V_A = 2\,V$
Output current LOW	$-I_{QLLmin}$	1.0	0.95	0.75	mA	5.7	0	$V_A = 2\,V$, V_Q externally forced to 0 V.
	$-I_{QLLmax}$	2.5	2.1	2.0	mA	6.3	0	
Supply current								
- output LOW	I_{PLmax}	4.2	3.7	3.5	mA	6.3	0	$V_A = 0\,V$
- output HIGH	I_{PHmax}	2.9	2.6	2.5	mA	6.3	0	$V_A = 2\,V$
DYNAMIC DATA								
Operating frequency	f_{min}	–	1	–	MHz	6.0	100 ± 1%	
	f_{typ}	–	5	–	MHz			

DESIGN CURVES at T_{amb} = 25 °C (dots indicate guaranteed values)

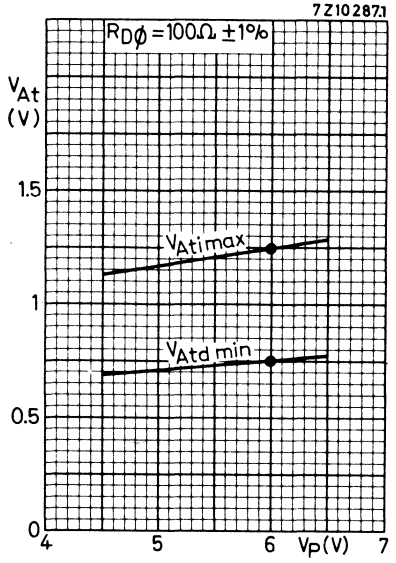


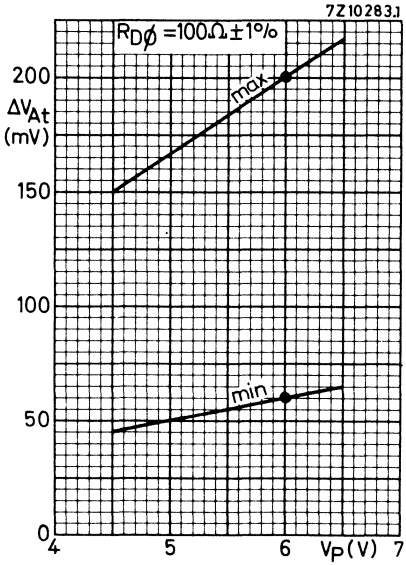
Input tripping levels versus feedback resistance



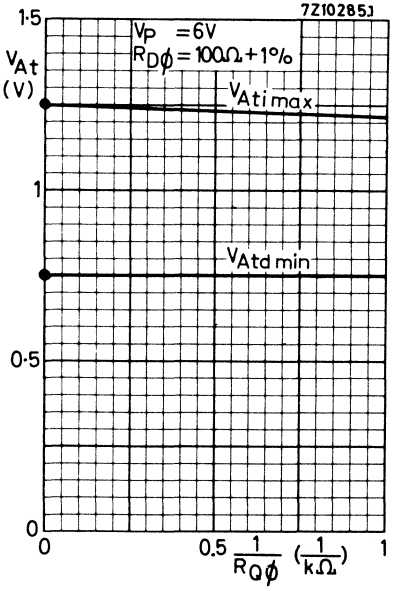
Input hysteresis voltage versus feedback resistance

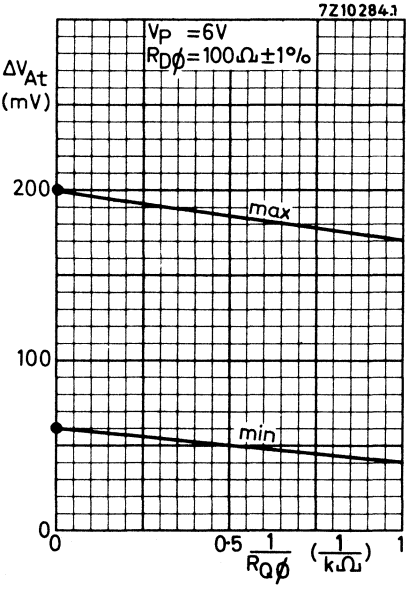
DESIGN CURVES (continued) at T_{amb} = 25 °C





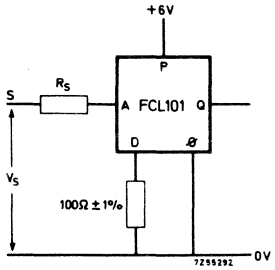
Input tripping levels and hysteresis voltage versus supply voltage



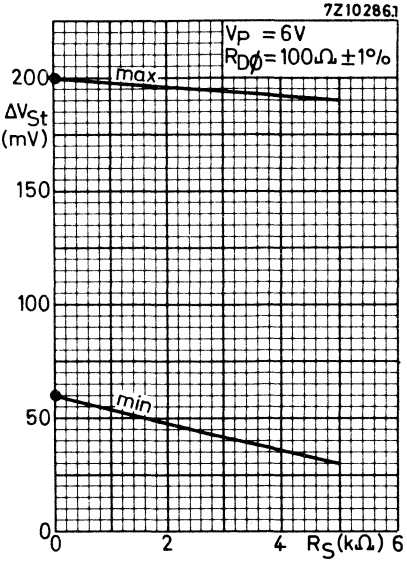


Input tripping levels and hysteresis voltage versus load conductance

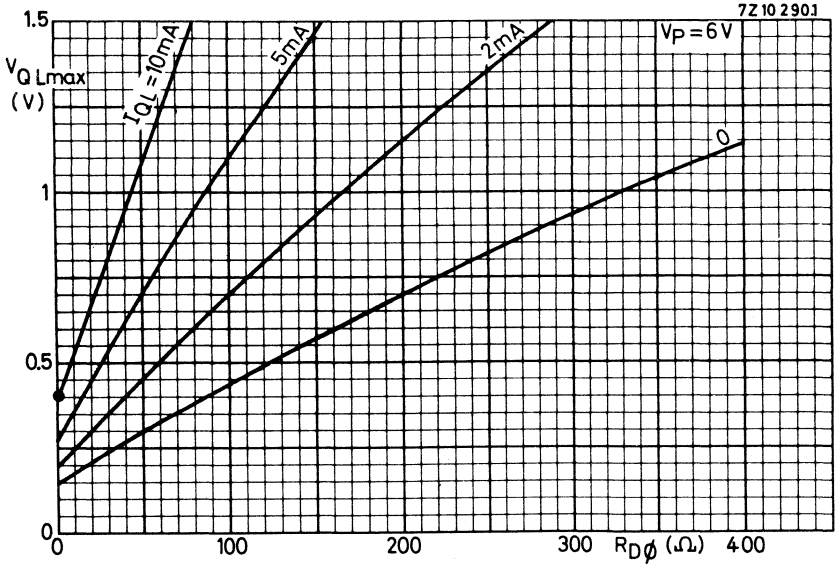
DESIGN CURVES (continued) at T_{amb} = 25 °C



ΔV_{St} = hysteresis at point S.



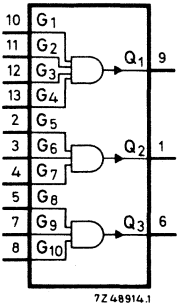
Hysteresis at signal source versus resistance

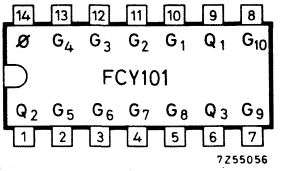


Low output voltage versus feedback resistance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

TRIPLE GATE EXPANDER





CHARACTERISTICS

		T_{amb} (°C)		
		25	75	
Reverse breakdown voltage at I_R = 50 μA	$V_{(BR)R}$	min. 8.0		V
Reverse leakage current at V_R = 8.0 V	I_R	max. 1.0	25	μA
Forward voltage at I_F = 2.0 mA	V_F	max. 1.0		V
Capacitance at V_R = 0; f = 1 MHz	C_d	max. 11		pF
Reverse recovery time at $I_F = I_R$ = 2.0 mA	t_{rr}	typ. 4		ns ←
		max. 11		ns ←

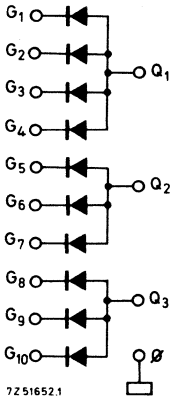
The FCY101 comprises three independent diode arrays. It is intended primarily for expanding the fan-in capability of those FCH gates that have an expansion input terminal.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Reverse voltage	V_R	max. 8.0	V
Forward current	I_F	max. 30	mA
Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature	T_{amb}	0 to +75	°C

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



T T L FJ family

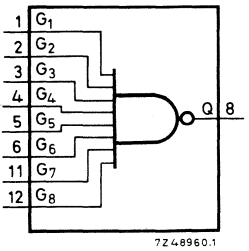
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

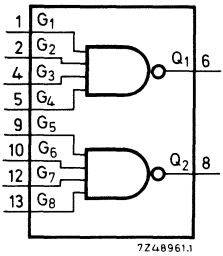
NAND GATES

In the standard temperature range the FJ family comprises the following NAND gates (positive logic):

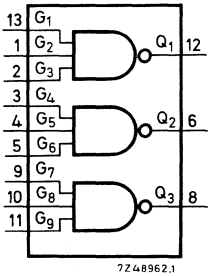
Single 8-input NAND gate	FJH101/7430
Dual 4-input NAND gate	FJH111/7420
Triple 3-input NAND gate	FJH121/7410
Quadruple 2-input NAND gate	FJH131/7400



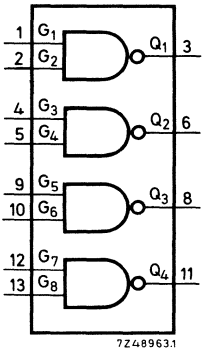
FJH101/7430



FJH111/7420



FJH121/7410



FJH131/7400

QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	10	mW

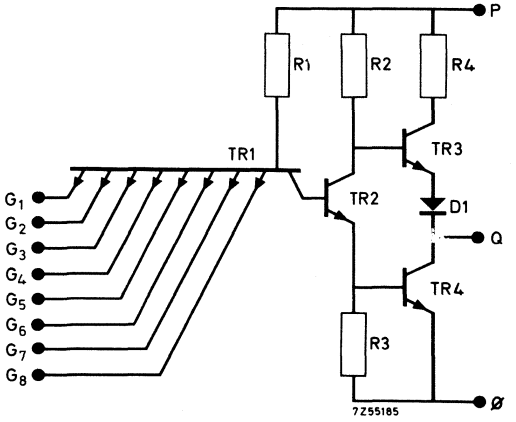
Each gate comprises a multi-emitter AND input gate followed by an inverting amplifier and a totem pole output stage.

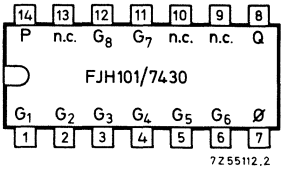
PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS

FJH101/7430

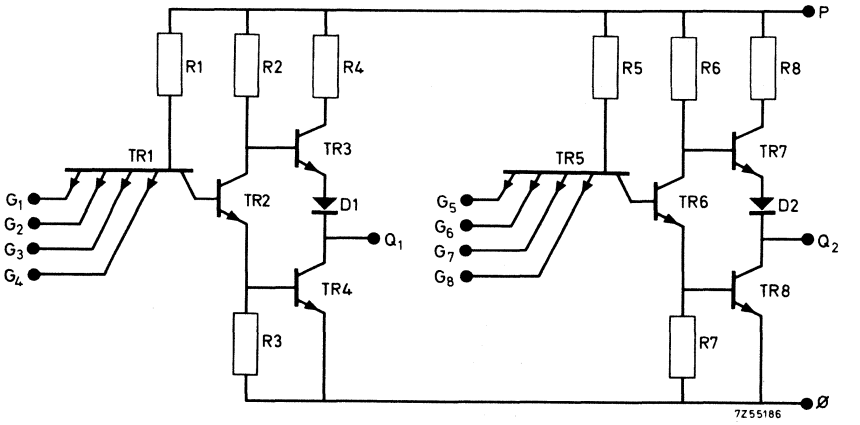
Single 8-input NAND gate

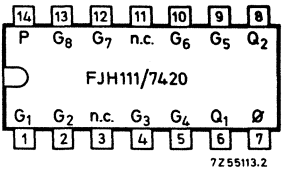




FJH111/7420

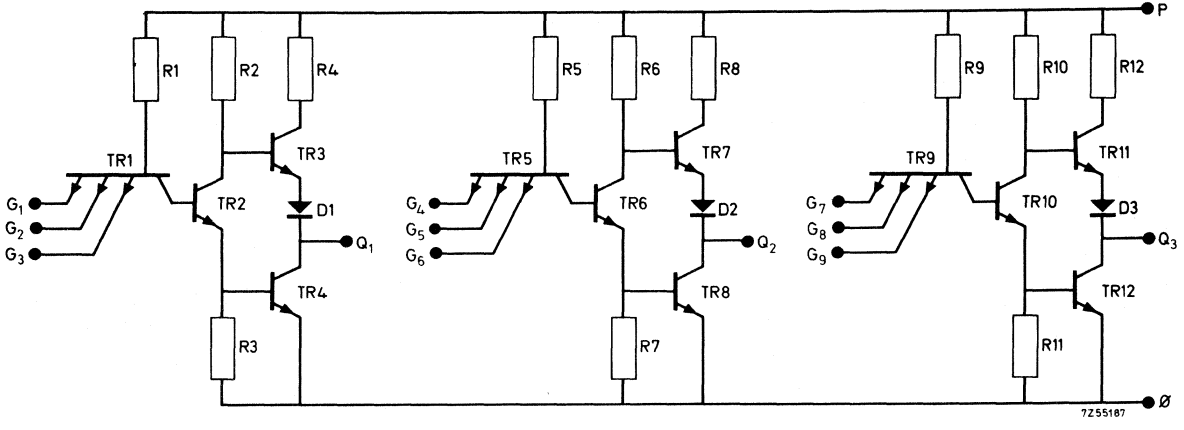
Dual 4-input NAND gate

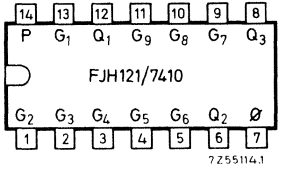




CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

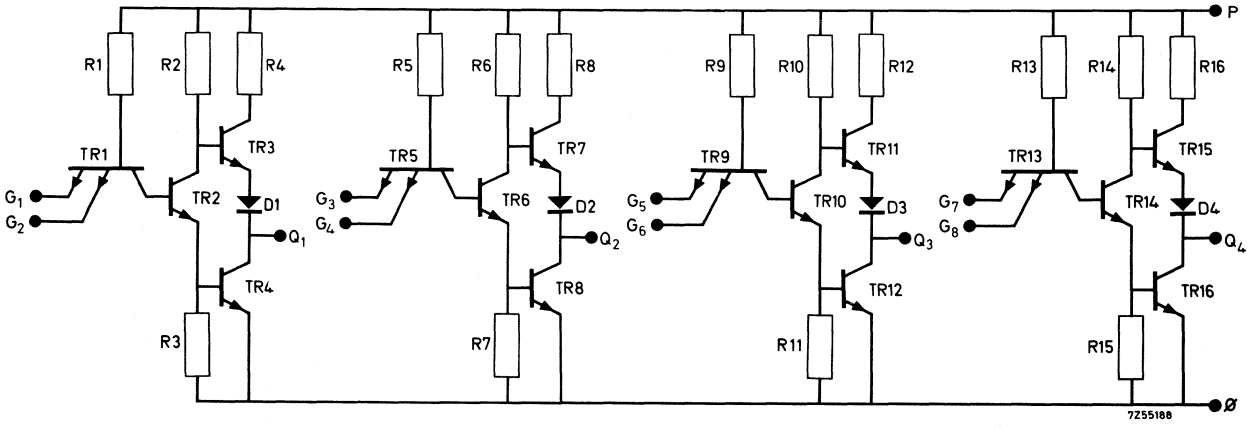
FJH121/7410
Triple 3-input NAND gate

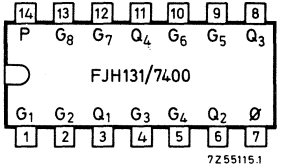




CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

FJH131/7400
Quadruple 2-input NAND gate





LOGIC FUNCTION

Individual gate operation

$C = \overline{A.B}$ positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Function table

A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	0 to	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+ 70	°C

[1] In addition the voltage difference between any two inputs max. 5.5 V

[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$; $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}	40	40	40	µA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short-circuited	$-I_{Qsc\ min}$ $-I_{Qsc\ max}$	18 55	18 55	18 55	mA mA	5.25	$V_Q=0$; $V_G=0$
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ. t_{pdr} <	-	13 22	-	ns ns	5.0	N=10
Fall propagation delay time	t_{pdf} typ. t_{pdf} <	-	8 15	-	ns ns	5.0	N=10

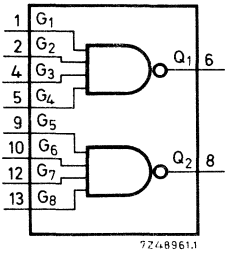
CHARACTERISTICS (continued)

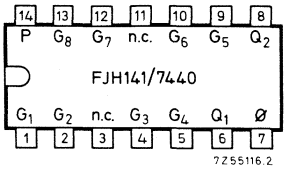
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
SUPPLY DATA						5.0	
Supply current							
Output LOW							
FJH101/7430	I_{PL} typ.	3	3	3	mA		V_G = 5.0 V; I_Q = 0
	I_{PL} <	6	6	6	mA		
FJH111/7420	I_{PL} typ.	6	6	6	mA		
	I_{PL} <	11	11	11	mA		
FJH121/7410	I_{PL} typ.	9	9	9	mA		
	I_{PL} <	16.5	16.5	16.5	mA		
FJH131/7400	I_{PL} typ.	12	12	12	mA		
	I_{PL} <	22	22	22	mA		
Output HIGH							
FJH101/7430	I_{PH} typ.	1	1	1	mA		V_G = 0; I_Q = 0
	I_{PH} <	2	2	2	mA		
FJH111/7420	I_{PH} typ.	2	2	2	mA		
	I_{PH} <	4	4	4	mA		
FJH121/7410	I_{PH} typ.	3	3	3	mA		
	I_{PH} <	6	6	6	mA		
FJH131/7400	I_{PH} typ.	4	4	4	mA		
	I_{PH} <	8	8	8	mA		

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL NAND POWER GATE



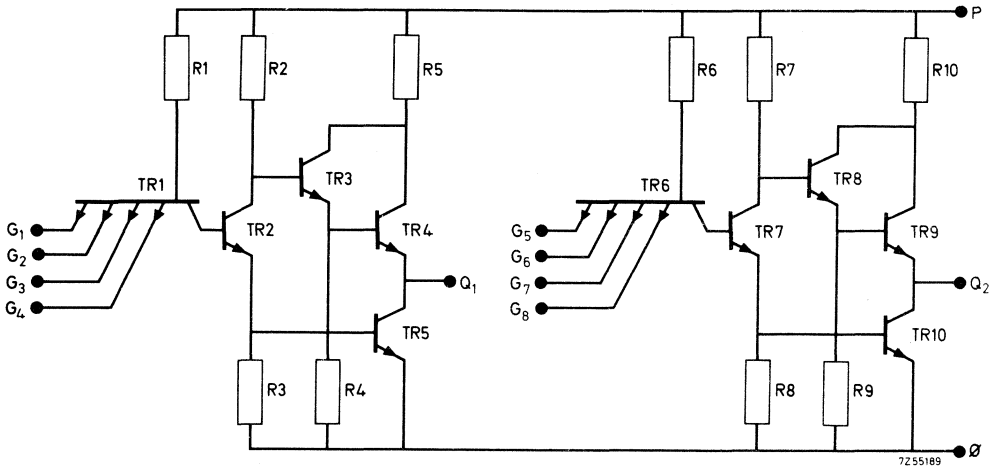


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 30; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	⩾	30	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	26.5	mW

Each gate comprises a multi-emitter AND gate followed by an inverting amplifier and a totem pole power output stage.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM (each gate)



LOGIC FUNCTION

Individual gate operation

$C = \overline{A.B}$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Function table

A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition, peak voltage difference between any two inputs = max. 5.5 V.
[2]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

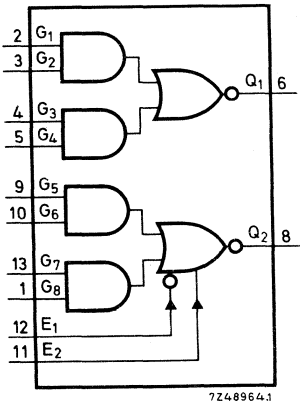
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Output LOW	V_{QLmax}		0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$; $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}		2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}		40	40	40	μA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0V
Output LOW	I_{QLmax}		48	48	48	mA		
Output HIGH	$-I_{QHmax}$		1.2	1.2	1.2	mA		
Output short-circuited	$-I_{Qscmin}$		18	18	18	mA	5.25	$V_Q=0$; $V_G=0$
	$-I_{Qscmax}$		70	70	70	mA		
SUPPLY DATA								
Supply current								
Output LOW	I_{PL}	typ.	17.2	17.2	17.2	mA	5.0	$V_G=5.0$ V; $I_Q=0$
		<	27	27	27	mA	5.0	
Output HIGH	I_{PH}	typ.	4.0	4.0	4.0	mA	5.0	$V_G=0$; $I_Q=0$
		<	8.0	8.0	8.0	mA	5.0	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	-	13	-	ns	5.0	N=30
	t_{pdr}	<	-	22	-	ns		
Fall propagation delay time	t_{pdf}	typ.	-	8	-	ns	5.0	N=30
	t_{pdf}	<	-	15	-	ns		

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

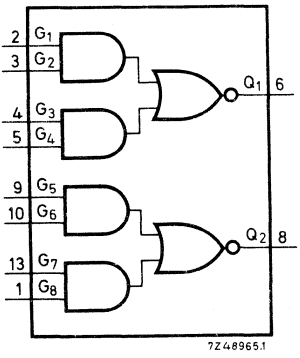
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL AND-OR-NOT GATES

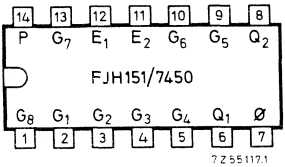
Dual expandable
2+2 input AND-OR-NOT gate FJH151/7450
Dual 2+2 input AND-OR-NOT gate FJH161/7451

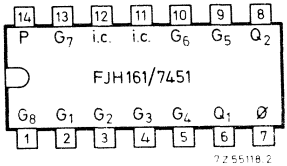


FJH151/7450



FJH161/7451





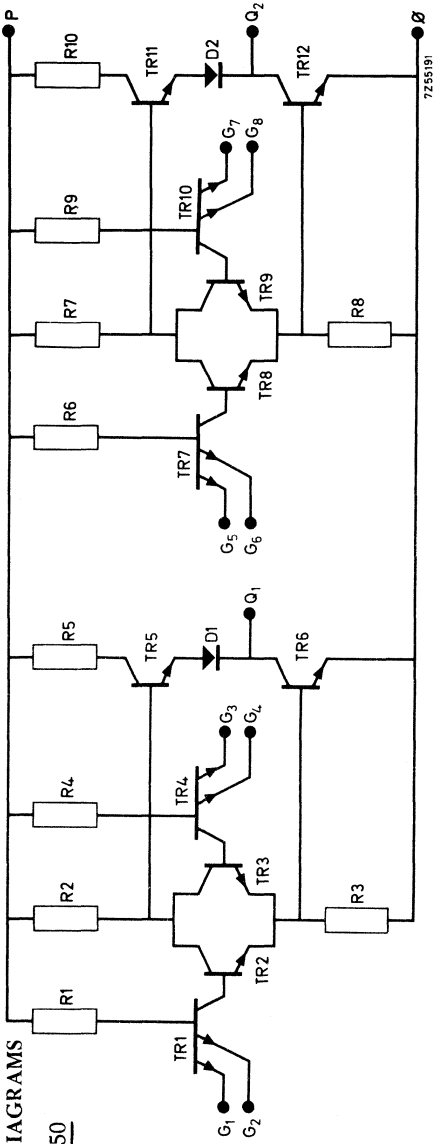
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ. 11	ns
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ. 14.25	mW

The FJH151/7450 is a dual 2+2 input AND-OR-NOT gate, one of the two gates having additional inputs for up to four FJY101/7460 expander circuits. It can be arranged to perform the exclusive OR function.
The FJH161/7451 is similar to the FJH151/7540, except for being non-expandable.

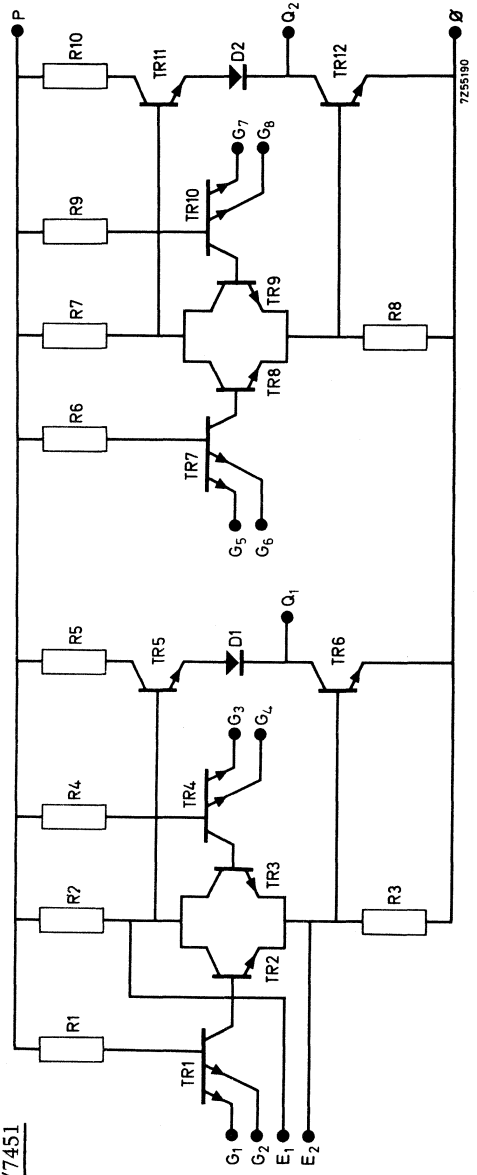
PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS

FJH151/7450



FJH161/7451



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	70	°C

1) In addition, peak voltage difference between any two inputs = max. 5.5 V.
2) Pulse duration t_p = 20 ms; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

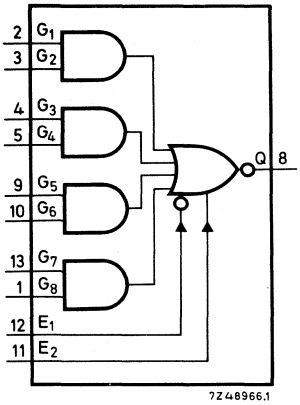
CHARACTERISTICS

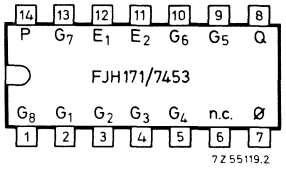
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$; $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}	40	40	40	μA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short-circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_Q=0$; $V_G=0$
	$-I_{Qscmax}$	55	55	55	mA		
SUPPLY DATA							
Supply current							
Output LOW	I_{PL} typ.	7.4	7.4	7.4	mA	5.0	$V_G=5.0$ V; $I_Q=0$
	I_{PL} <	14	14	14	mA	5.0	
Output HIGH	I_{PH} typ.	4.0	4.0	4.0	mA	5.0	$V_G=0$; $I_Q=0$
	I_{PH} <	8.0	8.0	8.0	mA	5.0	
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ.	-	13	-	ns	5.0	N = 10, one pair of AND inputs at V_G = 0.4V
	t_{pdr} <	-	22	-	ns		
Fall propagation delay time	t_{pdf} typ.	-	8	-	ns	5.0	
	t_{pdf} <	-	15	-	ns		

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

EXPANDABLE 2+2+2+2 INPUT AND-OR-NOT GATE



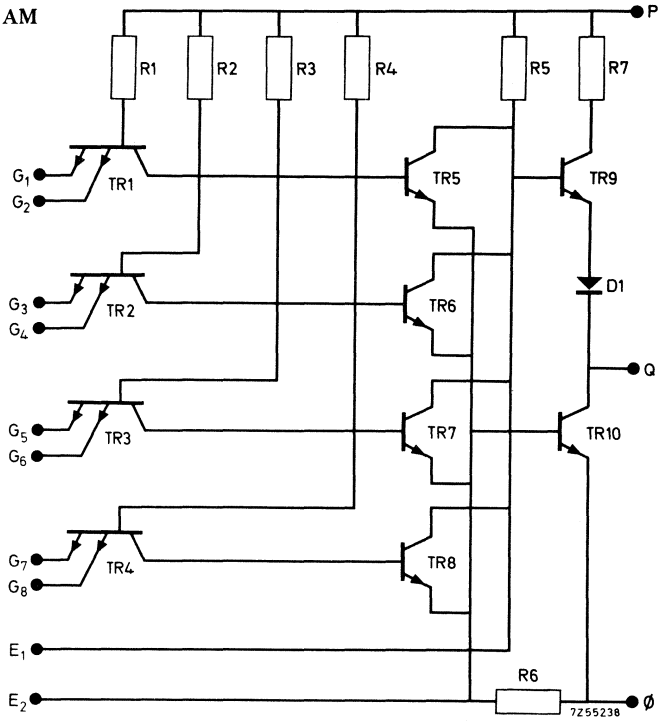


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption T_{amb} = 25 °C	P_{av}	typ.	22.75	mW

The FJH171/7453 has additional inputs for up to four FJY101/7460 expander circuits.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q = \overline{G_1.G_2 + G_3.G_4 + G_5.G_6 + G_7.G_8 + EX}$ (for positive logic)

EX represents the extra function available if gate expander FJY101 is used. (Connect E_1, E_2 to Q_1, Q_2 respectively or to Q_3, Q_4 respectively, of the FJY101 to get a 4-input NAND function).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−55	to +150	°C
Operating ambient temperature	T_{amb}	0	to +70	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}	40	40	40	μA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$ other inputs 0 V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short-circuited (see note 1)	$-I_{Qsc\ min}$ $-I_{Qsc\ max}$	18 55	18 55	18 55	mA mA	5.25	$V_Q = 0$; $V_G = 0$
SUPPLY DATA							
Supply current							
Output LOW	I_{PL} typ.	5.1	5.1	5.1	mA	5.0	$V_G = 5.0$ V; $I_Q = 0$
	I_{PL} <	9.5	9.5	9.5	mA	5.0	
Output HIGH	I_{PH} typ.	4.0	4.0	4.0	mA	5.0	$V_G = 0$; $I_Q = 0$
	I_{PH} <	8.0	8.0	8.0	mA	5.0	
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ.	–	13	–	ns	5.0	N = 10 one pair of AND inputs at $V_G = 0.4$ V
	t_{pdr} <	–	22	–	ns	5.0	
Fall propagation delay time	t_{pdf} typ.	–	8	–	ns	5.0	
	t_{pdf} <	–	15	–	ns	5.0	

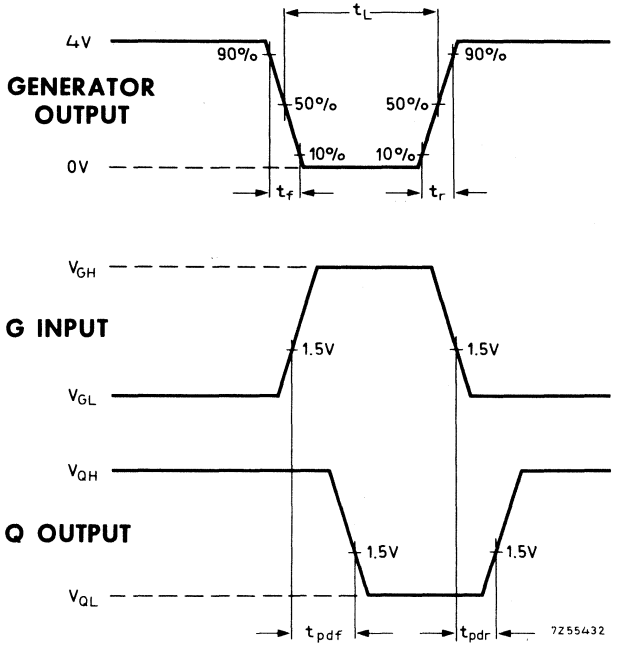
Note 1: Not more than one output must be short circuited at any time.

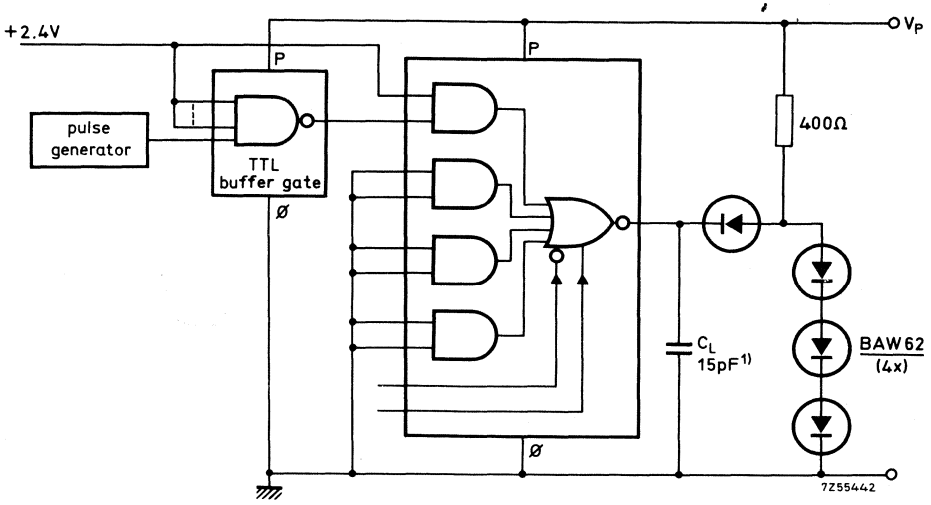
CHARACTERISTICS (continued)

DYNAMIC DATA

Generator:

f = 1 MHz
t_L = 0.5 μs
$t_f \leq 15$ ns
$t_r \leq 15$ ns
R_S = 50 Ω





1) Including probe and jig capacitance.

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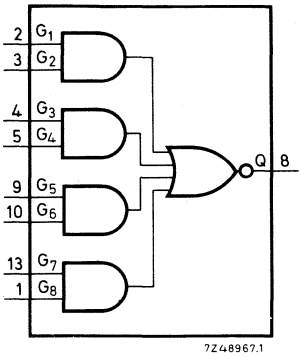
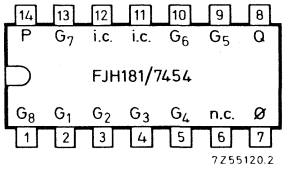
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

2+2+2+2 INPUT AND-OR-NOT GATE

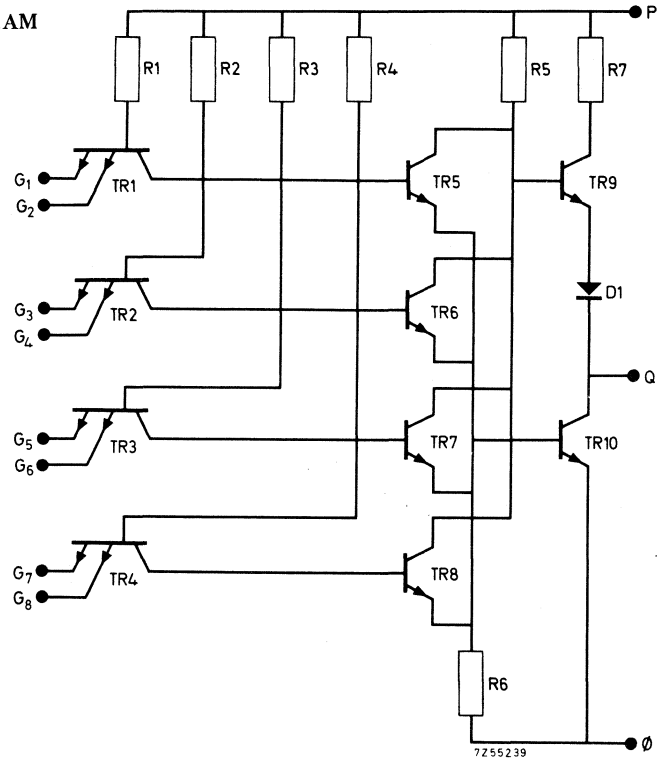




QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	> typ.	0.4 1.0	V V
Average power consumption T_{amb} = 25 °C	P_{av}	typ.	22.75	mW

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q = \overline{G_1 \cdot G_2 + G_3 \cdot G_4 + G_5 \cdot G_6 + G_7 \cdot G_8}$ (for positive logic)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition the voltage between any two inputs must not exceed 5.5 V.
[2]) Pulse duration $t_p = 20$ ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

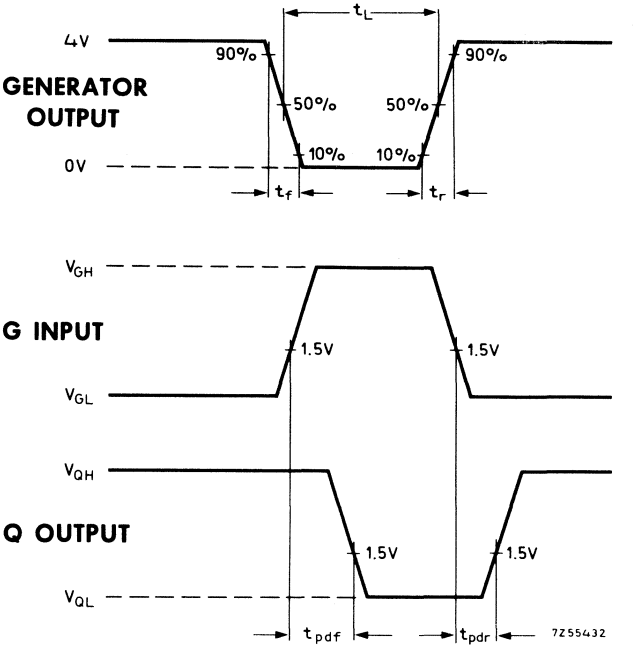
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Output LOW	V_{QLmax}		0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$ $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}		2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}		40	40	40	μA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0 V
Output LOW	I_{QLmax}		16	16	16	mA		
Output HIGH	$-I_{QHmax}$		0.4	0.4	0.4	mA		
Output short-circuited	$-I_{Qsc\ min}$		18	18	18	mA	5.25	$V_Q=0$; $V_G=0$
	$-I_{Qsc\ max}$		55	55	55	mA		
SUPPLY DATA								
Supply current								
Output LOW	I_{PL}	typ.	5.1	5.1	5.1	mA	5.0	$V_G=5.0$ V; $I_Q=0$
		<	9.5	9.5	9.5	mA	5.0	
Output HIGH	I_{PH}	typ.	4.0	4.0	4.0	mA	5.0	$V_G=0$; $I_Q=0$
		<	8.0	8.0	8.0	mA	5.0	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	–	13	–	ns	5.0	N = 10 one pair AND inputs at $V_G=0.4$ V
	t_{pdr}	<	–	22	–	ns	5.0	
Fall propagation delay time	t_{pdf}	typ.	–	8	–	ns	5.0	
	t_{pdf}	<	–	15	–	ns	5.0	

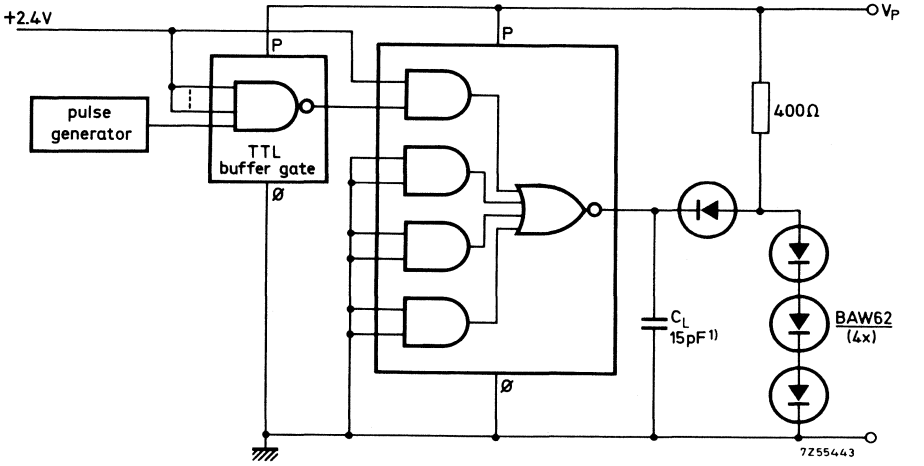
CHARACTERISTICS (continued)

DYNAMIC DATA

Generator

f = 1 MHz
t_L = 0.5 μs
$t_f \leq 15$ ns
$t_r \leq 15$ ns
R_S = 50 Ω



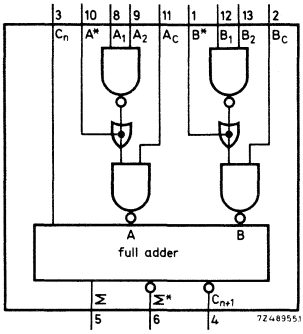


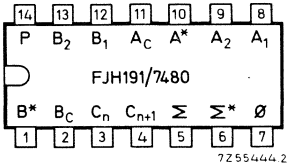
1) Including probe and jig capacitance.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

FULL ADDER



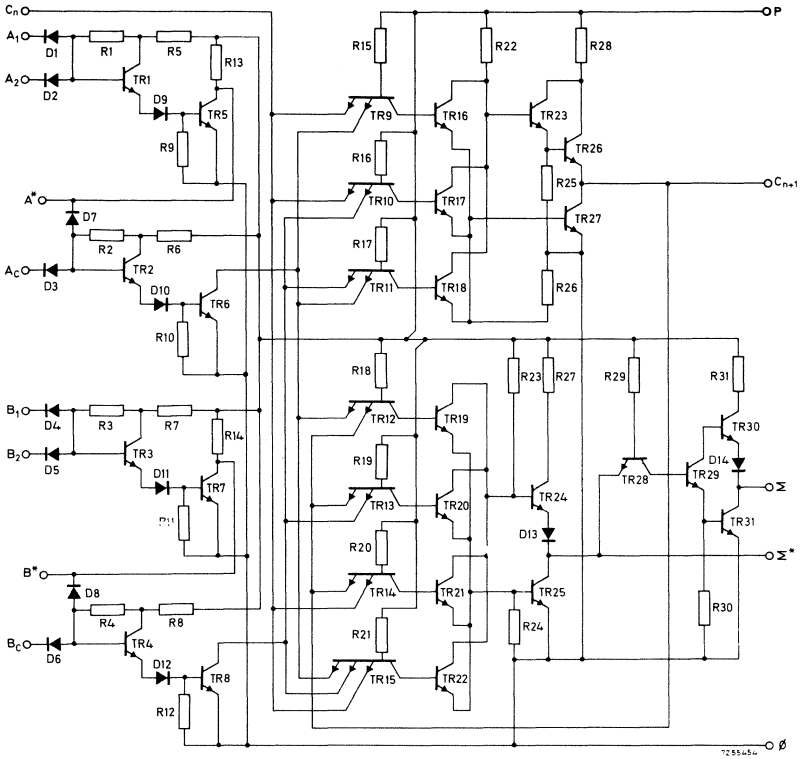


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available d.c. fan-out for outputs: Σ; Σ* (sum outputs)	N_a	≥ 10	
C_n+1 (inverted carry output)	N_a	≥ 5	
Average power consumption	P_{av}	typ. 105	mW

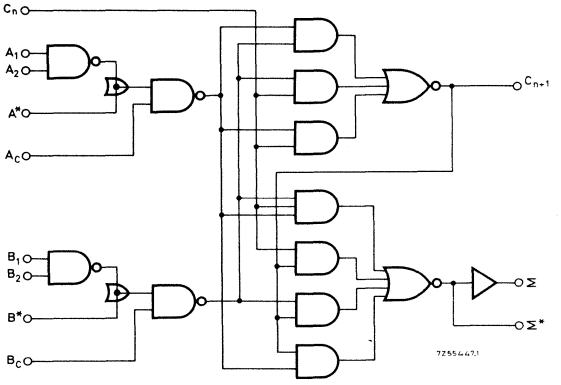
The FJH191/7480 is a single-bit, high speed, binary full adder with gated complementary inputs, complementary sum outputs (Σ and Σ*), and inverted carry output.

PACKAGE OUTLINE :14 lead plastic dual in-line (type A) See General Section

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

C_n	A	B	C_{n+1}	Σ	Σ^*
L	L	L	H	L	H
L	H	L	H	H	L
L	L	H	H	H	L
L	H	H	L	L	H
H	L	L	H	H	L
H	H	L	L	L	H
H	L	H	L	L	H
H	H	H	L	H	L

$A = \overline{A^* \cdot A_C}$

$A^* = \overline{A_1 \cdot A_2}$

$B = \overline{B^* \cdot B_C}$

$B^* = \overline{B_1 \cdot B_2}$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Notes

When A^* is used as an input, A_1 and A_2 must be connected to ϕ; when B^* is used as an input, B_1 and B_2 must be connected to ϕ.

When A_1 and A_2 are used as inputs, A^* must either be open or in wired-OR use; the same applies to B^* when B_1 and B_2 are used as inputs.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_G; V_{Q_1}; V_{Q_2}	max.	5.5	V
Peak negative input voltage	$-V_{IM}$	max.	2	V [1]
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−55 to	+125	°C

[1] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S > 75\ \Omega$

CHARACTERISTICS

		T_{amb} (°C) 0	25	70		Conditions and References V_P (V)	
STATIC DATA							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V	4.75	
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V	4.75	
Output LOW							
at Σ ; Σ^*	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 16 mA
at C_n+1	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 8 mA
at A^*; B^*	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 4.8 mA
Output HIGH							
at Σ ; Σ^*	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −400 µA
at C_n+1	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −200 µA
at A^*; B^*	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −120 µA
Currents							
Input LOW							
at C_n	$-I_{ILmax}$	8.0	8.0	8.0	mA	5.25	$V_I = V_{OLmax}$; $I_O = 0$
at A_1; A_2; A_C; B_1; B_2; B_C	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{OLmax}$; $I_O = 0$
at A^*; B^*	$-I_{ILmax}$	2.6	2.6	2.6	mA	5.25	$V_O = V_{OLmax}$; $I_O = 0$
Input HIGH							
at C_n	I_{IHmax}	200	200	200	µA	5.25	$V_I = V_{OLmax}$; $I_O = 0$
	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V; I_O = 0
at A_1; A_2; A_C	I_{IHmax}	15	15	15	µA	5.25	$V_I = V_{OHmin}$; $I_O = 0$
B_1; B_2; B_C	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V; I_O = 0
Output short circuit							
at Σ ; Σ^*	$-I_{Oscmin}$	18	18	18	mA	5.25	V_O = 0; V_O = 0
	$-I_{Oscmax}$	57	57	57	mA	5.25	
at C_n+1	I_{Oscmin}	18	18	18	mA	5.25	V_O = 0; V_I = 0
	I_{Oscmax}	70	70	70	mA	5.25	
SUPPLY DATA							
Supply current	I_P typ.	21	21	21	mA	5.0	All terminals open
	I_P <	35	35	35	mA	5.0	

CHARACTERISTICS (continued)

		T_{amb} (°C)			Conditions and References		
		0	25	70	V_p (V)	Waveform Fig.1	loading circuit
DYNAMIC DATA							
Rise propagation delay times:							
$C_n \rightarrow C_{n+1}$	t_{pdr} typ.	–	13	– ns	5.0	A	Fig.2
	t_{pdr} <	–	17	– ns	5.0		
$A_1 \rightarrow A^*$	t_{pdr} typ.	–	48	– ns	5.0	A	Fig.3
	t_{pdr} <	–	65	– ns	5.0		
$B_1 \rightarrow B^*$	t_{pdr} typ.	–	48	– ns	5.0	A	Fig.4
	t_{pdr} <	–	65	– ns	5.0		
$B_C \rightarrow C_{n+1}$	t_{pdr} typ.	–	18	– ns	5.0	B	Fig.5
	t_{pdr} <	–	25	– ns	5.0		
$A_C \rightarrow \Sigma$	t_{pdr} typ.	–	52	– ns	5.0	B	Fig.6
	t_{pdr} <	–	70	– ns	5.0		
$B_C \rightarrow \Sigma^*$	t_{pdr} typ.	–	38	– ns	5.0	B	Fig.7
	t_{pdr} <	–	55	– ns	5.0		
Fall propagation delay times:							
$C_n \rightarrow C_{n+1}$	t_{pdf} typ.	–	8	– ns	5.0	A	Fig.2
	t_{pdf} <	–	12	– ns	5.0		
$A_1 \rightarrow A^*$	t_{pdf} typ.	–	17	– ns	5.0	A	Fig.3
	<	–	25	– ns	5.0		
$B_1 \rightarrow B^*$	t_{pdf} typ.	–	17	– ns	5.0	A	Fig.4
	t_{pdf} <	–	25	– ns	5.0		
$B_C \rightarrow C_{n+1}$	t_{pdf} typ.	–	38	– ns	5.0	B	Fig.5
	t_{pdf} <	–	55	– ns	5.0		
$A_C \rightarrow \Sigma$	t_{pdf} typ.	–	62	– ns	5.0	B	Fig.6
	t_{pdf} <	–	80	– ns	5.0		
$B_C \rightarrow \Sigma^*$	t_{pdf} typ.	–	56	– ns	5.0	B	Fig.7
	t_{pdf} <	–	75	– ns	5.0		

CHARACTERISTICS (continued)

DYNAMIC DATA

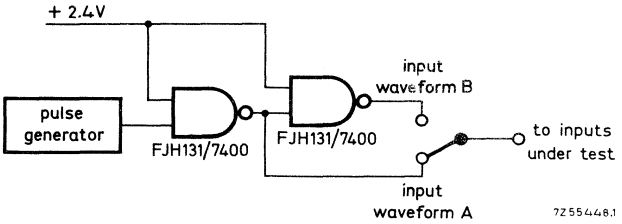


Fig.1

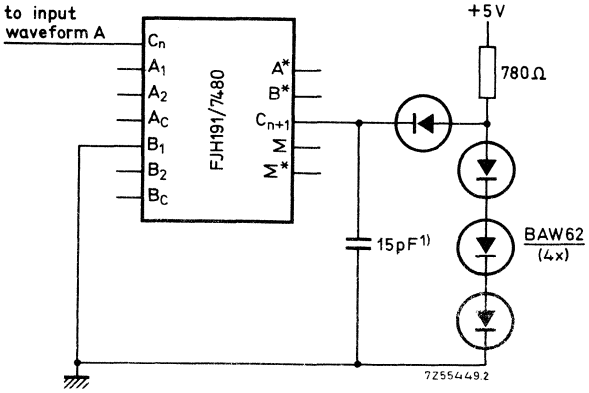


Fig.2 Fan out: N = 5

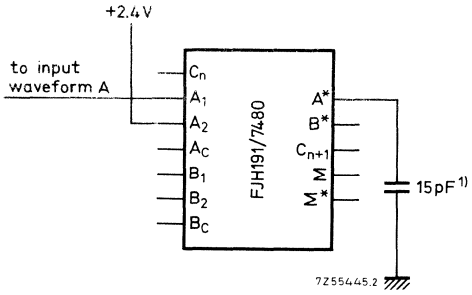


Fig.3

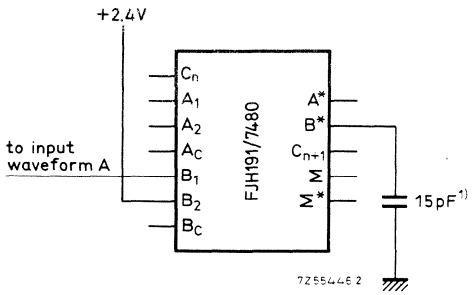


Fig.4

1) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA

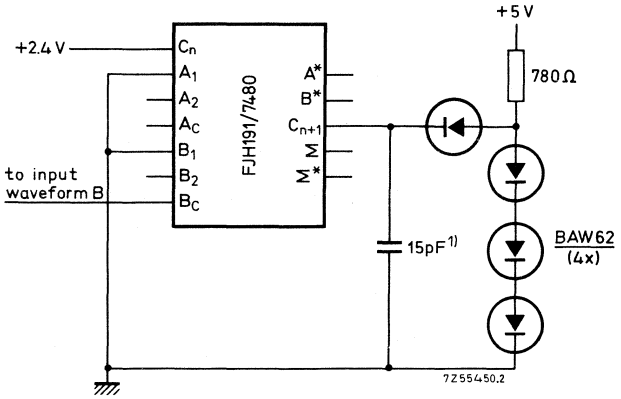


Fig.5 Fan out: N = 5

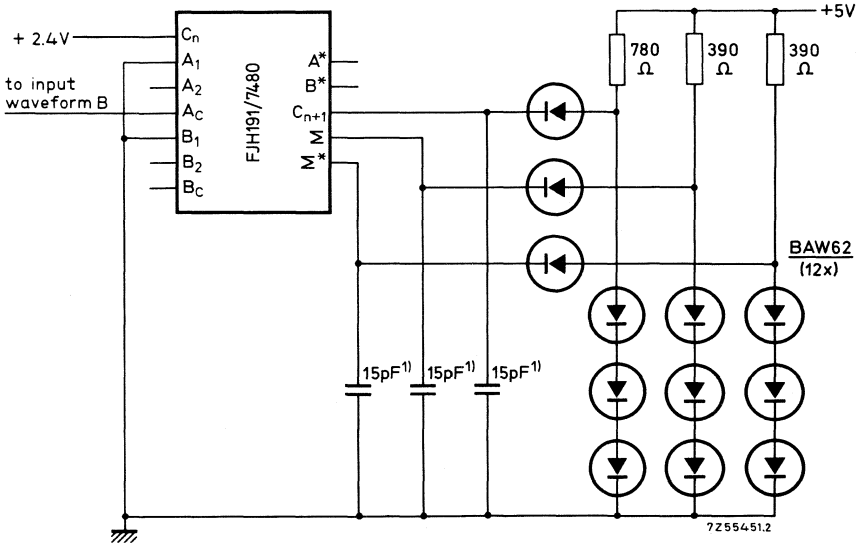


Fig.6 Fan out Q_4: N = 10
Fan out Q_5: N = 10
Fan out Q_3: N = 5

1) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA

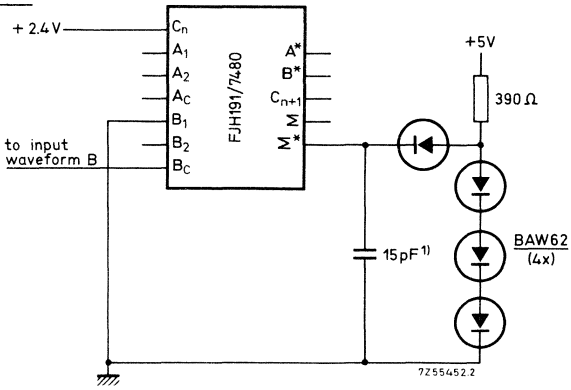
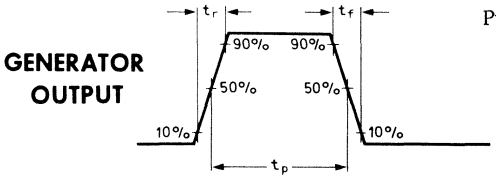
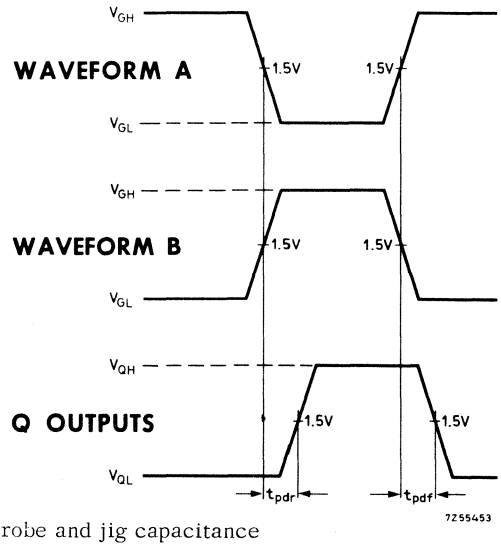


Fig. 7 Fan out: N = 10



Pulse generator:
f = 1 MHz
t_r < 15 ns
t_f < 15 ns
t_p = 0.5 μs
R_S = 50 Ω

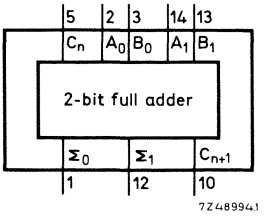


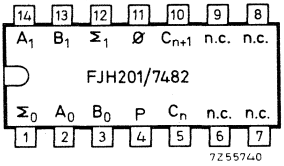
1) Including probe and jig capacitance

The FJ family TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

2 - BIT BINARY FULL ADDER

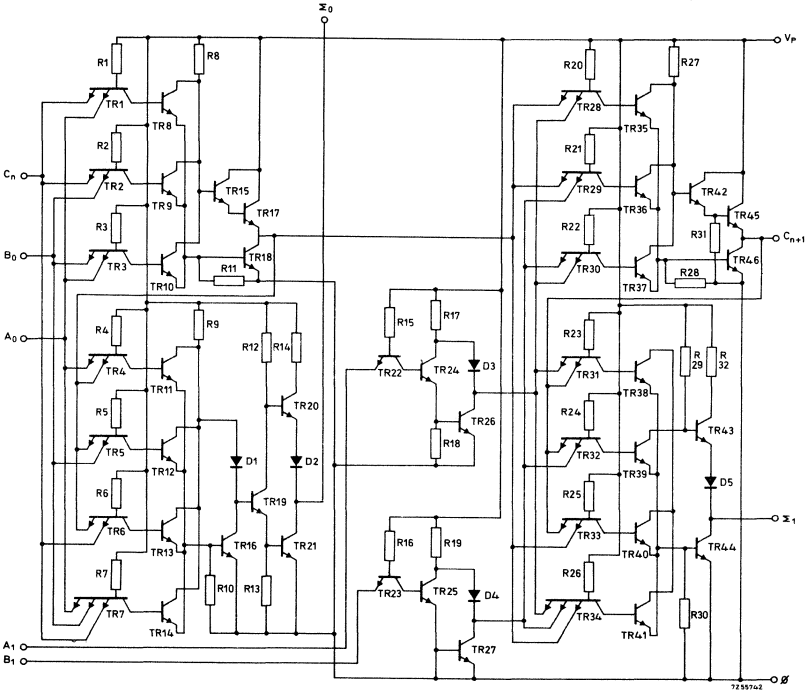




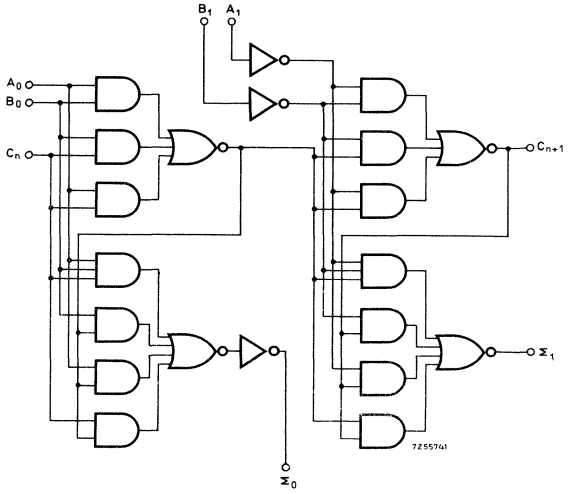
QUICK REFERENCE DATA				
Supply voltage	V_P	5.0	±5%	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Available d.c. fan-out				
for outputs: Σ_0; Σ_1 (sum outputs)	N_a	≥	10	
C_{n+1} (carry output)	N_a	≥	5	
Average power consumption	P_{av}		175	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



The FJH201/7482 full adder is designed for medium-to-high speed, multiple-bit, parallel-add/serial-carry applications and performs the addition of two 2-bit binary numbers. The summation outputs (Σ_0 and Σ_1) are provided for each bit and the resultant carry output (C_{n+1}) is obtained from the second bit. High speed serial-carry circuitry within each bit minimises the necessity for extensive "look-ahead" and carry-cascading circuits.

INPUT				OUTPUT					
				C_n = L			C_n = H		
A_0	B_0	A_1	B_1	Σ_0	Σ_1	C_{n+1}	Σ_0	Σ_1	C_{n+1}
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. input voltage	V_I	max.	5.5	V [1]
Peak negative transient input voltage	$-V_{IM}$	max.	2.0	V [2]
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

1) In addition, the voltage between any two inputs must not exceed 5.5 V.
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V	4.75	
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V	4.75	
Output LOW							
at Σ_0; Σ_1	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 16 mA
at C_{n+1}	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 8 mA
Output HIGH							
at Σ_0; Σ_1	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −400 µA
at C_{n+1}	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −200 µA
Currents							
Input LOW							
at A_1; B_1	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	V_I = 0.4 V
at A_0; B_0; C_n	$-I_{ILmax}$	6.4	6.4	6.4	mA	5.25	V_I = 0.4 V
Input HIGH							
at A_1; B_1	I_{IHmax}	40	40	40	µA	5.25	V_I = 2.4 V
	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V
at A_0; B_0; C_n	I_{IHmax}	160	160	160	µA	5.25	V_I = 2.4 V
	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V
Output LOW							
at Σ_0; Σ_1	I_{OLmax}	16	16	16	mA		
at C_{n+1}	I_{OLmax}	8	8	8	mA		
Output HIGH							
at Σ_0; Σ_1	$-I_{OHmax}$	0.4	0.4	0.4	mA		
at C_{n+1}	$-I_{OHmax}$	0.2	0.2	0.2	mA		
Output short circuit [1]							
at Σ_0; Σ_1; C_{n+1}	$-I_{scmin}$	18	18	18	mA	5.25	
at Σ_0; Σ_1	$-I_{scmax}$	55	55	55	mA	5.25	
at C_{n+1}	$-I_{scmax}$	70	70	70	mA	5.25	
SUPPLY DATA							
Supply current	I_p typ.	35	35	35	mA	5.0	All terminals open
	I_p <	58	58	58	mA	5.0	All terminals open

[1]) Only one output to be shorted at a time

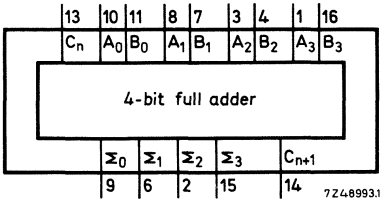
CHARACTERISTICS (continued)

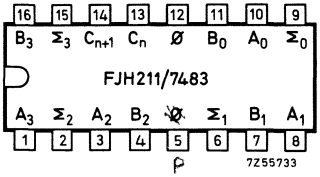
		T_{amb} (°C)			Conditions and references	
		0	25	70	V_P (V)	
DYNAMIC DATA						
Rise propagation delay times						
$C_n \rightarrow \Sigma_0$	t_{pdr} <	–	34	– ns	5.0	C_L = 15 pF; N_a = 10
$B_1 \rightarrow \Sigma_1$	t_{pdr} <	–	40	– ns	5.0	C_L = 15 pF; N_a = 10
$C_n \rightarrow \Sigma_1$	t_{pdr} <	–	38	– ns	5.0	C_L = 15 pF; N_a = 10
$C_n \rightarrow C_{n+1}$	t_{pdr} typ.	–	12	– ns	5.0	C_L = 15 pF; N_a = 5
	t_{pdr} <	–	29	– ns	5.0	C_L = 15 pF; N_a = 5
Fall propagation delay times						
$C_n \rightarrow \Sigma_0$	t_{pdf} <	–	40	– ns	5.0	C_L = 15 pF; N_a = 10
$B_1 \rightarrow \Sigma_1$	t_{pdf} <	–	35	– ns	5.0	C_L = 15 pF; N_a = 10
$C_n \rightarrow \Sigma_1$	t_{pdf} <	–	42	– ns	5.0	C_L = 15 pF; N_a = 10
$C_n \rightarrow C_{n+1}$	t_{pdf} typ.	–	17	– ns	5.0	C_L = 15 pF; N_a = 5
	t_{pdf} <	–	27	– ns	5.0	C_L = 15 pF; N_a = 5

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

4 - BIT FULL ADDER

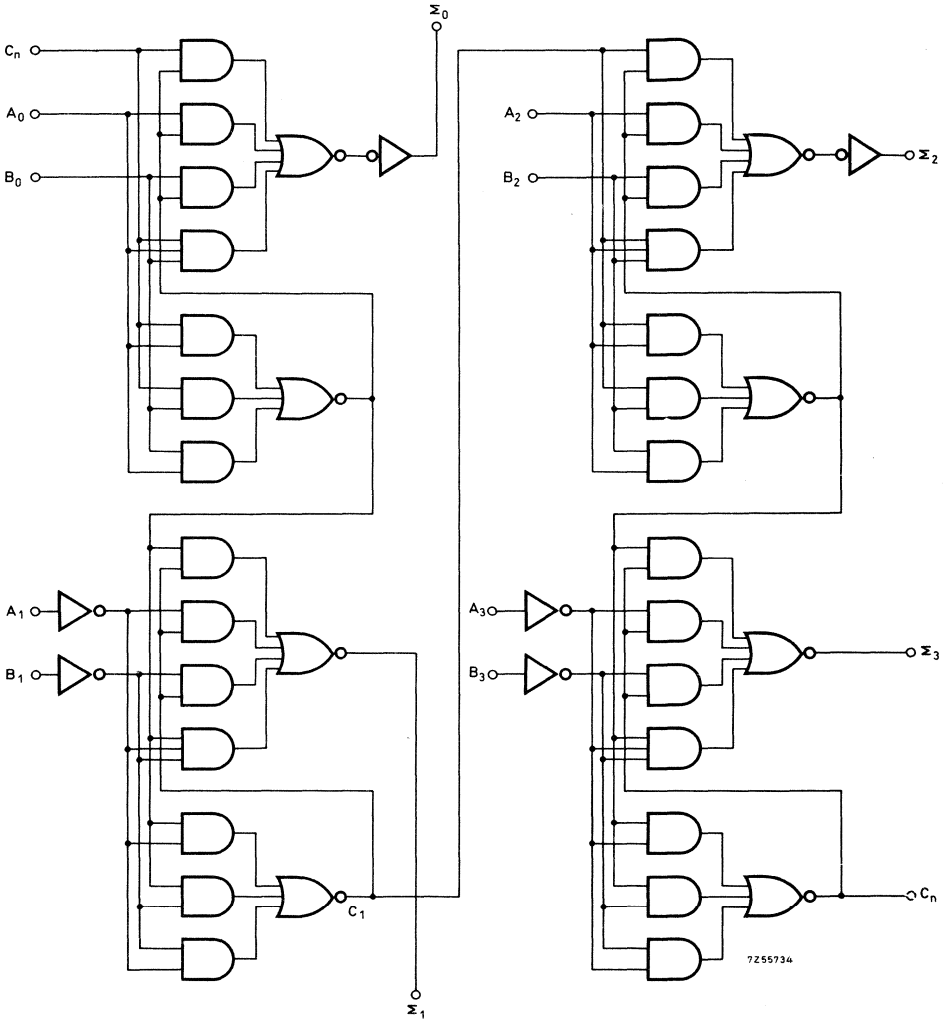




QUICK REFERENCE DATA				
Supply voltage	V_P	5.0 ± 5%		V
Operating ambient temperature	T_{amb}	0 to +70		°C
Available d.c. fan-out (full temperature range)				
from $\Sigma 0$, $\Sigma 1$, $\Sigma 2$, $\Sigma 3$	N_a	>	10	
from C_{n+1}	N_a	>	5	
Average propagation delay time				
$C_n \rightarrow C_{n+1}$	t_{pd}	typ.	29	ns
$C_n \rightarrow \Sigma_3$	t_{pd}	<	55	ns
$B_3 \rightarrow \Sigma_3$	t_{pd}	<	38	ns
D.C. noise margin (full temperature range)	M	>	0.4	V
		typ.	1.0	V
Average power consumption				
T_{amb} = 25 °C	P_{av}	typ.	390	mW

PACKAGE OUTLINE : 16 lead plastic dual in-line (type A) (See General Section)

LOGIC FUNCTION



The FJH211/7483 consists of a full adder for two words of four bits each plus a carry input (C_n). Sum outputs (Σ) are provided for each bit and the carry output (C_{n+1}) is obtained from the last bit. The high-speed internal serial carry circuitry used in the FJH211/7483 minimises the need for external "carry look ahead" logic when cascading adders for long word-length addition.

FUNCTION TABLE

To simplify the function table, it is presented in two parts:

Input conditions at A_0, A_1, B_0, B_1 and C_n determine the outputs Σ_0 and Σ_1 together with the internal carry (C_1) obtained from this addition.

Input conditions at A_2, A_3, B_2, B_3 and the internal carry C_1 determine the outputs Σ_2, Σ_3 and C_{n+1}.

INPUT				OUTPUT					
				C_n = L			C_n = H		
				C_1 = L			C_1 = H		
A_0 / A_2	B_0 / B_2	A_1 / A_3	B_1 / B_3	Σ_0 / Σ_2	Σ_1 / Σ_3	C_1 / C_{n+1}	Σ_0 / Σ_2	Σ_1 / Σ_3	C_1 / C_{n+1}
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_O	max.	5.5	V
D.C. input voltage	V_I	max.	5.5	V 1)
Peak negative input voltage	$-V_{IM}$	max.	2	V 2)
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V	4.75	
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V	4.75	
Output LOW							
at Σ_0, Σ_1, Σ_2, Σ_3	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 16 mA
at C_{n+1}	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 8 mA
Output HIGH							
at Σ_0, Σ_1, Σ_2, Σ_3	V_{OHmin}	2.4	2.4	2.4	V	4.75	$-I_O$ = 400 µA
at C_{n+1}	V_{OHmin}	2.4	2.4	2.4	V	4.75	$-I_O$ = 200 µA
Currents							
Input LOW							
at A_0, A_2, B_0, B_2, C_n	$-I_{ILmax}$	6.4	6.4	6.4	mA	5.25	V_I = 0.4 V
at A_1, A_3, B_1, B_3	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	V_I = 0.4 V
Input HIGH							
at A_0, A_2, B_0, B_2, C_n	I_{IHmax}	160	160	160	µA	5.25	V_I = 2.4 V
at A_1, A_3, B_1, B_3	I_{IHmax}	40	40	40	µA	5.25	V_I = 2.4 V
at all inputs	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V
Output LOW							
at Σ_0, Σ_1, Σ_2, Σ_3	I_{OLmax}	16	16	16	mA		
at C_{n+1}	I_{OLmax}	8	8	8	mA		

1) In addition, the voltage between any two inputs max. 5.5 V
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$

CHARACTERISTICS (continued)

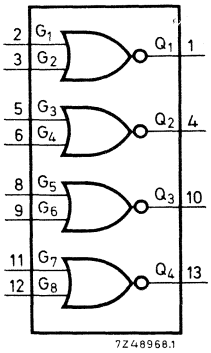
		T_{amb} (°C)			Conditions and references	
		0	25	70	Vp (V)	
STATIC DATA						
Output HIGH						
at Σ_0; Σ_1; Σ_2; Σ_3	$-I_{OHmax}$	400	400	400 µA		
at C_{n+1}	$-I_{OHmax}$	200	200	200 µA		
Output short-circuited [1]						
all outputs	$-I_{scmin}$	18	18	18 mA	5.25	
at Σ_0; Σ_1; Σ_2; Σ_3	$-I_{scmax}$	55	55	55 mA	5.25	
at C_{n+1}	$-I_{scmax}$	70	70	70 mA	5.25	
SUPPLY DATA						
Supply current	I_P typ	–	78	– mA	5.0	
	I_P <	128	128	128 mA	5.25	
DYNAMIC DATA						
Rise propagation delay time						
$C_n \rightarrow \Sigma_0$	t_{pdr} <	–	34	– ns	5.0	$N_a = 10$; $C_L = 15$ pF
$C_n \rightarrow \Sigma_1$	t_{pdr} <	–	38	– ns	5.0	
$C_n \rightarrow \Sigma_2$	t_{pdr} <	–	50	– ns	5.0	
$C_n \rightarrow \Sigma_3$	t_{pdr} <	–	55	– ns	5.0	
$C_n \rightarrow C_{n+1}$	t_{pdr} typ	–	35	– ns	5.0	$N_a = 5$; $C_L = 15$ pF
	t_{pdr} <	–	48	– ns	5.0	
A_1; $B_1 \rightarrow \Sigma_1$	t_{pdr} <	–	40	– ns	5.0	$N_a = 10$; $C_L = 15$ pF
A_3; $B_3 \rightarrow \Sigma_3$	t_{pdr} <	–	40	– ns	5.0	
Fall propagation delay time						
$C_n \rightarrow \Sigma_0$	t_{pdf} <	–	40	– ns	5.0	$N_a = 10$; $C_L = 15$ pF
$C_n \rightarrow \Sigma_1$	t_{pdf} <	–	42	– ns	5.0	
$C_n \rightarrow \Sigma_2$	t_{pdf} <	–	60	– ns	5.0	
$C_n \rightarrow \Sigma_3$	t_{pdf} <	–	55	– ns	5.0	
$C_n \rightarrow C_{n+1}$	t_{pdf} typ	–	22	– ns	5.0	$N_a = 5$; $C_L = 15$ pF
	t_{pdf} <	–	32	– ns	5.0	
A_1; $B_1 \rightarrow \Sigma_1$	t_{pdf} <	–	35	– ns	5.0	$N_a = 10$; $C_L = 15$ pF
A_3; $B_3 \rightarrow \Sigma_3$	t_{pdf} <	–	35	– ns	5.0	

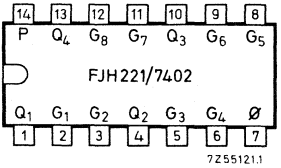
[1]) Not more than one output must be shorted at a time

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

QUADRUPLE 2-INPUT NOR GATE

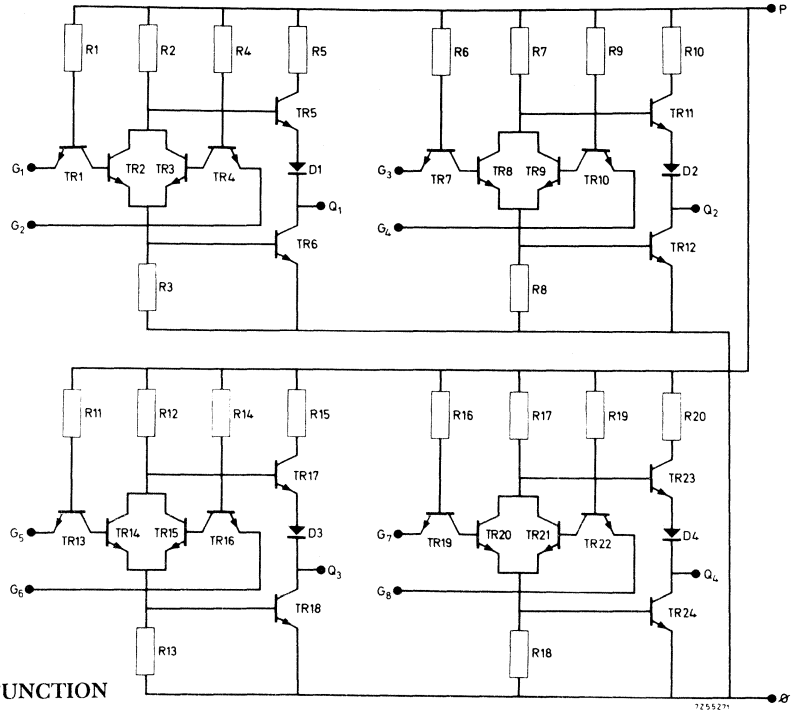




QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	10	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	14.25	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q_1 = \overline{G_1 + G_2}$ $\quad Q_3 = \overline{G_5 + G_6}$

$Q_2 = \overline{G_3 + G_4}$ $\quad Q_4 = \overline{G_7 + G_8}$

for positive logic

Function table

$G_1;G_3$ $G_5;G_7$	$G_2;G_4$ $G_6;G_8$	$Q_1;Q_2$ $Q_3;Q_4$
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

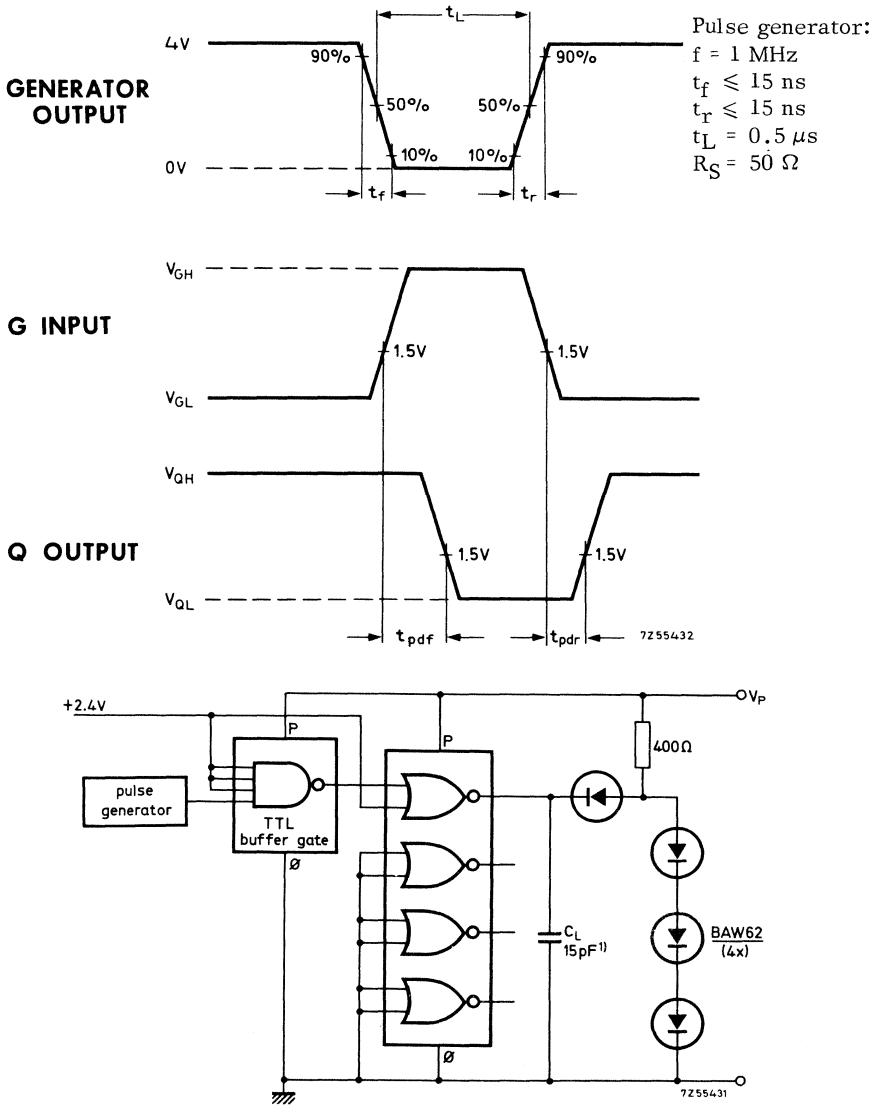
[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Output LOW	V_{QLmax}		0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}		2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}		40	40	40	μA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$ other inputs 0 V
Output LOW	I_{QLmax}		16	16	16	mA		
Output HIGH	$-I_{QHmax}$		0.4	0.4	0.4	mA		
Output short-circuited	$-I_{Qsc}$	min	18	18	18	mA	5.25	$V_Q = 0$; $V_G = 0$
	$-I_{Qsc}$	max	55	55	55	mA		
SUPPLY DATA								
Supply current								
Output LOW	I_{PL}	typ.	14.8	14.8	14.8	mA	5.0	$V_G = 5.0$ V; $I_Q = 0$
		<	27	27	27	mA	5.0	
Output HIGH	I_{PH}	typ.	8.0	8.0	8.0	mA	5.0	$V_G = 0$; $I_Q = 0$
		<	16	16	16	mA	5.0	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	–	12	–	ns	5.0	N = 10 one pair AND inputs at $V_G = 0.4$ V
		<	–	22	–	ns	5.0	
Fall propagation delay time	t_{pdf}	typ.	–	8	–	ns	5.0	
		<	–	15	–	ns	5.0	

CHARACTERISTICS (continued)

DYNAMIC DATA



1) Including probe and jig capacitance

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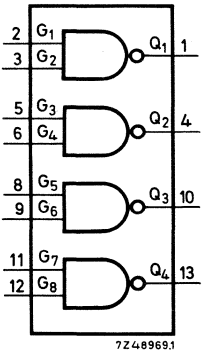
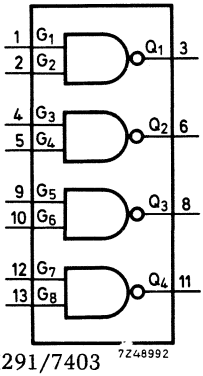
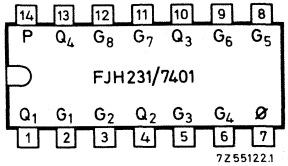
QUADRUPLE 2-INPUT NAND GATE

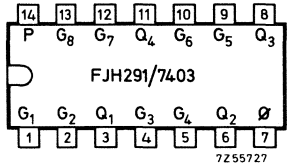


FJH231/7401



FJH291/7403



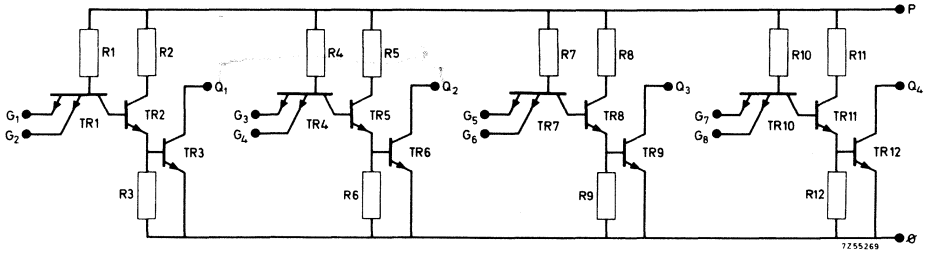


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ. 22	ns
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (each gate) T_{amb} = 25 °C	P_{av}	typ. 7.5	mW

The FJH231/7401 and FJH291/7403 are quadruple 2-input NAND gates with open-collector output transistors for use in "wired-OR" connection with other gates of the FJ family.
The FJH291/7403 is pin-compatible with the FJH131/7400 NAND gate.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See general Section)

CIRCUIT DIAGRAM



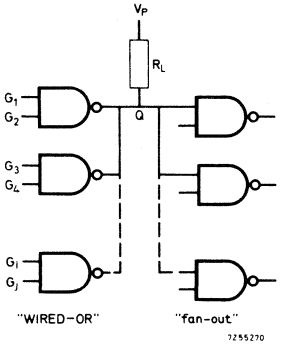
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. output voltage (applied through $R_L \geq 270\ \Omega$)	V_Q	max.	7.0	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}		−55 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ms; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

Fan-out and the "wired-OR" function

TTL gates with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.
A gate alone will drive 10 TTL loads; when it is paralleled with other gates, it can drive from 1 to 9 loads.



To find the proper value of R_L, see application information on page 6.

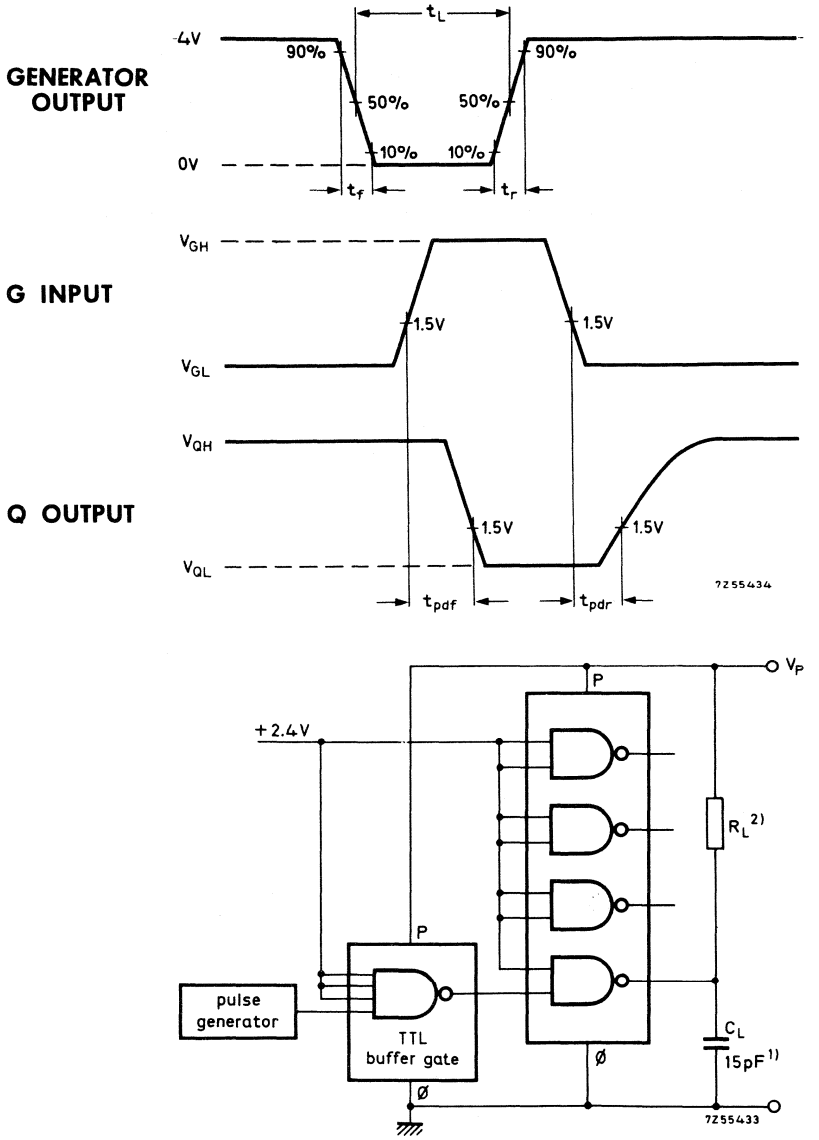
Wired-OR logic function (positive logic)

$$Q = \overline{G_1.G_2 + G_3.G_4 + \ldots\ldots + G_i.G_j}$$

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}	40	40	40	µA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$ other inputs 0 V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH (reverse)	I_{QHmax}	250	250	250	µA	4.75	$V_G = V_{GLmax}$ $V_Q = 5.5$ V
SUPPLY DATA							
Supply current							
Output LOW	I_{PL} typ.	12	12	12	mA	5.0	$V_G = 5.0$ V; $I_Q = 0$
	I_{PL} <	22	22	22	mA	5.0	
Output HIGH	I_{PH} typ.	4.0	4.0	4.0	mA	5.0	$V_G = 0$; $I_Q = 0$
	<	8	8	8	mA	5.0	
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ.	–	35	–	ns	5.0	$R_L = 3.9$ kΩ; $C_L = 15$ pF
	t_{pdr} <	–	45	–	ns	5.0	
Fall propagation delay time	t_{pdf} typ.	–	8	–	ns	5.0	$R_L = 390$ Ω; $C_L = 15$ pF
	t_{pdf} <	–	15	–	ns	5.0	

CHARACTERISTICS (continued)



1) Including probe and jig capacitance

2) R_L = 390 Ω for t_{pdf}
R_L = 3900 Ω for t_{pdr}

APPLICATION INFORMATION

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table 1

fan-out to TTL loads	wired-OR outputs							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000*
	maximum							min.
	load resistor values in ohms							

X = not recommended or not possible

* = the thoretical value is ∞

All values shown in the table are based on:

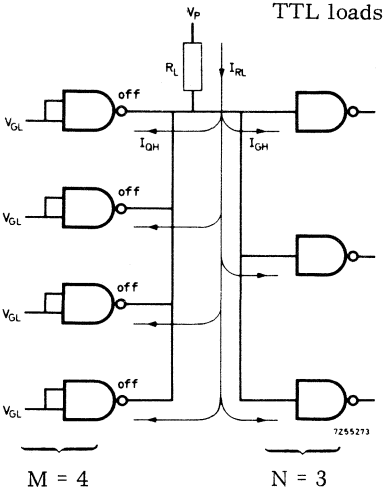
Logical HIGH conditions: V_P = 5 V; V_{QH} required = 2.4 V

Logical LOW conditions: V_P = 5 V; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$M.I_{QH} = 4 \times 250\ \mu A$ $\quad N.I_{GH} = 3 \times 40\ \mu A$ $\quad R_{Lmax} = \dfrac{(5-2.4)V}{(0.001 + 0.00012)A} = 2321\ \Omega$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

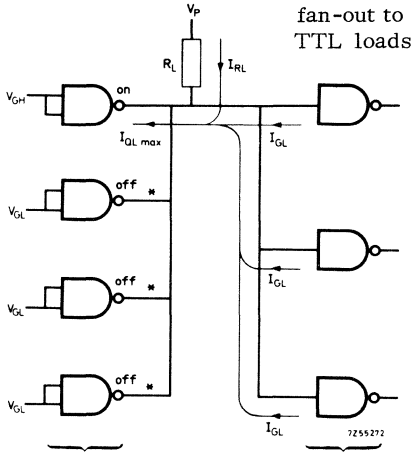
$$I_{RL} = M.I_{QH} + N.I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M.I_{QH} + N.I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



M = 4 N = 3

I_{QLmax} = 16 mA N. $|I_{GLmax}|$ = 3 x 1.6 mA $R_{Lmin} = \frac{(5-0.4)V}{(0.016-0.0048)A} = 410\ \Omega$

*current through OFF outputs negligible at LOW output state

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistors, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.
The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L.
These considerations lead to the minimum value of R_L

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N.|I_{GLmax}|}$$

For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.
For a single output the values are determined by the fan-out plus the leakage current of one transistor.
More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.
The value of R_L for driving 10 loads should be infinite according to these calculations but 4 kΩ is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

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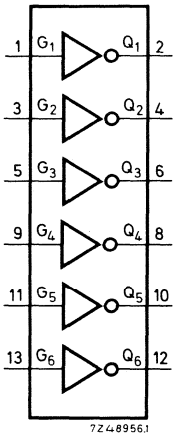
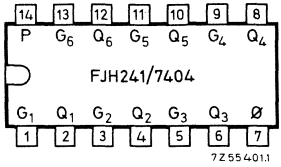
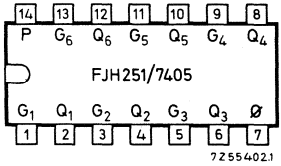
SEXTUPLE SINGLE INPUT INVERTERS

Sextuple single input inverter with an active output (totem pole): FJH241/7404
Sextuple single input inverter with an open collector output: FJH251/7405







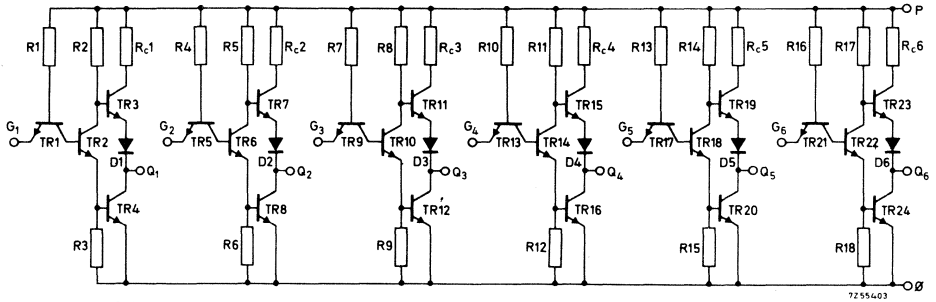
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	FJH241/7404: t_{pd}	typ. 10	ns
	FJH251/7405: t_{pd}	typ. 24	ns
Available d.c. fan-out; full temperature range (for FJH251/7405 see table on page 5)	N_a	< 10	
D.C. noise margin (full temperature range)	M_L	> 0.4	V
		typ. 1.0	V
Average power consumption (each gate) T_{amb} = 25 °C	P_{av}	typ. 10	mW

The FJH241/7404 is a sextuple single-input inverter with an active output (totem pole). The FJH251/7405 is a sextuple single-input inverter with an open collector output transistor. It can be used in wired-OR connections with other gates of the FJ family.

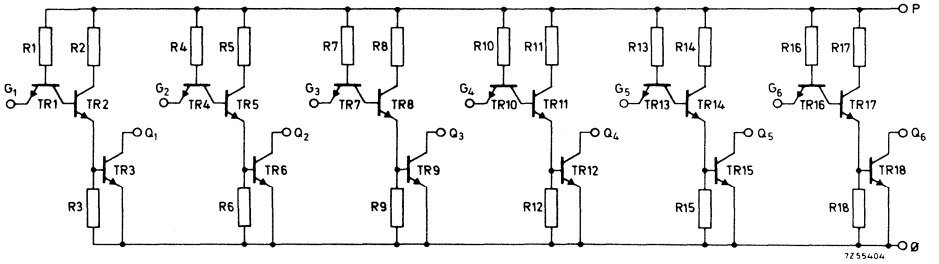
PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS

FJH241/7404



FJH251/7405

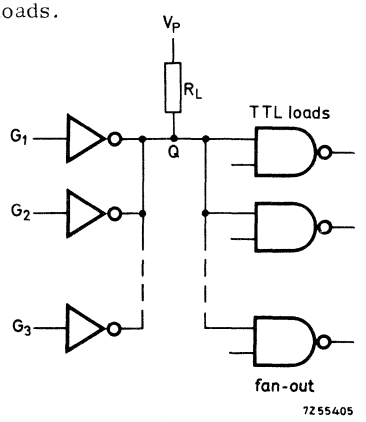


RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
G input voltage	V_G	max.	5.5	V
Peak negative G input voltage	$-V_{GM}$	max.	2	V [1]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

Fan-out and "wired-OR" function of FJH251/7405

TTL inverters with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.
An inverter **alone** will drive 10 TTL loads; when it is paralleled with other inverters it can drive from 1 to 9 TTL loads.



To find the proper value of R_L see application information on page 5.

Wired-OR logic function (positive logic)

$$Q = \overline{G_1 + G_2 + \ldots . G_i}$$

[1]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C) 0	25	75	Conditions and References V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8 V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents						
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6 mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}	40	40	40 μA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$
Output LOW	I_{QLmax}	16	16	16 mA		
Output HIGH FJH241/7404	$-I_{QHmax}$	400	400	400 μA	4.75	$V_Q = V_{QHmin}$
Output reverse HIGH; FJH251/7405	I_{QHmax}	250	250	250 μA	4.75	$V_G = V_{GLmax}$; $V_Q = 5.5$ V
Output short circuited FJH241/7404 See note 1	$-I_{Qscmin}$	18	18	18 mA	5.25	$V_G = 0$; $V_Q = 0$
	$-I_{Qscmax}$	55	55	55 mA	5.25	
SUPPLY DATA						
Output LOW	I_{PL} typ.	18	18	18 mA	5.0	$V_G = 5$ V; $I_Q = 0$
	<	33	33	33 mA	5.0	
Output HIGH	I_{PH} typ.	6	6	6 mA	5.0	$V_G = 0$; $I_Q = 0$
	<	12	12	12 mA	5.0	
DYNAMIC DATA						
Rise propagation delay time: FJH241/7404	t_{pdr} typ.	–	12	– ns	5.0	$R_L = 390\ \Omega$; $C_L = 15$ pF
	t_{pdr} <	–	22	– ns	5.0	
FJH251/7405	t_{pdr} typ.	–	40	– ns	5.0	$R_L = 3.9$ kΩ; $C_L = 15$ pF
	t_{pdr} <	–	55	– ns	5.0	
Fall propagation delay time	t_{pdf} typ.	–	8	– ns	5.0	$R_L = 390\ \Omega$; $C_L = 15$ pF
	t_{pdf} <	–	15	– ns	5.0	

Note 1: Not more than one output should be short circuited at a time

APPLICATION INFORMATION for FJH251/7405

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table I

fan-out to TTL loads	wired-OR outputs							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000*
	maximum							min.
	load resistor values in ohms							

X = not recommended or not possible

* = the theoretical value is ∞

All values shown in the table are based on:

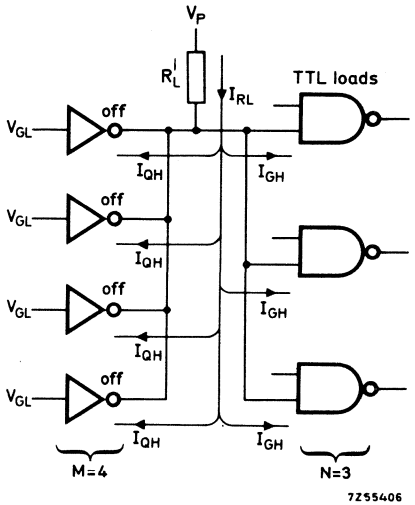
Logical HIGH conditions: V_P = 5 V; V_{QH} required = 2.4 V

Logical LOW conditions: V_P = 5 V; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$M.I_{QH} = 4 \times 250\ \mu A$ $\quad N.I_{GH} = 3 \times 40\ \mu A$ $\quad R_{Lmax} = \dfrac{(5-2.4)V}{(0.001 + 0.00012)A} = 2321\ \Omega$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

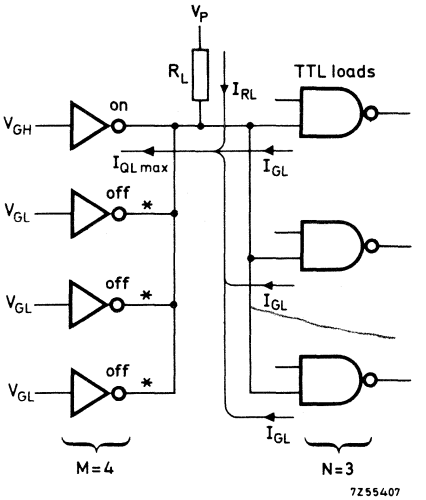
$$I_{RL} = M.I_{QH} + N.I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M.I_{QH} + N.I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



I_{QLmax} = 16 mA N. $|I_{GLmax}|$ = 3 x 1.6 mA $R_{Lmin} = \frac{(5-0.4)V}{(0.016-0.0048)A} = 410\ \Omega$

*current through OFF outputs negligible at LOW output state

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistor, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.
The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L;
These considerations lead to the minimum value of R_L

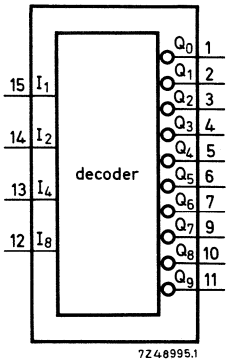
$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N.|I_{GLmax}|}$$

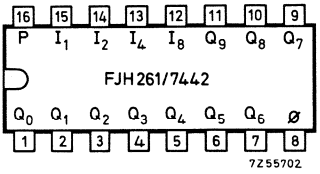
For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.
For a single output the values are determined by the fan-out plus the leakage current of one transistor.
More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.
The value of R_L for driving 10 loads should be infinite according to these calculations but 4 kΩ is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

BCD-to-DECIMAL DECODER





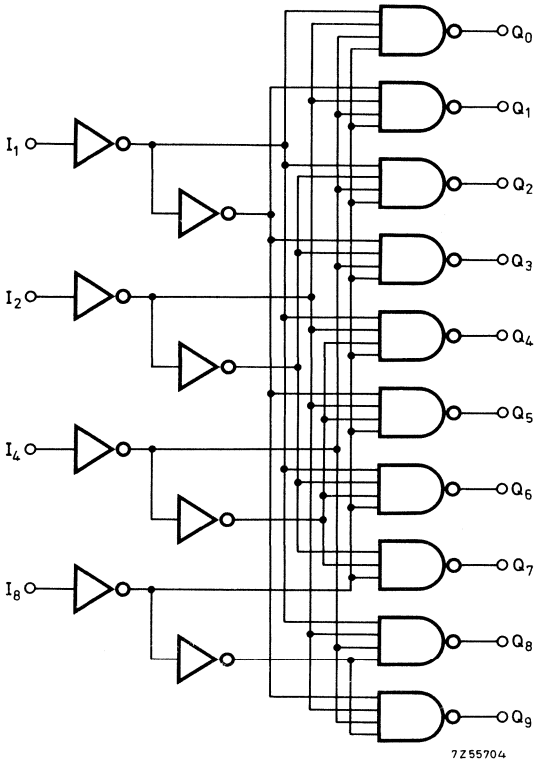
QUICK REFERENCE DATA			
Supply voltage	V_P	5 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available d.c. fan-out (each output)	N_a	≥ 10	
Average propagation delay	t_{pd}	typ. 20	ns
Average power consumption	P_{av}	typ. 140	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

GENERAL DESCRIPTION

The FJH261/7442 is a multipurpose decoder which accepts four BCD (8-4-2-1 code) inputs and provides ten mutually exclusive outputs.
The active LOW outputs facilitate addressing functions when inverting drivers are used. Full decoding of valid input logic ensures that all outputs remain HIGH (off) for input binary codes greater than nine.
The most significant input (I_8) provides a useful inhibit function when the FJH261/7442 is used as a 1-of-8 decoder, as shown in the APPLICATION INFORMATION section on page 6.

LOGIC DIAGRAM



FUNCTION TABLE

inputs				outputs									
I_8	I_4	I_2	I_1	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH (the more positive voltage)
L = LOW (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7	V
Input voltage (d.c.)	V_I	max.	5.5	V [1]
Negative transient input voltage (t_p = 20 ns; f = 5 MHz, $R_S \geq 75\ \Omega$)	$-V_{IM}$	max.	2	V
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

[1]) In addition, the voltage between any two inputs must not exceed 5.5 V.

CHARACTERISTICS

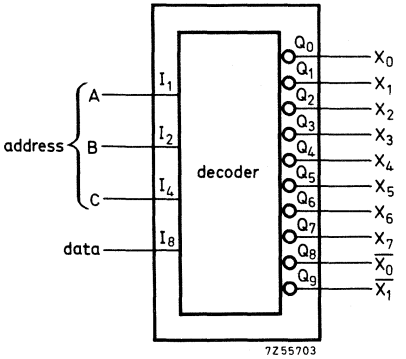
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V	4.75	
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V	4.75	
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	I_Q = 16 mA
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q$ = 400 µA
Currents							
Input LOW (each input)	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	V_I = 0.4 V
Input HIGH (each input)	I_{IHmax}	40	40	40	µA	5.25	V_I = 2.4 V
	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V
Output LOW	I_{QLmax}	16	16	16	mA		
Output short circuited [1]	$-I_{Qsc\ min}$	18	18	18	mA	5.25	
	$-I_{Qsc\ max}$	55	55	55	mA	5.25	
SUPPLY DATA							
Supply current	I_P typ.	--	28	-	mA	5.0	V_I = 0 V
	$I_P \leq$	56	56	56	mA	5.25	V_I = 0 V
DYNAMIC DATA		min.	typ.	max.			
Propagation delay times							
Rise: through two logic levels	t_{pdr}	10	17	25	ns	5.0	C_L = 15 pF, N = 10, T_{amb} = 25 °C
through three logic levels	t_{pdr}	-	26	35	ns	5.0	C_L = 15 pF, N = 10, T_{amb} = 25 °C
Fall: through two logic levels	t_{pdf}	10	22	30	ns	5.0	C_L = 15 pF, N = 10, T_{amb} = 25 °C
through three logic levels	t_{pdf}	-	23	35	ns	5.0	C_L = 15 pF, N = 10, T_{amb} = 25 °C

[1]) Only one output to be shorted at a time.

APPLICATION INFORMATION

Digital demultiplexer

Data may be routed from a single source to any of 8 outputs by addressing that output. All other outputs remain HIGH. Complements of outputs Q_0 and Q_1 are available at Q_8 and Q_9 respectively.

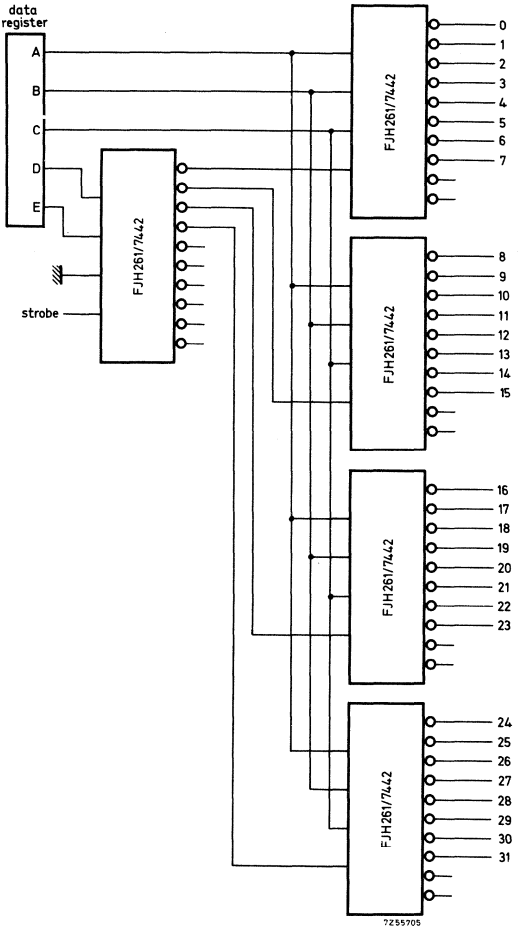


address			output
A	B	C	line
L	L	L	X_0
H	L	L	X_1
L	H	L	X_2
H	H	L	X_3
L	L	H	X_4
H	L	H	X_5
L	H	H	X_6
H	H	H	X_7

APPLICATION INFORMATION (continued)

1-of-32 decoding

The general purpose nature of the FJH261/7442 is shown by this application, where the most significant input (I_8) is used as an inhibit in the four 1-of-8 decoders.



QUADRUPLE 2-INPUT NAND GATE

For data of this type please refer to FJH231/7401

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

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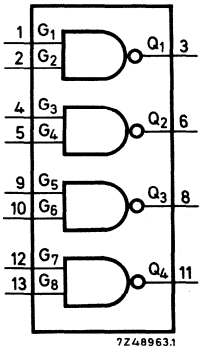
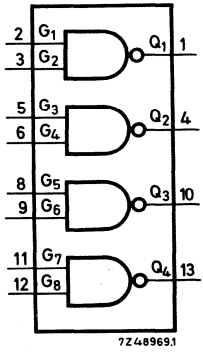
NAND GATES

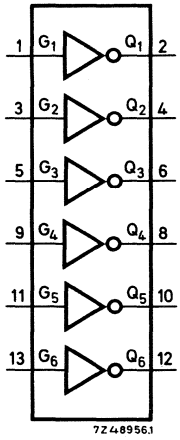
Quadruple 2-input NAND gate, with open collector — FJH301/7426
Quadruple 2-input NAND gate, with open collector — FJH311/7401-S1
Sextuple single input inverter, with open collector — FJH321/7405-S1



FJH301/7426



FJH311/7401-S1



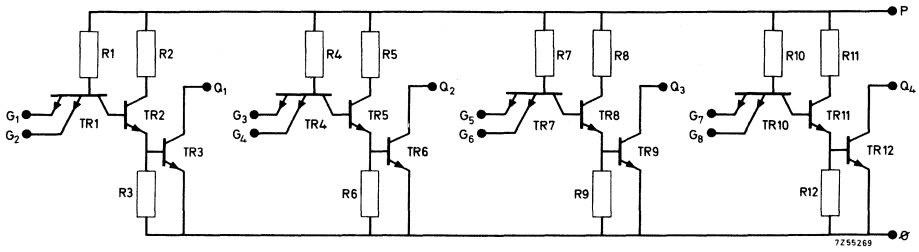
FJH321/7405-S1

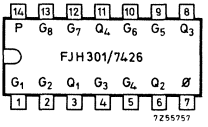
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Output voltage	V_Q	max. 15	V
Average propagation delay			
N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	max. 22	ns
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4	V
		typ. 1.0	V
Average power consumption at T_{amb} = 25 °C	P_{av}	typ. 10	mW

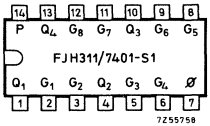
PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) See General Section

CIRCUIT DIAGRAMS

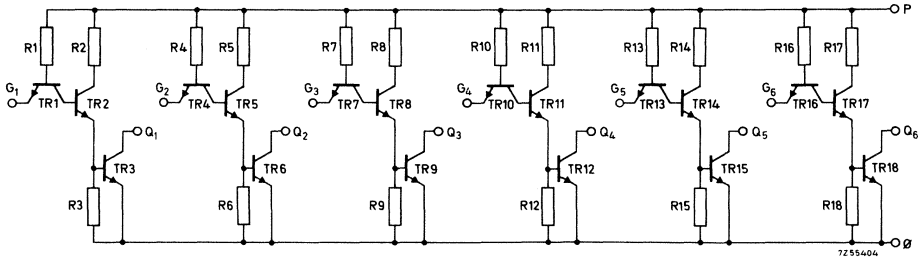
FJH301/7426 and FJH311/7401-S1

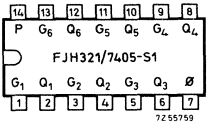






FJH321/7405-S1





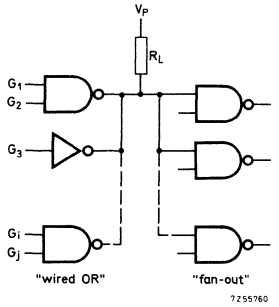
This series of open-collector NAND gates features 15 V output voltage ratings and is intended to be used for interfacing with MOS logic or as open-collector drivers for indicator lamps and relays.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. output voltage	V_Q	max.	15	V
D.C. input voltage	V_G	max.	5.5	V [1]
Peak negative input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

Fan-out and the "wired-OR" function

TTL gates with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.
A gate alone will drive 10 TTL loads; when it is paralleled with other gates, it can drive from 1 to 9 loads.



To find the proper value of R_L, see application information on page 6.

Wired-OR logic function (positive logic)

$$Q = \overline{G_1 \cdot G_2 + G_3 + \ldots\ldots\ldots + G_i \cdot G_j}$$

1) In addition, the voltage between any two inputs must not exceed 5.5 V
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$

CHARACTERISTICS

		T_{amb}(°C)				Conditions and References	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{GLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	15	15	15	V	4.75	$-I_Q$ = 1 mA; $V_G = V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}	40	40	40	µA	5.25	V_G = 2.4 V; $I_Q = 0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output reverse HIGH	I_{QHmax}	50	50	50	µA	4.75	$V_G = V_{GLmax}$; V_Q = 12 V
SUPPLY DATA							
Supply current							
Output LOW	I_{PL} typ.	–	12	–	mA	5.0	V_G = 5 V; $I_Q = 0$
	I_{PL} <	–	22	–	mA	5.0	
Output HIGH	I_{PH} typ.	–	4	–	mA	5.0	$V_G = 0$; $I_Q = 0$
	I_{PH} <	–	8	–	mA	5.0	
DYNAMIC DATA							
Rise propagation delay time:	t_{pdr} typ.	–	35	–	ns	5.0	R_L = 390 Ω; C_L = 15 pF
	t_{pdr} <	–	45	–	ns	5.0	
Fall propagation delay time:	t_{pdf} typ.	–	8	–	ns	5.0	R_L = 390 Ω; C_L = 15 pF
	t_{pdf} <	–	15	–	ns	5.0	

APPLICATION INFORMATION

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table 1

fan-out to TTL loads	wired-OR outputs							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000*
	maximum							min.
	load resistor values in ohms							

X = not recommended or not possible

* = the theoretical value is ∞

All values shown in the table are based on:

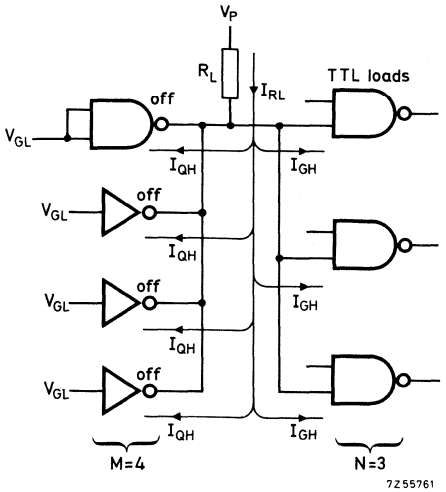
Logical HIGH conditions: V_P = 5 V; V_{QH} required = 2.4 V

Logical LOW conditions: V_P = 5 V; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$M.I_{QH} = 4 \times 250\ \mu A$ $\quad N.I_{GH} = 3 \times 40\ \mu A$ $\quad R_{Lmax} = \frac{(5-2.4)V}{(0.001+0.00012)A} = 2321\ \Omega$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

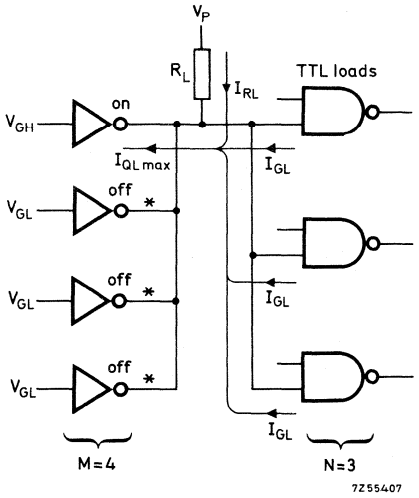
$$I_{RL} = M.I_{QH} + N.I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M.I_{QH} + N.I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



I_{QLmax} = 16 mA N. $|I_{GLmax}|$ = 3 x 1.6 mA $R_{Lmin} = \frac{(5-0.4)V}{(0.016-0.0048)A} = 410\ \Omega$

*current through OFF outputs negligible at LOW output state

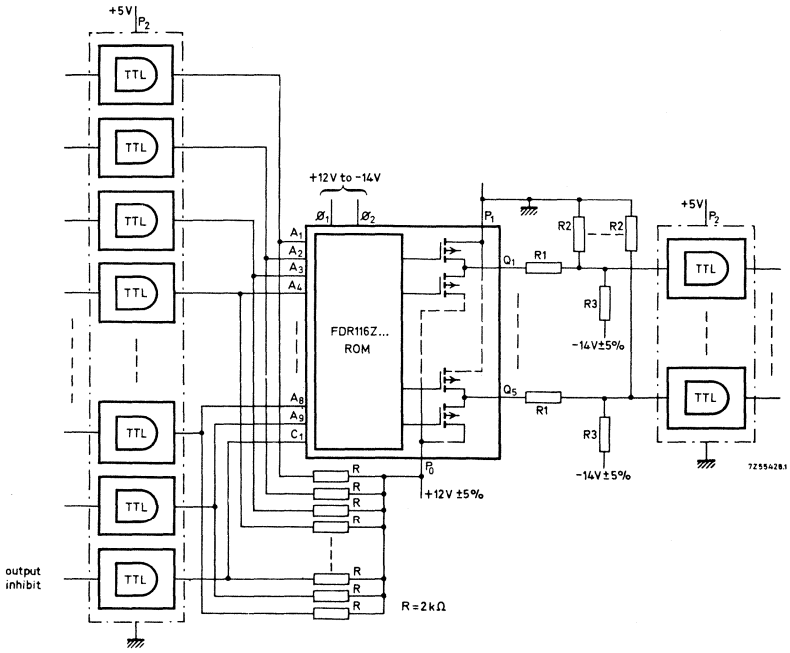
The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistor, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.
The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L;
These considerations lead to the minimum value of R_L

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N.\ |I_{GLmax}|}$$

For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.
For a single output the values are determined by the fan-out plus the leakage current of one transistor.
More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.
The value of R_L for driving 10 loads should be infinite according to these calculations but 4 kΩ is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

APPLICATION INFORMATION (continued)

Typical application of open-collector gates as interface with MOS circuit.



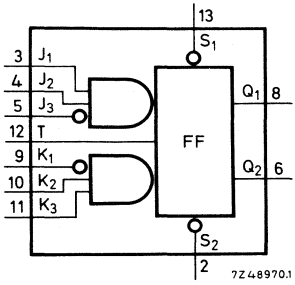
The example above shows a FDR116Z 2560-bit read-only memory being used together with TTL.

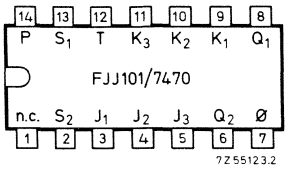
Open-collector gates are used at the input interface, each collector being taken through a 2 kΩ resistor to the 12 V positive supply voltage of the FDR116Z. A normal totem-pole output FJ type is used as the output to restore the TTL logic levels.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE JK FLIP-FLOP (AND INPUTS)



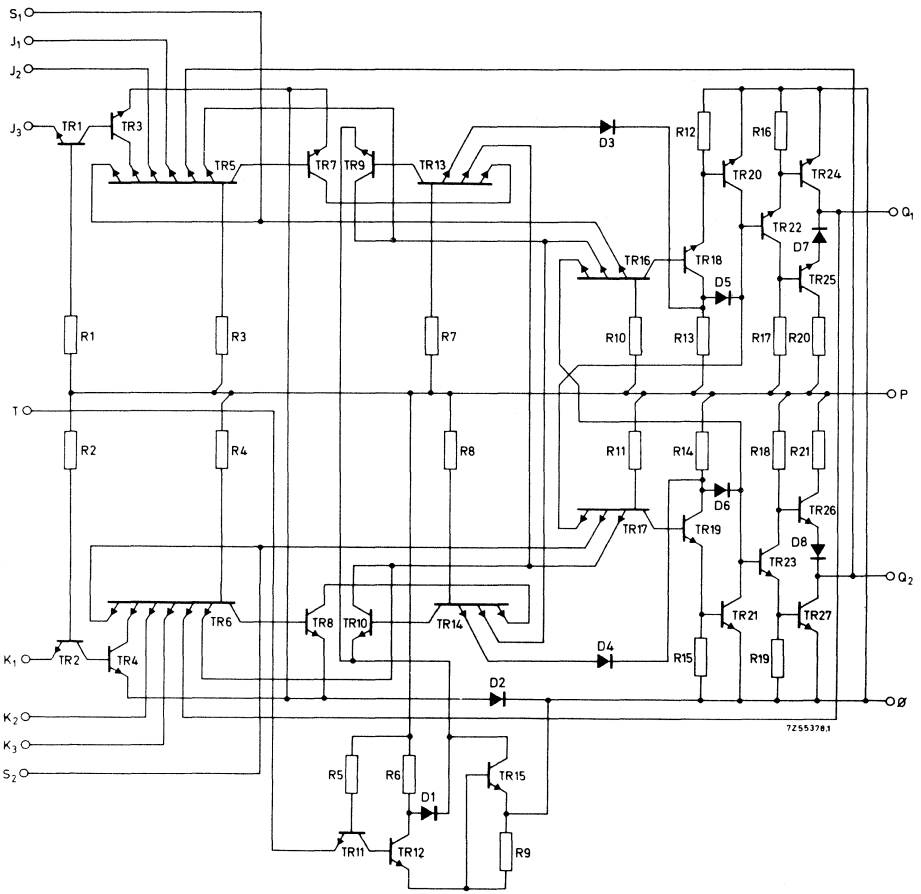


QUICK REFERENCE DATA				
Supply voltage	V_P	5.0 ± 5%		V
Operating ambient temperature range	T_{amb}	0 to +70		°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
Max. operating frequency; T_{amb} = 25 °C	f	>	20	MHz
Average power consumption; T_{amb} = 25 °C	P_{av}	typ.	70	mW

The FJJ101/7470 is a monolithic, edge-triggered JK flip-flop with gated inputs, direct S_1 and S_2 inputs, and complementary Q_1 and Q_2 outputs. It is suited for medium and high speed applications. In systems where input gating is required, its use can lead to a lower package count and reduced system power dissipation. Input information is transferred to the outputs in time with the positive-going edge of the trigger pulse. Direct-coupled input triggering occurs as soon as the trigger pulse reaches a fixed threshold voltage; thereafter the gated inputs are locked out.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

t_n		t_{n+1}
J*	K**	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

* $J = J_1 \cdot J_2 \cdot \overline{J_3}$

** $K = \overline{K_1} \cdot K_2 \cdot K_3$

S_1 and S_2 function can only occur when T is LOW.

H=HIGH state (the more positive voltage)

L=LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0 V
Input voltage	V_J, V_K, V_T, V_S	max.	5.5 V[1]
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2 V[2]
Storage temperature	T_{stg}		−55 to +150 °C
Operating ambient temperature	T_{amb}		0 to +70 °C

1) In addition the input voltage between any two J inputs or between any two K inputs: max. 5.5 V.

2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

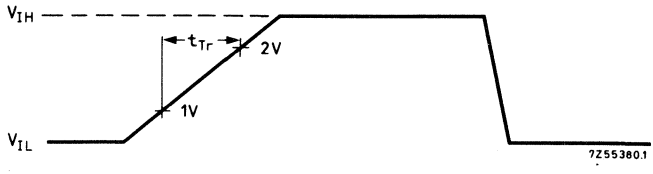
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$
Currents							
Input LOW (T, J, K)	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I=V_{QLmax}$; $I_Q=0$
Input HIGH (T, J, K)	I_{IHmax}	40	40	40	μA	5.25	$V_I=V_{QHmin}$; $I_Q=0$
Input LOW (S)	$-I_{SLmax}$	3.2	3.2	3.2	mA	5.25	$V_S=V_{QLmax}$; $I_Q=0$
Input HIGH (S)	I_{SHmax}	80	80	80	μA	5.25	$V_S=V_{QHmin}$; $I_Q=0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_I=0$; $V_Q=0$
	$-I_{Qscmax}$	57	57	57	mA	5.25	$V_I=0$; $V_Q=0$

CHARACTERISTICS (continued)

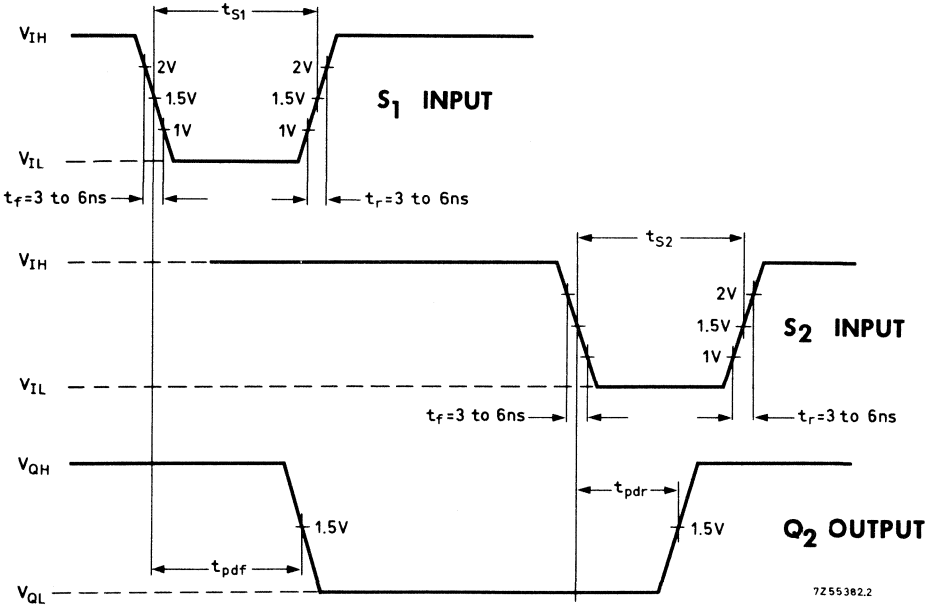
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	13	13	13	mA	5.0	I_Q=0
		<	26	26	26	mA	5.0	
DYNAMIC DATA								
Signal requirements								
Rise time (T input)	t_{Tr}	<	-	150	-	ns	5.0	
Pulse duration (T input)	t_{TH}	>	-	20	-	ns	5.0	
Pulse duration (S input)	t_{SL}	>	-	25	-	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	<	-	50	-	ns	5.0	N=10
Fall propagation delay time (S→Q)	t_{pdf}	<	-	50	-	ns	5.0	N=10
Rise propagation delay time (T→Q)	t_{pdr}	>	-	10	-	ns	5.0	N=10
	t_{pdr}	typ.	-	27	-	ns	5.0	
	t_{pdr}	<	-	50	-	ns	5.0	
Fall propagation delay time (T→Q)	t_{pdf}	>	-	10	-	ns	5.0	N=10
	t_{pdf}	typ.	-	18	-	ns	5.0	
	t_{pdf}	<	-	50	-	ns	5.0	
Set-up time (J_3, K_1)	$t_{su\,min}$	<	-	20	-	ns		
Hold time (J_1, J_2, K_2, K_3)	$t_{hold\,min}$	<	-	5	-	ns		
Preset time (S_1)	t_{S1}	>	-	25	-	ns		
Clear time (S_2)	t_{S2}	>	-	25	-	ns		
Maximum operating frequency	f	>	-	20	-	MHz	5.0	N=10
	f	typ.	-	35	-	MHz		

CHARACTERISTICS (continued)

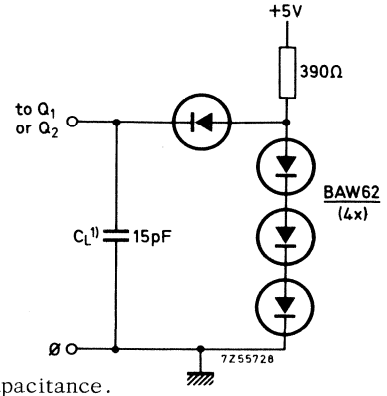
DYNAMIC DATA



Waveform illustrating trigger signal rise time



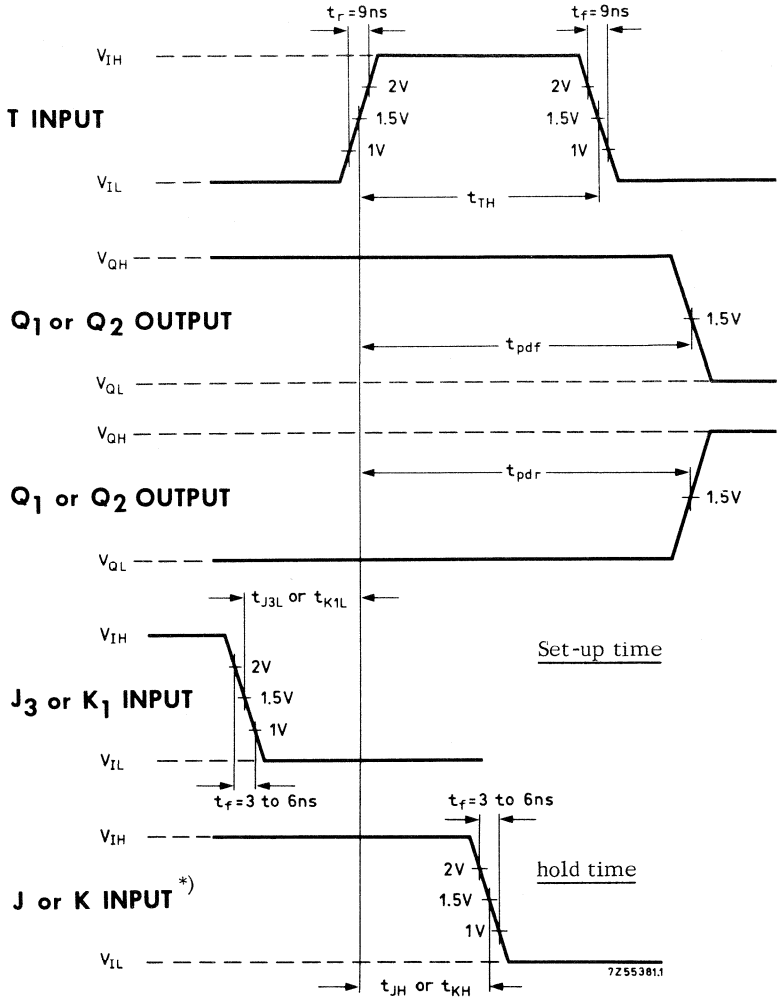
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.



1) Including probe and jig capacitance.

CHARACTERISTICS (continued)

DYNAMIC DATA



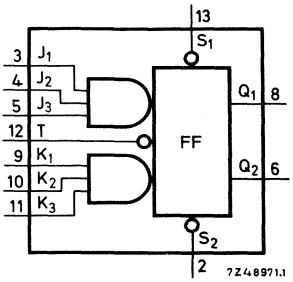
Waveform illustrating switching times.

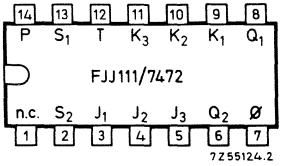
*) J = J_1 or J_2
K = K_2 or K_3

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE JK MASTER-SLAVE FLIP-FLOP (AND INPUTS)



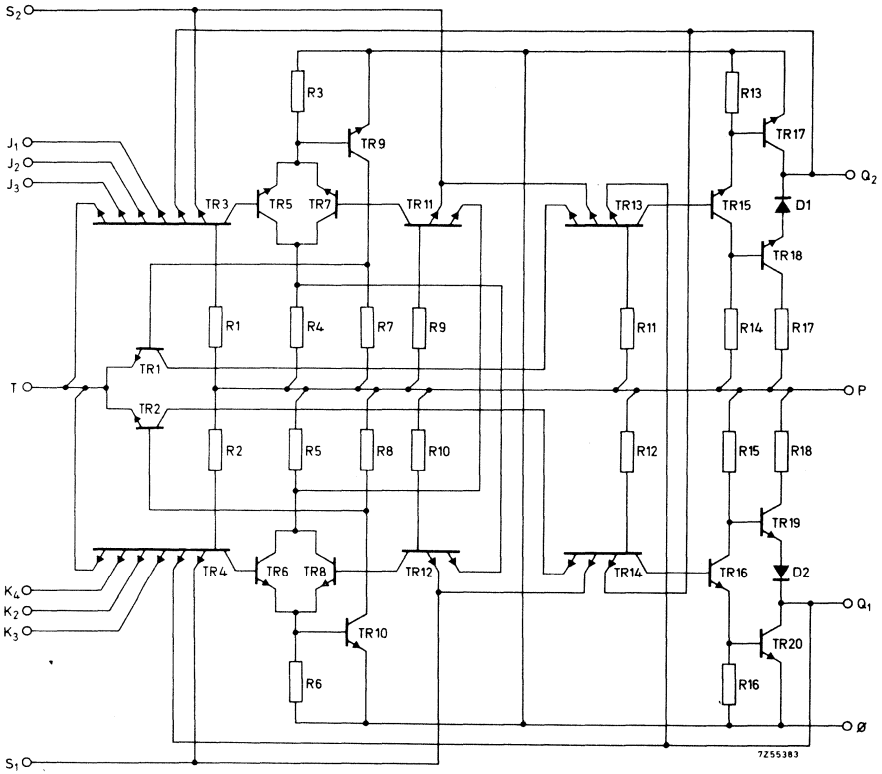


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
Max. operating frequency; T_{amb} = 25 °C	f	> 10	MHz
Average power consumption; T_{amb} = 25 °C	P_{av}	typ. 40	mW

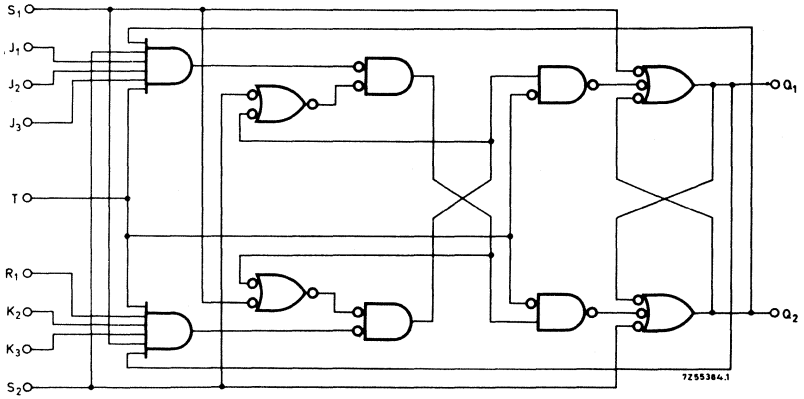
The FJJ111/7472 is a master-slave flip-flop having three J and three K input (AND function). The circuit operates at a frequency up to 15 MHz (typ.). The information at the J and K input enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n		t_{n+1}
J*	K**	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

*$J = J_1 . J_2 . J_3$

**$K = K_1 . K_2 . K_3$

S_1 and S_2 functions are independent of T.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	5.5	V [1]
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}		−55 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1] In addition the voltage between any two J inputs, or between any two K inputs: max. 5.5 V.

[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

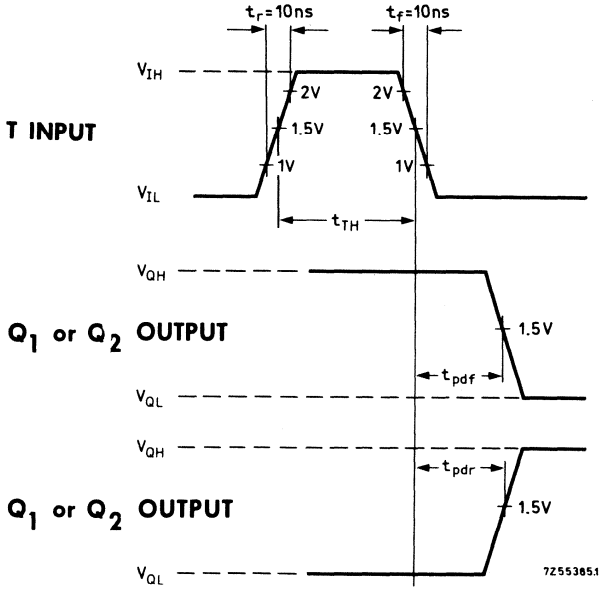
		T_{amb} (°C)				Conditions and references	
		0	25	75		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (J, K)	$-I_{JLmax}$ $-I_{KLmax}$	1.6	1.6	1.6	mA	5.25	$V_{JK}=V_{QLmax}$; $I_Q=0$
Input HIGH (J, K)	I_{JHmax} I_{KHmax}	40	40	40	μA	5.25	$V_{JK}=V_{QHmin}$; $I_Q=0$
Input LOW (S, T)	$-I_{SLmax}$ $-I_{TLmax}$	3.2	3.2	3.2	mA	5.25	$V_{ST}=V_{QLmax}$; $I_Q=0$
Input HIGH (S, T)	I_{SHmax} I_{THmax}	80	80	80	μA	5.25	$V_{ST}=V_{QHmin}$; $I_Q=0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	I_{QHmax}	0.4	0.4	0.4	mA		
Output short circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_I=0$; $V_Q=0$
	$-I_{Qscmax}$	57	57	57	mA		

CHARACTERISTICS (continued)

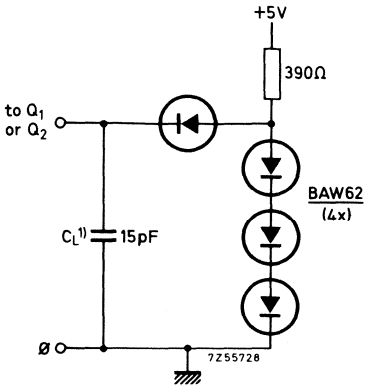
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	8	8	8	mA	5.0	
		<	20	20	20	mA	5.0	
DYNAMIC DATA								
Signal requirements								
Pulse duration (T input)	t_{TH}	>	–	20	–	ns	5.0	
Pulse duration (S input)	t_{SL}	>	–	25	–	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	typ.	–	16	–	ns	5.0	N = 10
	t_{pdr}	<	–	25	–	ns		
Fall propagation delay time (S→Q)	t_{pdf}	typ.	–	25	–	ns	5.0	N = 10
	t_{pdf}	<	–	40	–	ns		
Rise propagation delay time (T→Q)	t_{pdr}	>	–	10	–	ns	5.0	N = 10
	t_{pdr}	typ.	–	16	–	ns		
	t_{pdr}	<	–	25	–	ns		
Fall propagation delay time (T→Q)	t_{pdf}	>	–	10	–	ns	5.0	N = 10
	t_{pdf}	typ.	–	25	–	ns		
	t_{pdf}	<	–	40	–	ns		
Set-up time	t_{su}	>	–	0	–	ns		
Clear time	t_c	>	–	25	–	ns		
Maximum operating frequency	f	>	–	10	–	MHz	5.0	N = 10
		typ.	–	15	–	MHz		

CHARACTERISTICS (continued)

DYNAMIC DATA



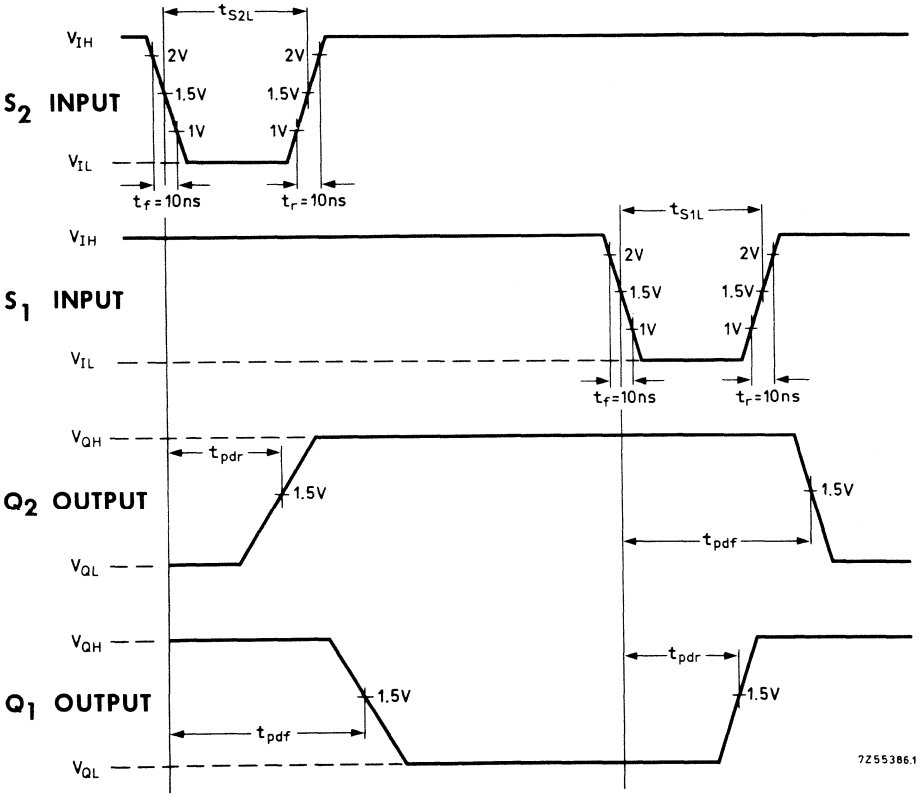
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.



[1]) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms illustrating switching times.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

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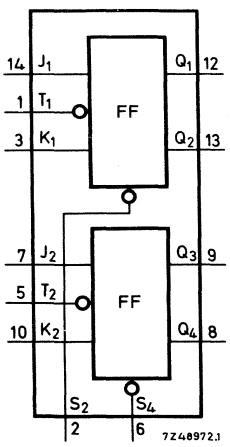
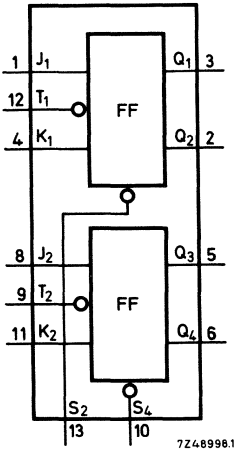
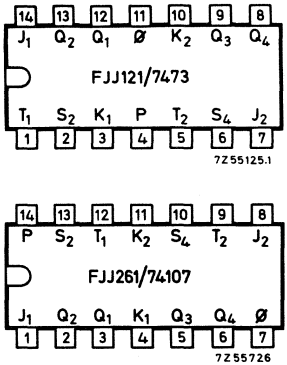
DUAL JK MASTER-SLAVE FLIP-FLOP



FJJ121/7473



FJJ261/74107

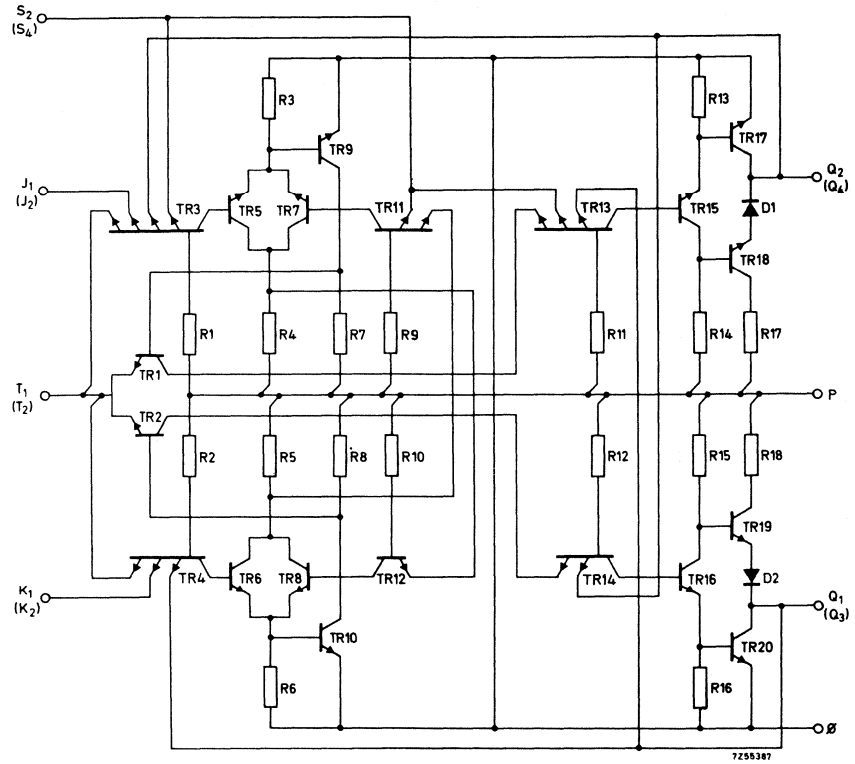


QUICK REFERENCE DATA				
Supply voltage	V_P	5.0 ± 5%		V
Operating ambient temperature range	T_{amb}	0 to +70		°C
Available d.c. fan-out (full temperature range)	N_a	⩾	10	
Max. operating frequency; T_{amb} = 25 °C	f	>	10	MHz
Average power consumption; T_{amb} = 25 °C (per flip-flop)	P_{av}	<	40	mW

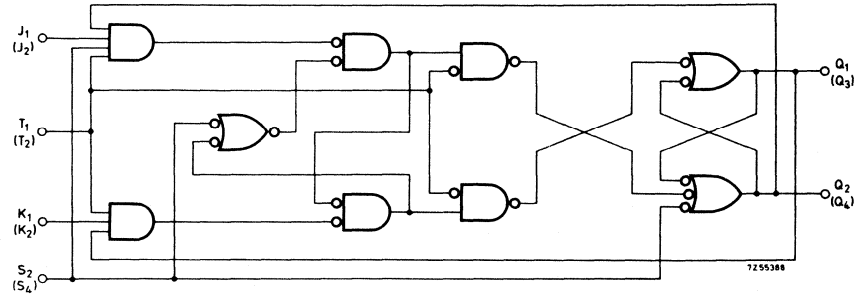
The FJJ121/7473 comprises two independent flip-flops, each provided with one J and one K input and based on the master-slave principle. The circuits operate at a frequency up to 15 MHz (typ.). The information at the J and K inputs enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs. The FJJ261/74107 is electrically identical to the FJJ121/7473 but has power supply and ground on corner pins. (7 and 14)

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n		t_{n+1}
J	K	Q_1 (Q_3)
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

S_2 and S_4 functions are independent of T_1 and T_2.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_J, V_K, V_S, V_T	max.	5.5	V
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2	V [1]
Storage temperature	T_{stg}		−55 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (J,K)	$-I_{JLmax}$ $-I_{KLmax}$	1.6	1.6	1.6	mA	5.25	$V_{JK}=V_{QLmax}$; $I_Q=0$
Input HIGH (J,K)	I_{JHmax} I_{KHmax}	40	40	40	μA	5.25	$V_{JK}=V_{QHmin}$; $I_Q=0$
Input LOW (S,T)	$-I_{SLmax}$ $-I_{TLmax}$	3.2	3.2	3.2	mA	5.25	$V_{ST}=V_{QLmax}$; $I_Q=0$
Input HIGH (S,T)	I_{SLmax} I_{TLmax}	80	80	80	μA	5.25	$V_{ST}=V_{QHmin}$; $I_Q=0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_I=0$; $V_Q=0$
	$-I_{Qscmax}$	57	57	57	mA	5.25	$V_I=0$; $V_Q=0$

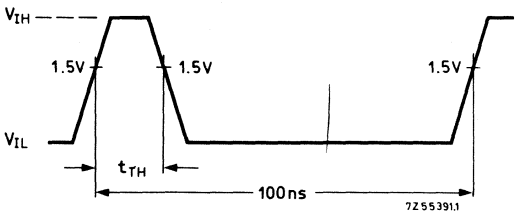
CHARACTERISTICS (continued)

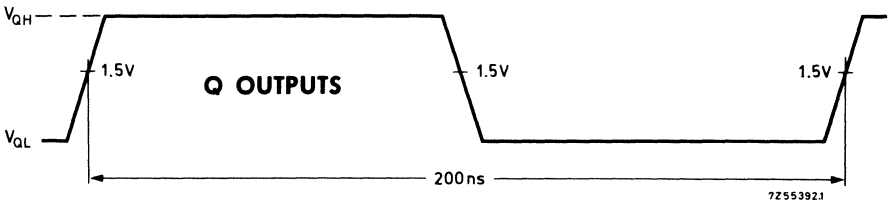
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	16	16	16	mA	5.0	
		<	40	40	40	mA	5.0	
DYNAMIC DATA								
Signal requirements								
Pulse duration (T input)	t_{TH}	>	–	20	–	ns	5.0	
Pulse duration (S input)	t_{SL}	>	–	25	–	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	typ.	–	16	–	ns	5.0	N = 10
	t_{pdr}	<	–	25	–	ns		
Fall propagation delay time (S→Q)	t_{pdf}	typ.	–	25	–	ns	5.0	N = 10
	t_{pdf}	<	–	40	–	ns		
Rise propagation delay time (T→Q)	t_{pdr}	>	–	10	–	ns	5.0	N = 10
	t_{pdr}	typ.	–	16	–	ns		
	t_{pdr}	<	–	25	–	ns		
Fall propagation delay time (T→Q)	t_{pdf}	>	–	10	–	ns	5.0	N = 10
	t_{pdf}	typ.	–	25	–	ns		
	t_{pdf}	<	–	40	–	ns		
Set-up time	t_{su}	>	–	0	–	ns		
Clear time (S_2 or S_4)	t_S	>	–	25	–	ns		
Maximum operating frequency	f	>	–	15	–	MHz	5.0	N = 10
		typ.	–	20	–	MHz		

CHARACTERISTICS (continued)

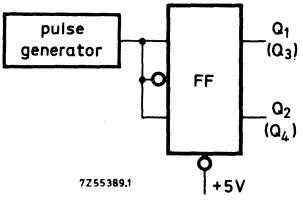
DYNAMIC DATA

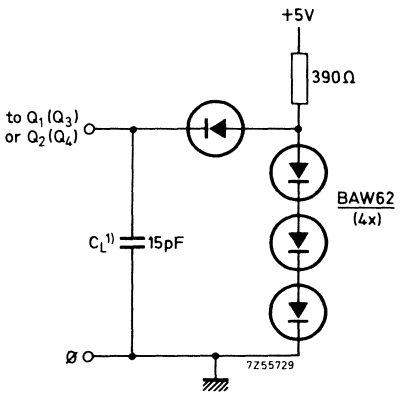
T, J, and K INPUTS





Waveforms illustrating in- and output pulses.



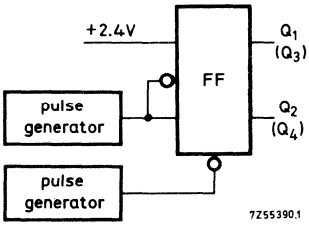


Equivalent load for N = 10

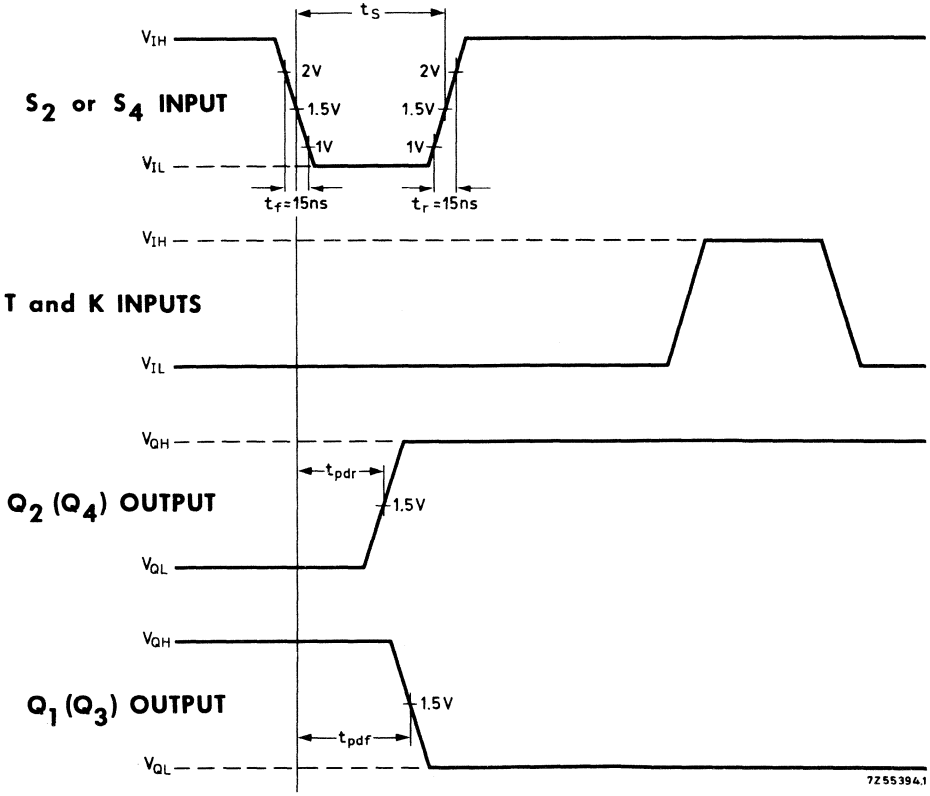
[1]) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA



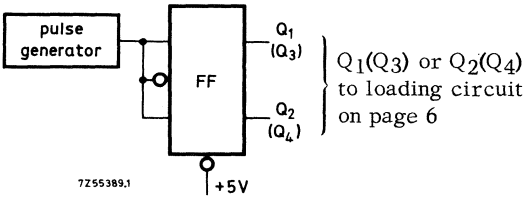
$Q_1(Q_3)$ or $Q_2(Q_4)$ to loading circuit on page 6

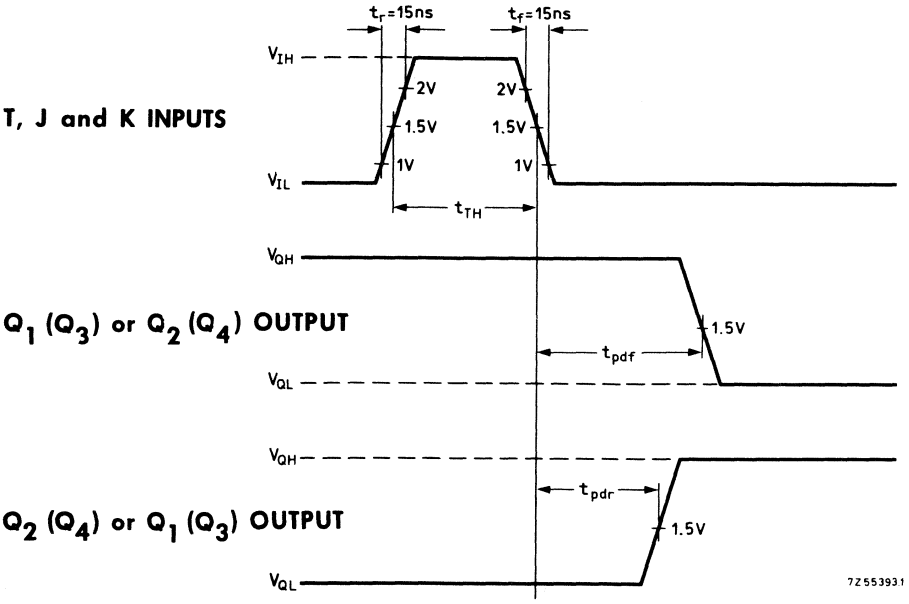


Waveforms illustrating measurement of t_{pdr} and t_{pdf}. (S→Q)

CHARACTERISTICS (continued)

DYNAMIC DATA



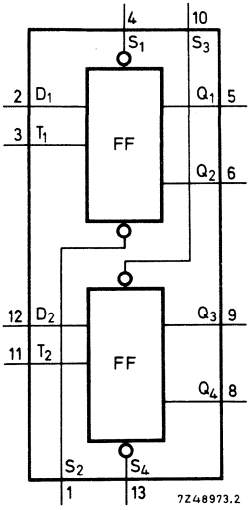


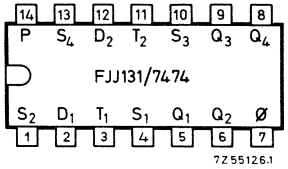
Waveforms illustrating measurement of t_{pdr} and t_{pdf}. (T→Q)

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



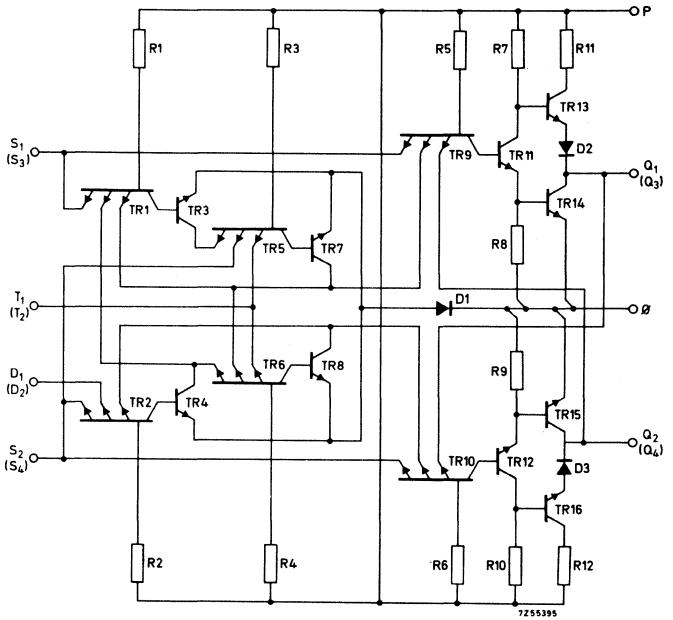


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
Max. operating frequency; T_{amb} = 25 °C	f	>	15	MHz
Average power consumption; T_{amb} = 25 °C (per flip-flop)	P_{av}	<	42.5	mW

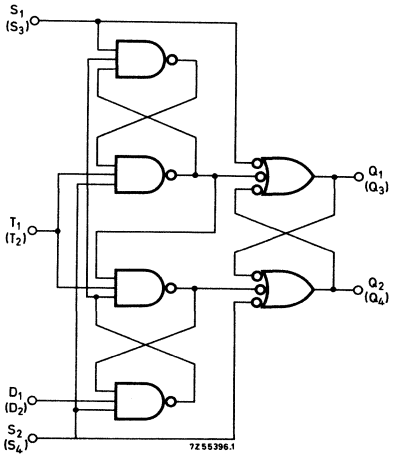
The FJJ131/7474 is an edge-triggered dual D-type flip-flop with direct SET inputs and complementary outputs. On the positive going edge of the clock pulse the information on the D input is transferred to Q_1 (or resp. Q_3).

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n	t_{n+1}	
D	Q_1	Q_2
L	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
Input voltage	V_D, V_S, V_T	max.	5.5	V
Peak negative input voltage (D, S, T)	$-V_M$	max.	2	V [1]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

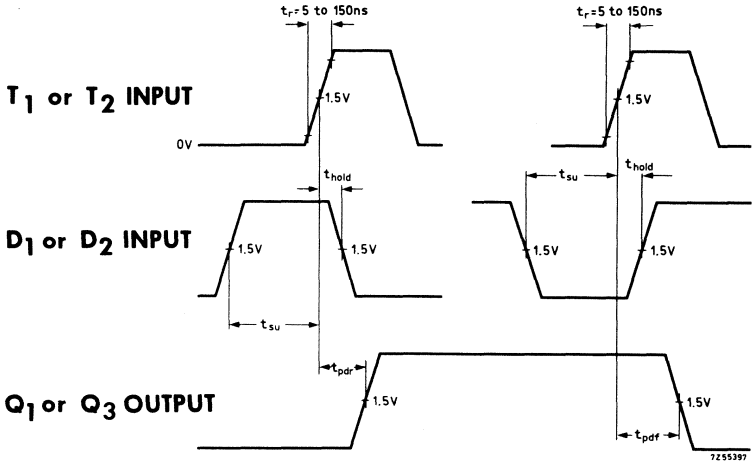
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (S_1,D_1)	$-I_{S1Lmax}$ $-I_{D1Lmax}$	1.6	1.6	1.6	mA	5.25	$V_{S1}, V_{D1}=V_{QLmax}$
Input LOW (S_2,T_1)	$-I_{S2Lmax}$ $-I_{T1Lmax}$	3.2	3.2	3.2	mA	5.25	$V_{S2}, V_{T1}=V_{QLmax}$
Input HIGH (D)	I_{DHmax}	40	40	40	µA	5.25	$V_D = V_{QHmin}$
Input HIGH (S_1,T_1)	I_{S1Hmax} I_{T1Hmax}	80	80	80	µA	5.25	$V_{S1}, V_{T1}=V_{QHmin}$
Input HIGH (S_2)	I_{S2Hmax}	120	120	120	µA	5.25	$V_{S2} = V_{QHmin}$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_Q = 0$
	$-I_{Qscmax}$	57	57	57	mA	5.25	$V_Q = 0$

CHARACTERISTICS (continued)

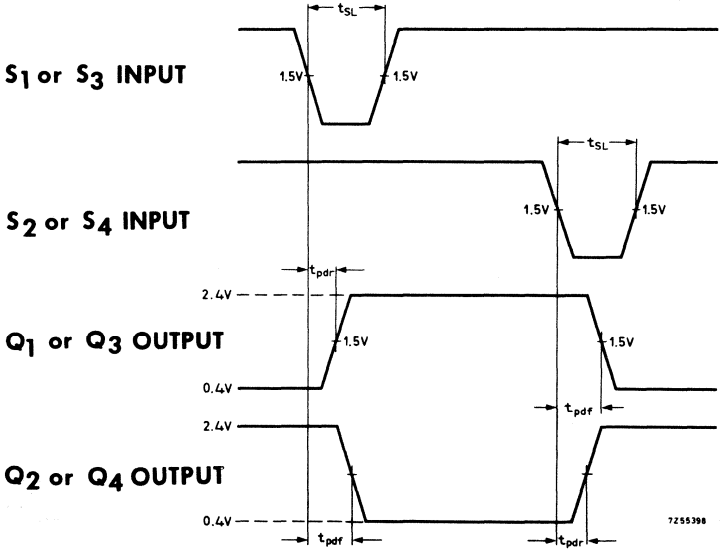
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	17	17	17	mA	5.0	V_I = 5.0 V
		<	30	30	30	mA	5.0	
DYNAMIC DATA								
Signal requirement								
Pulse duration (S, T input)	t_{SL}, t_{TL}	>	30	30	30	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	<	–	25	–	ns	5.0	N = 10
Fall propagation delay time (S→Q)	t_{pdf}	<	–	40	–	ns	5.0	N = 10
Rise propagation delay time (T→Q)	t_{pdr}	>	–	10	–	ns	5.0	N = 10
		typ.	–	14	–	ns		
		<	–	25	–	ns		
Fall propagation delay time (T→Q)	t_{pdf}	>	–	10	–	ns	5.0	N = 10
		typ.	–	20	–	ns		
		<	–	50	–	ns		
Set-up time	t_{su}	>	–	20	–	ns		
Hold time	t_{hold}	>	–	5	–	ns		
Maximum operating frequency	f	>	–	15	–	MHz	5.0	N = 10
		typ.	–	25	–	MHz		

CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms illustrating set-up and hold times.

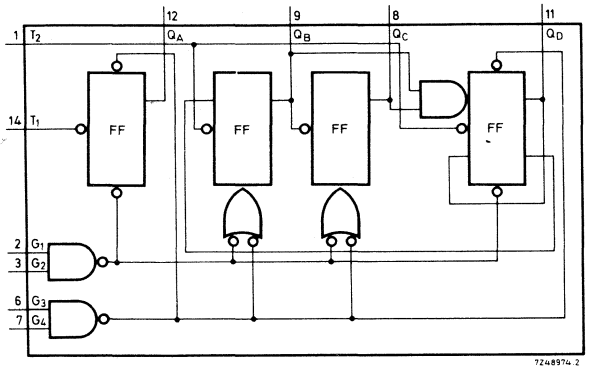


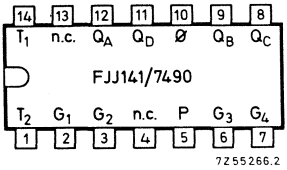
Waveforms illustrating measurement of t_{pdr} and t_{pdf} (S→Q)

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

BCD DECADE COUNTER



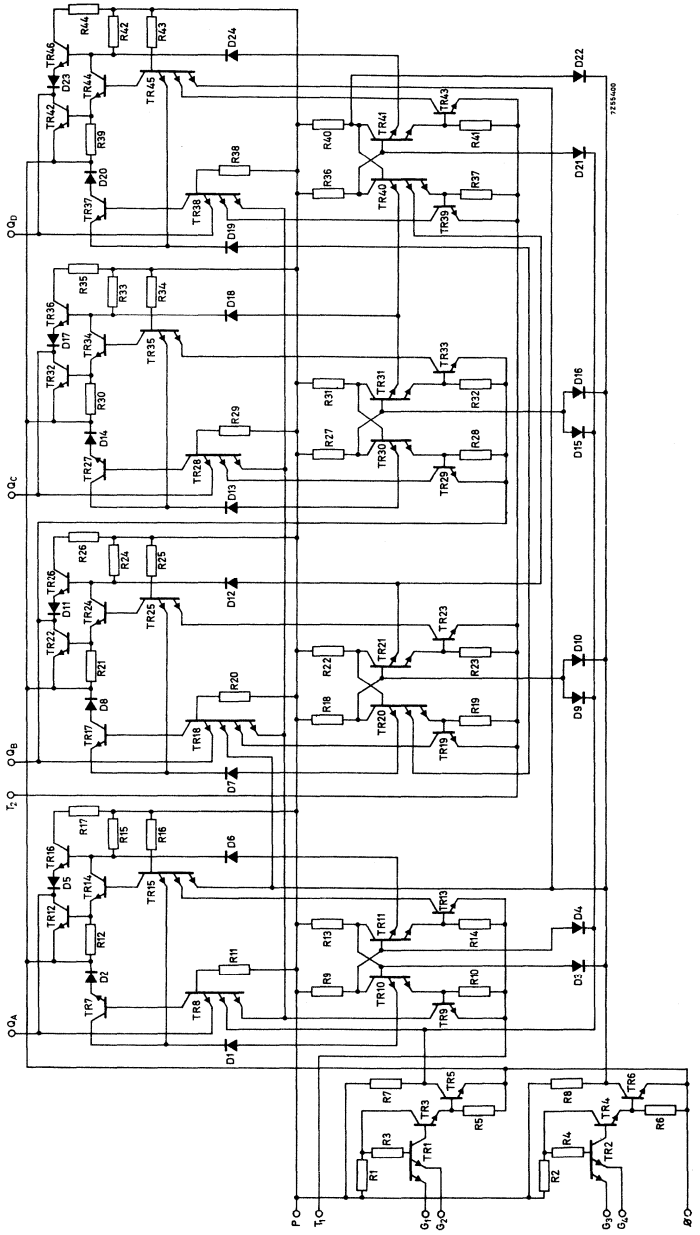


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Max. operating frequency; T_{amb} = 25°C	f_c	≥ 10	MHz
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
Average power consumption T_{amb} = 25 °C	P_{av}	typ. 160	mW

The FJJ141/7490 is a high speed decade counter, consiting of 4 master-slave flip-flops. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical zero (inputs G_1, G_2) or to a binary coded (BCD) count of nine (inputs G_3, G_4).

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

As the output Q_A from the first flip-flop is not internally connected to the succeeding stages, the counter can be used in three different modes.

1. Binary coded decimal decade counter: the T_2 input must be externally connected to the Q_A output. T_1 is then the counter input.
2. Symmetrical divide-by-ten counter for frequency synthesizer or other applications requiring division of a binary count by the power of ten: the Q_D output must be connected to the T_1 input. In this case T_2 becomes counter input and a divide-by-ten square wave is obtained at output Q_A.
3. Divide-by-two counter and a divide-by-five counter: no external interconnections are required.

FUNCTION TABLES

BCD count sequence (output Q_A connected to input T_2)

Count	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Reset/count

RESET INPUTS				OUTPUTS			
G_1	G_2	G_3	G_4	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	L	H	H	H	L	L	H
L	X	H	H	H	L	L	H
X	L	X	L	no change			
L	X	L	X	no change			
L	X	X	L	no change			
X	L	L	X	no change			

H=HIGH state (the more positive voltage)
L=LOW state (the less positive voltage)
X=state is immaterial

G_1 and G_2 are "preset 0" inputs (reset all Q outputs to LOW)
G_3 and G_4 are "preset 9" inputs (set Q_A and Q_D to HIGH and reset Q_B and Q_C to LOW to provide BCD 9 count for nine complement applications)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
T input voltage	V_T	max.	5.5	V
G input voltage	V_G	max.	5.5	V
Duration of negative transient input voltage of 2 V $R_S \geq 75\ \Omega$; f = 5.0 MHz	t_p	max.	20	ns
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

CHARACTERISTICS

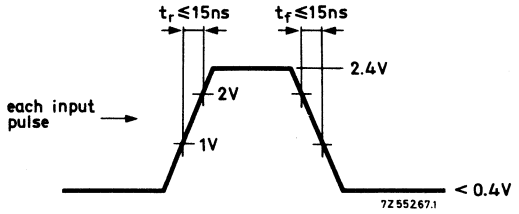
		T_{amb} (°C)				Conditions and References	
		0	25	75		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH all inputs except T_2	V_{IHmin}	2.0	2.0	2.0	V		
T_2 input	V_{T2Hmin}	2.2	2.2	2.2	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (G input)	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_I = 0.4$ V
Input HIGH (G input)	I_{GHmax}	40	40	40	μA	5.25	$V_I = 2.4$ V
Input LOW (T_1 input)	$-I_{T1Lmax}$	3.2	3.2	3.2	mA	5.25	$V_I = 0.4$ V
Input HIGH (T_1 input)	I_{T1Hmax}	80	80	80	μA	5.25	$V_I = 2.4$ V
Input LOW (T_2 input)	$-I_{T2Lmax}$	6.4	6.4	6.4	mA	5.25	$V_I = 0.4$ V
Input HIGH (T_2 input)	I_{T2Hmax}	160	160	160	μA	5.25	$V_I = 2.4$ V
Output LOW	I_{QLmax}	16	16	16	mA	4.75	
Output short-circuited [1]	$-I_{Qscmin}$	18	18	18	mA	5.25	
	$-I_{Qscmax}$	57	57	57	mA	5.25	
SUPPLY DATA							
Supply current	I_P typ.	32	32	32	mA	5.0	$V_I = 4.5$ V
	<	53	53	53	mA	5.0	
DYNAMIC DATA							
Signal requirements							
Pulse duration (G inputs)	t_{GH} >	–	50	–	ns	5.0	
	t_{GL} >	–	50	–	ns	5.0	
Pulse duration (T inputs)	t_{TH} >	–	50	–	ns	5.0	
	t_{TL} >	–	50	–	ns	5.0	
Performance							
Rise propagation [2] delay time ($T_1 \rightarrow Q_C$)	t_{pdr} typ.	–	60	–	ns	5.0	
	<	–	100	–	ns	5.0	
Fall propagation [2] delay time ($T_1 \rightarrow Q_C$)	t_{pdf} typ.	–	60	–	ns	5.0	
	<	–	100	–	ns	5.0	
Maximum counting frequency	f >	–	10	–	MHz	5.0	
	typ.	–	18	–	MHz	5.0	

1) Do not short circuit more than one output at a time.

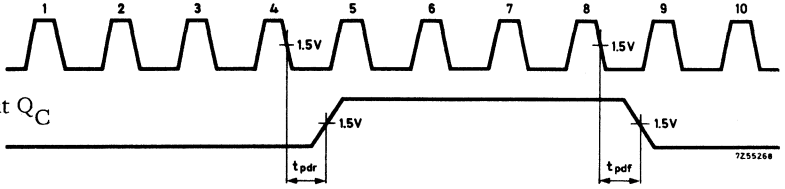
2) All four outputs loaded, Q_A output connected to T_2 input, delay from T_1 input to Q_C output. (see also waveforms page 6).

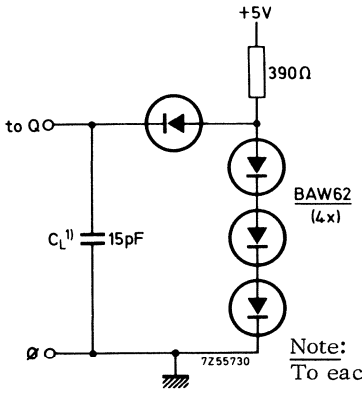
CHARACTERISTICS (continued)

Input pulse



Input T_1 (Q_A output connected to T_2)





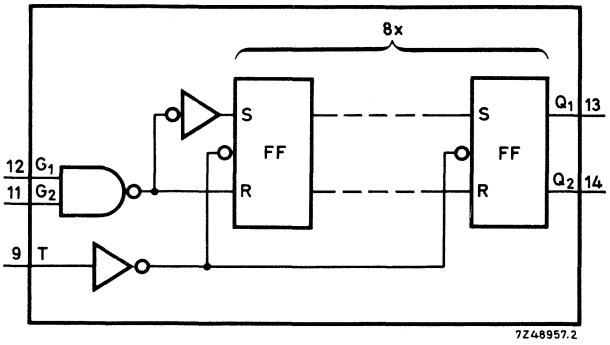
Note:
To each output the same loading circuit

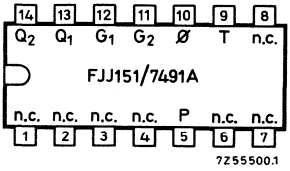
[1]) Including probe and jig capacitance

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

·Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices * it corresponds to the 74Nseries TTL.

8 BIT SHIFT REGISTER

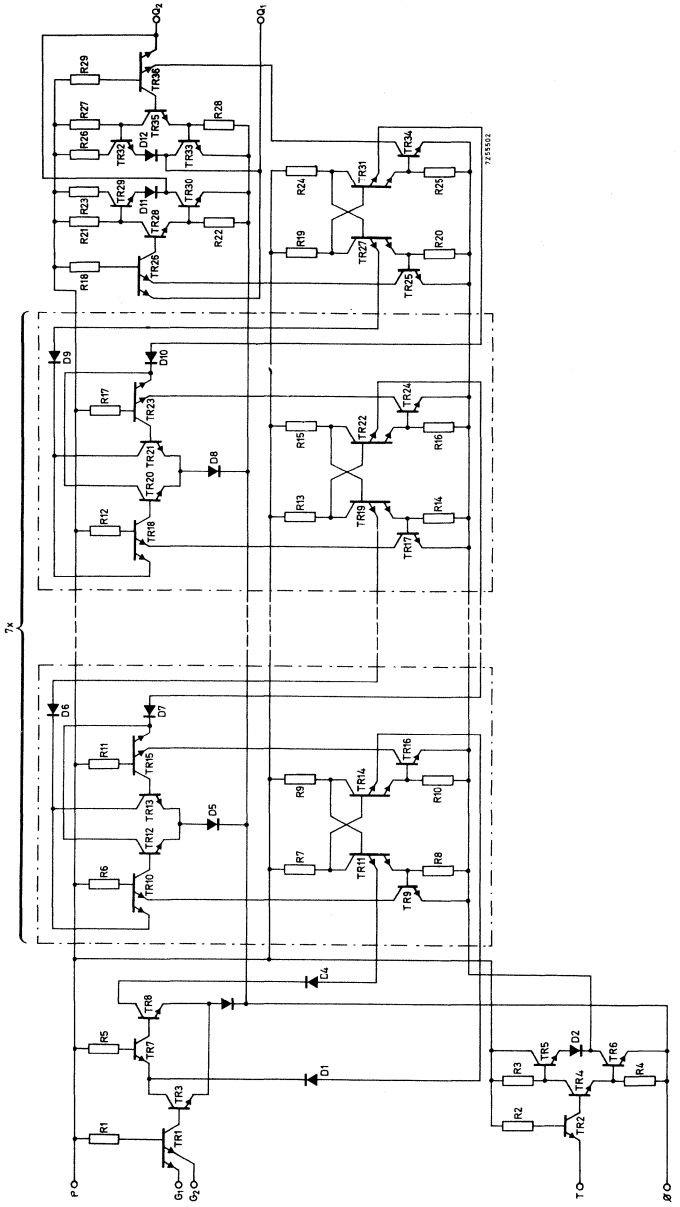




QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Max. shift frequency	f	10	MHz
Available d.c. fan-out (full temperature range)	N_a	10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Total power dissipation	P_{tot}	typ. 175	mW

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



The FJJ151 is a serial input, serial-ouput 8-bit shift register with complementary outputs. It consists of eight RS master-slave flip-flops, a two-input NAND gate, and a clock driver. Inputs G_1 and G_2 go to an AND gate; either one or both inputs may be used. If only one is used, the other must be kept in the HIGH state.
When the T input is HIGH, information at the input of each stage is shifted to the next; thus, information at the G_1 or G_2 input is transferred to the Q_1 or Q_2 output after 8 clock pulses.
The FJJ151 corresponds to the SN7491AN.

LOGIC FUNCTION

Function table

t_n		t_{n+8}
G_1	G_2	Q_1
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+8} = bit time after 8 trigger pulses

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages	V_P	max.	7.0	V
Input voltages	$V_{G1}; V_{G2}; V_T$	max.	5.5	V [1]
Peak negative input voltage (G_1, G_2, T)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition the voltage between any two inputs must not exceed 5.5 V.
[2]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C) 0	25	70	Conditions and References: V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8 V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$
Currents						
Input LOW; G_1	$-I_{G1Lmax}$	1.6	1.6	1.6 mA	5.25	$V_I = 0.4$ V
G_2	$-I_{G2Lmax}$	1.6	1.6	1.6 mA	5.25	
T	$-I_{TLmax}$	1.6	1.6	1.6 mA	5.25	
Input HIGH; G_1	I_{G1Hmax}	40	40	40 μA	5.25	$V_I = 2.4$ V
G_2	I_{G2Hmax}	40	40	40 μA	5.25	
T	I_{THmax}	40	40	40 μA	5.25	
G_1	I_{G1Hmax}	1.0	1.0	1.0 mA	5.25	$V_I = 5.5$ V
G_2	I_{G2Hmax}	1.0	1.0	1.0 mA	5.25	
T	I_{THmax}	1.0	1.0	1.0 mA	5.25	
Output LOW	I_{QLmax}	16	16	16 mA		$V_Q = V_{QLmax}$
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4 mA		$V_Q = V_{QHmin}$
Output short circuited (see note 1)	$-I_{Qscmin}$	18.0	18.0	18.0 mA	5.25	$V_Q = 0$
	$-I_{Qscmax}$	55.0	55.0	55.0 mA	5.25	
SUPPLY DATA						
Supply current; HIGH input G_1; G_2; T	I_{PH} typ.	35	35	35 mA	5.0	
	I_{PH} <	60	60	60 mA	5.0	

Note 1: Not more than one output should be short circuited at a time.

CHARACTERISTICS

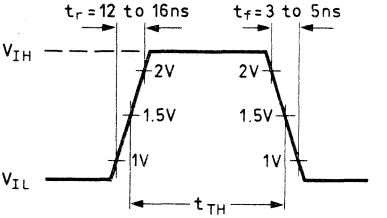
			T_{amb} (°C)				Conditions and References	
			0	25	70		V_P (V)	
DYNAMIC DATA								
Performance								
Rise propagation delay time (T►Q) (see note 1)	t_{pdr}	typ.	–	24	–	ns	5.0	
	t_{pdr}	≤	–	40	–	ns	5.0	
Fall propagation delay time (T►Q) (see note 1)	t_{pdf}	typ.	–	27	–	ns	5.0	
	t_{pdf}	≤	–	40	–	ns	5.0	
Signal requirements								
Set-up time for G_1; G_2 inputs HIGH	t_{suH}	≥	–	25	–	ns	5.0	
LOW	t_{suL}	≥	–	25	–	ns	5.0	
Clock pulse width	t_{TH}	>	–	25	–	ns	5.0	
G_1; G_2 input width	t_{GH}	>	–	25	–	ns	5.0	
Hold time	t_{hold}	≥	–	0	–	ns	5.0	
Maximum operating shift frequency	f	≥	–	10	–	MHz	5.0	

Note 1: Refers to propagation delay from seventh bit to output stage.

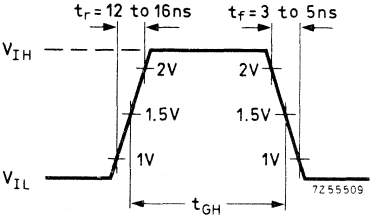
CHARACTERISTICS (continued)

DYNAMIC DATA

T INPUT



$G_1 \cdot G_2$ INPUT

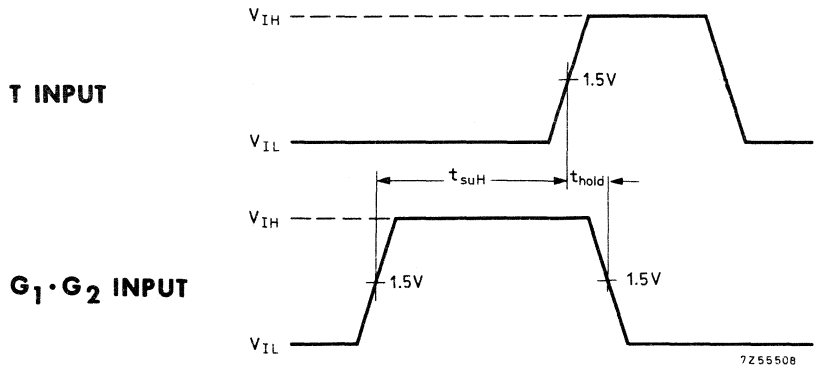


Waveforms illustrating input signals

CHARACTERISTICS (continued)

DYNAMIC DATA

In general case

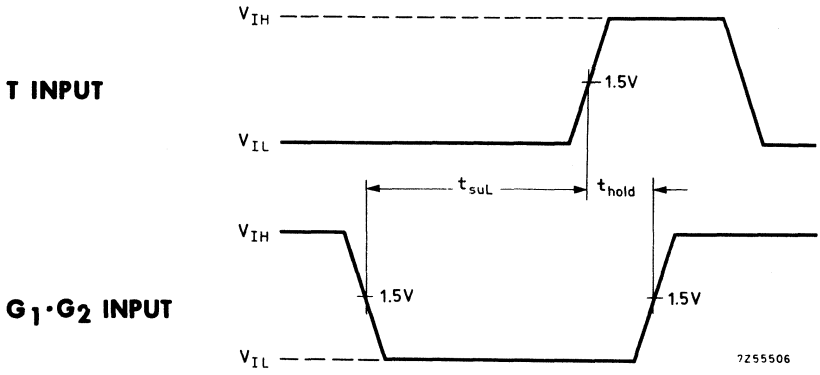


Waveforms illustrating measurement of set-up and hold times to guarantee shifting operation, for HIGH logic level.

CHARACTERISTICS (continued)

DYNAMIC DATA

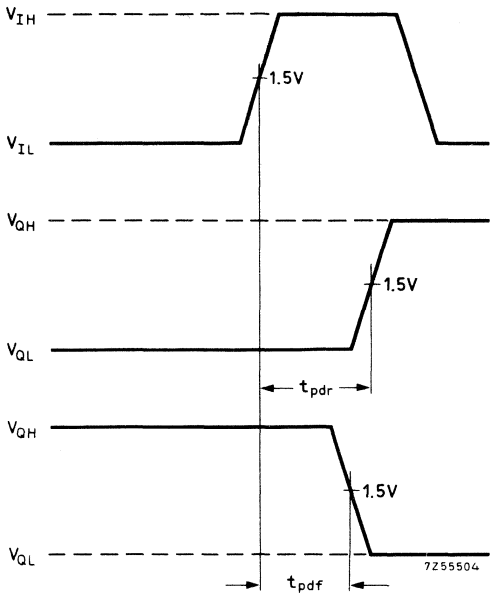
In general case



Waveforms illustrating measurement of set-up and hold times to guarantee shifting operation, for LOW logic level.

CHARACTERISTICS (continued)

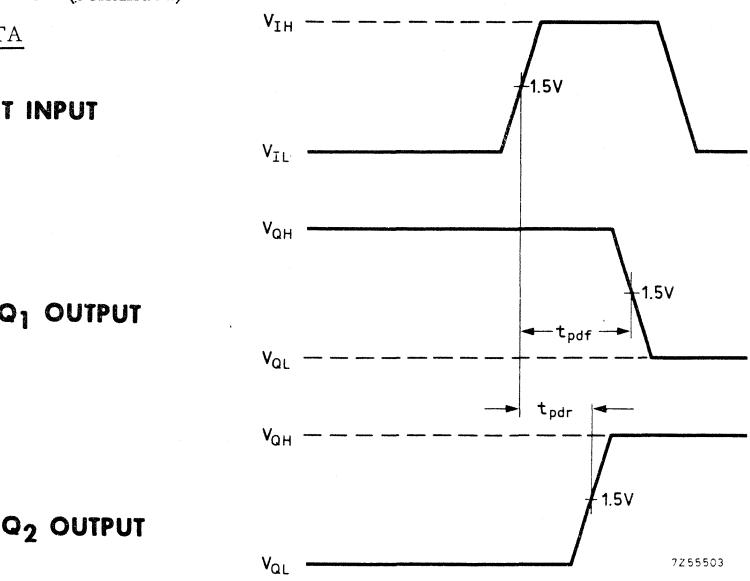
DYNAMIC DATA



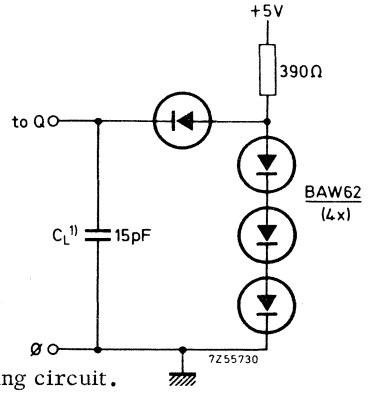
Waveforms illustrating measurement of t_{pdr} and t_{pdf} if S input of eight bit at logic HIGH level is 25 ns prior to rising edge of T input. (t_{hold} = 0 ns)

CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms illustrating measurement of t_{pdr} and t_{pdf} if S input of eight bit at logic LOW level is 25 ns prior to rising edge of T input (t_{hold} = 0 ns).



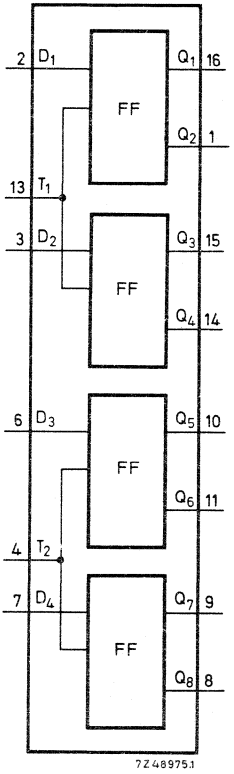
To output Q_2 the same loading circuit.

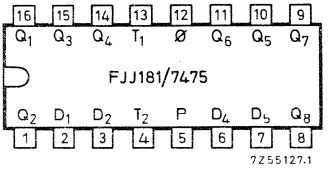
1) Including probe and jig capacitance

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

QUADRUPLE LATCH D FLIP-FLOP



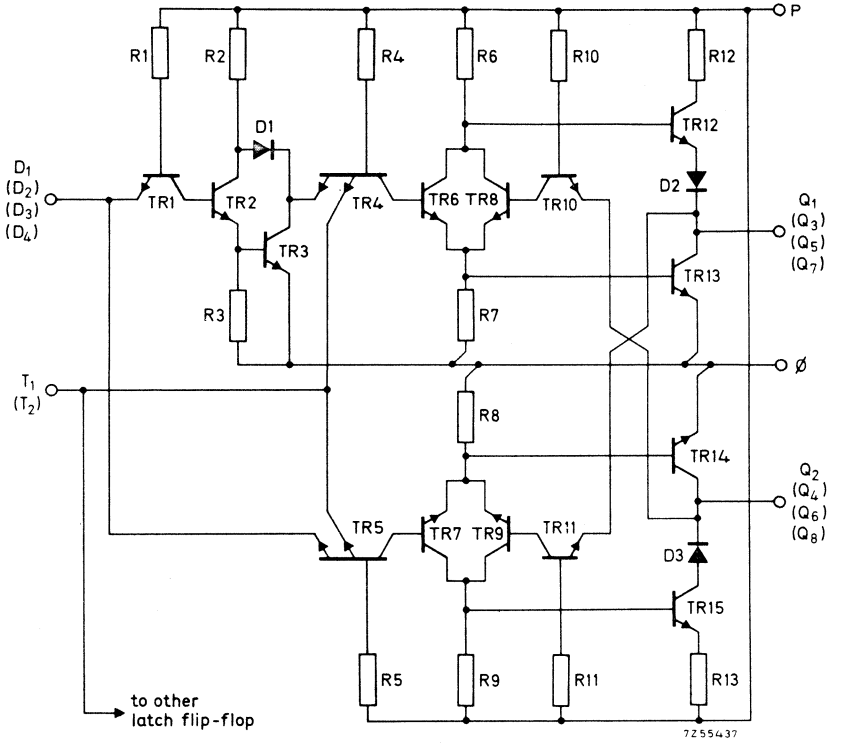


PACKAGE OUTLINE:

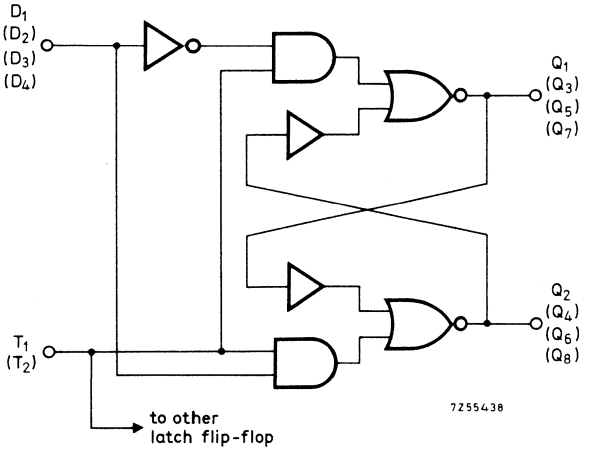
16 lead plastic dual in-line (type A) (See General Section)

QUICK REFERENCE DATA			
Supply voltage	V_p	5.0 ±5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 160	mW

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

Information present at a data input is transferred to the Q output. For so long as the trigger input is HIGH, the Q output will follow the data input. When the trigger goes LOW, the information present at the data input at the time of transition is retained at the Q output until the trigger again goes HIGH.

Function table (each gate)

t_n data input	t_{n+1} output Q
L	L
H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after rising edge of trigger pulse

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_D, V_T	max.	5.5	V [1]
Peak negative input voltage (D, T)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

1) In addition the voltage between any two input must not exceed 5.5 V.
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

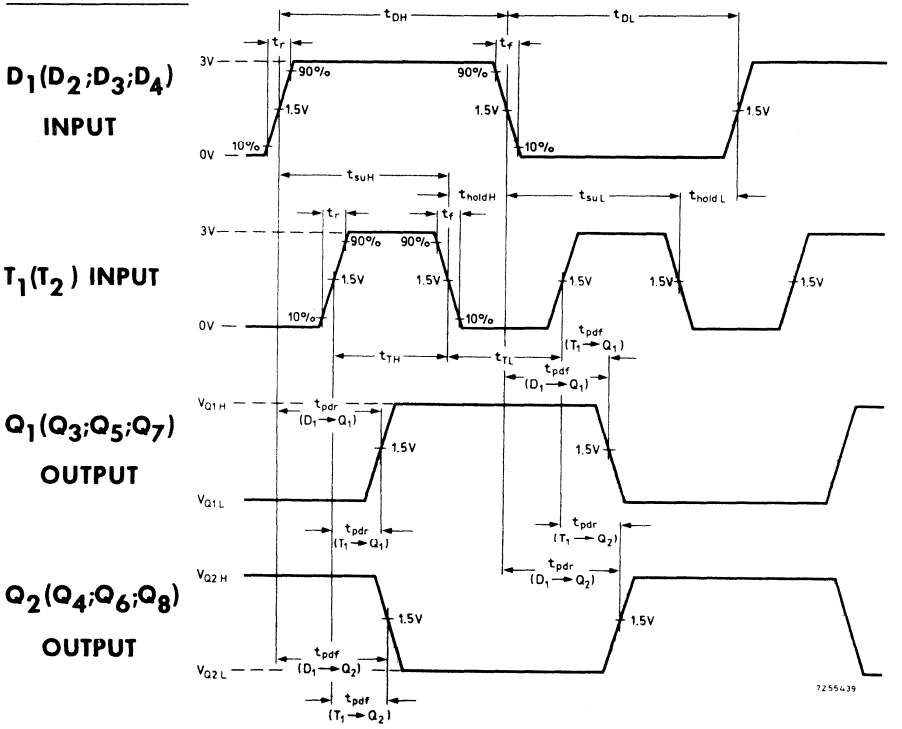
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (D)	$-I_{DLmax}$	3.2	3.2	3.2	mA	5.25	$V_D = V_{QLmax}$; $I_Q = 0$
Input HIGH (D)	I_{DHmax}	80	80	80	μA	5.25	$V_D = V_{QHmin}$; $I_Q = 0$
Input LOW (T)	$-I_{TLmax}$	6.4	6.4	6.4	mA	5.25	$V_T = V_{QLmax}$; $I_Q = 0$
Input HIGH (T)	I_{THmax}	160	160	160	μA	5.25	$V_T = V_{QHmin}$; $I_Q = 0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output short circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	
	$-I_{Qscmax}$	57	57	57	mA		
SUPPLY DATA							
Supply current (total)	I_P typ.	32	32	32	mA	5.0	$V_T = V_D = 0$ V
	I_P <	53	53	53	mA	5.0	

CHARACTERISTICS

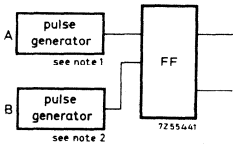
		T_{amb} (°C)	Conditions and References	
		0 25 70	V_p (V)	All these times at N = 10
DYNAMIC DATA				C_L = 15 pF; R_L = 400 Ω
Performance				
Set-up time				
D inputs:				
HIGH	t_{suH} typ.	– 7 – ns	5	
	t_{suH} <	– 20 – ns	5	
LOW	t_{suL} typ.	– 14 – ns	5	
	t_{suL} <	– 20 – ns	5	
Hold time				
D inputs:				
HIGH	$t_{hold\ H}$ typ.	– 15 – ns	5	
LOW	$t_{hold\ L}$ typ.	– 6 – ns	5	
Propagation delay times:				
Rise D→Q_1(Q_3; Q_5; Q_7)	t_{pdr} <	– 30 – ns	5	
Fall D→Q_1(Q_3; Q_5; Q_7)	t_{pdf} <	– 25 – ns	5	
Rise D→Q_2(Q_4; Q_6; Q_8)	t_{pdr} <	– 40 – ns	5	
Fall D→Q_2(Q_4; Q_6; Q_8)	t_{pdf} <	– 15 – ns	5	
Rise T_1→Q_1(Q_3) T_2→Q_5(Q_7)	t_{pdr} <	– 30 – ns	5	
Fall T_1→Q_1(Q_3) T_2→Q_5(Q_7)	t_{pdf} <	– 15 – ns	5	
Rise T_1→Q_2(Q_4) T_2→Q_6(Q_8)	t_{pdr} <	– 30 – ns	5	
Fall T_1→Q_2(Q_4) T_2→Q_6(Q_8)	t_{pdf} <	– 15 – ns	5	

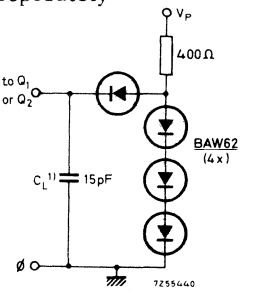
CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms inllustrating measurement of t_{pdr} and t_{pdf}.
Each latch D flip-flop is tested seperately





1) C_L includes probe and jig capacitance

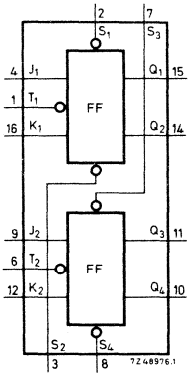
Notes:

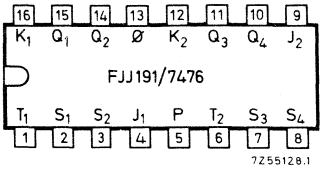
1. Pulse generator A: V_A = 3V; $t_r \leq 10$ ns; $t_f \leq 10$ ns; R_S = 50 Ω; $t_{DH} = t_{DL}$ = 1 μs; f = 500 kHz
2. Pulse generator B; V_B = 3 V; $t_r \leq 10$ ns; $t_f \leq 10$ ns; R_S = 50 Ω; $t_{TH} = t_{TL}$ = 500 ns; f = 1 MHz

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL JK MASTER-SLAVE FLIP-FLOP



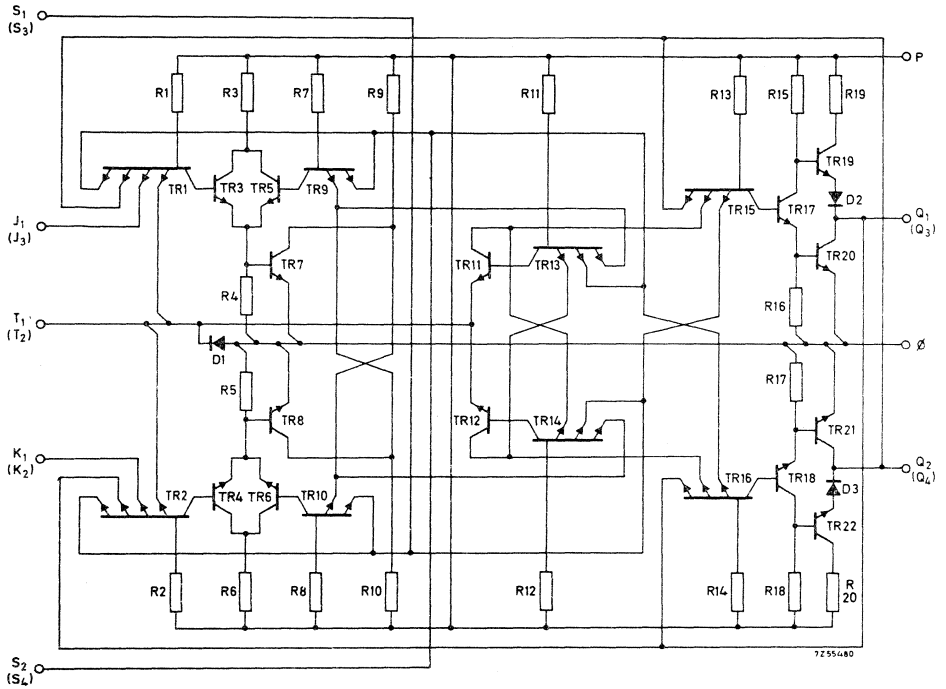


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Maximum operating frequency	f	≥ 15	MHz
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 80	mW

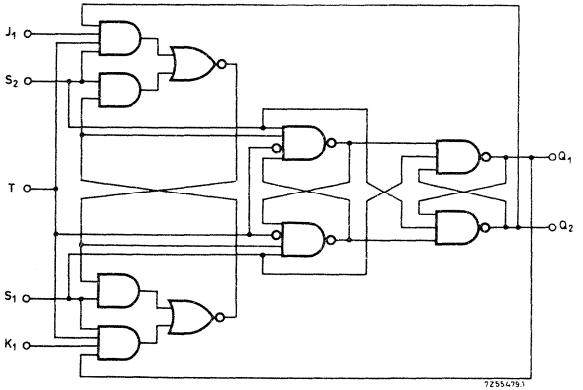
The FJJ191/7476 is a dual JK master-slave flip-flop having one J and one K input per flip-flop. The circuits operate at a frequency up to 15 MHz (typ.) The information at the J and K inputs enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs. The SET signals on S_1 and S_2 (S_3 and S_4) which override any other inputs, are active at the LOW level.

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

LOW input to $S_1(S_3)$ sets $Q_1(Q_3)$ to HIGH
LOW input to $S_2(S_4)$ sets $Q_1(Q_3)$ to LOW
} independent of trigger pulse

Function table for J and K inputs

t_n		t_{n+1}
J	K	Q_1
L	L	Q_{1n}
L	H	L
H	L	H
H	H	$\overline{Q_{1n}}$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after trigger pulse

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	5.5	V [1]
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

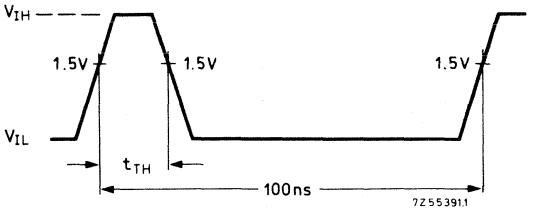
CHARACTERISTICS

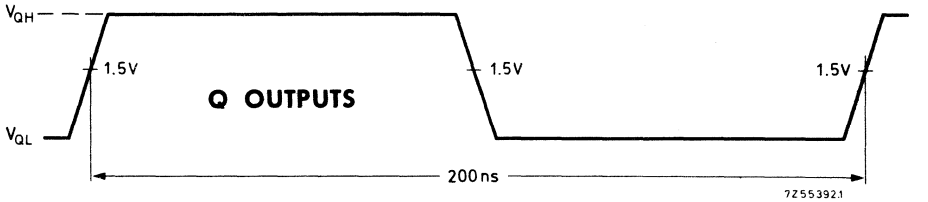
		T_{amb} (°C) 0	25	75		V_P (V)	Conditions and references
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (J, K)	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$; $I_Q = 0$
Input HIGH (J, K)	I_{IHmax}	40	40	40	μA	5.25	$V_I = V_{QHmin}$; $I_Q = 0$
Input LOW (S, T)	$-I_{SLmax}$	3.2	3.2	3.2	mA	5.25	$V_{S,T} = V_{QLmax}$; $I_Q = 0$
	$-I_{TLmax}$	3.2	3.2	3.2	mA		
Input HIGH (S, T)	I_{SHmax}	80	80	80	μA	5.25	$V_{S,T} = V_{QHmin}$; $I_Q = 0$
	I_{THmax}	80	80	80	μA		
Output LOW	I_{QL}	16	16	16	mA		
Output short circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_I = 0$; $V_Q = 0$
	$-I_{Qscmax}$	57	57	57	mA	5.25	
SUPPLY DATA							
Supply current (total)	I_P typ.	16	16	16	mA	5.0	
	<	40	40	40	mA	5.0	
DYNAMIC DATA							
Signal requirements							
Pulse duration (T input)	t_{TH} >	–	20	–	ns	5.0	
Pulse duration (S input)	t_{SL} >	–	25	–	ns	5.0	
Performance							
Rise propagation delay time (S→Q)	t_{pdr} typ.	–	16	–	ns	5.0	N = 10; C_L = 15 pF
	t_{pdr} <	–	25	–	ns	5.0	
Fall propagation delay time (S→Q)	t_{pdf} typ.	–	25	–	ns	5.0	N = 10; C_L = 15 pF
	t_{pdf} <	–	40	–	ns	5.0	
Rise propagation delay time (T→Q)	t_{pdr} >	–	10	–	ns	5.0	
	t_{pdr} typ.	–	16	–	ns	5.0	N = 10; C_L = 15 pF
	t_{pdr} <	–	25	–	ns	5.0	
Fall propagation delay time (T→Q)	t_{pdf} >	–	10	–	ns	5.0	
	t_{pdf} typ.	–	25	–	ns	5.0	N = 10; C_L = 15 pF
	t_{pdf} <	–	40	–	ns	5.0	
Maximum operating frequency	f >	–	15	–	MHz	5.0	N = 10; C_L = 15 pF
	f typ.	–	20	–	MHz		

CHARACTERISTICS (continued)

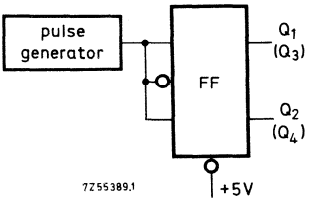
DYNAMIC DATA

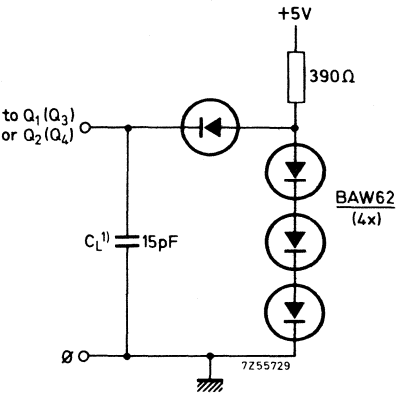
T, J and K INPUTS





Waveforms illustrating in- and output pulses



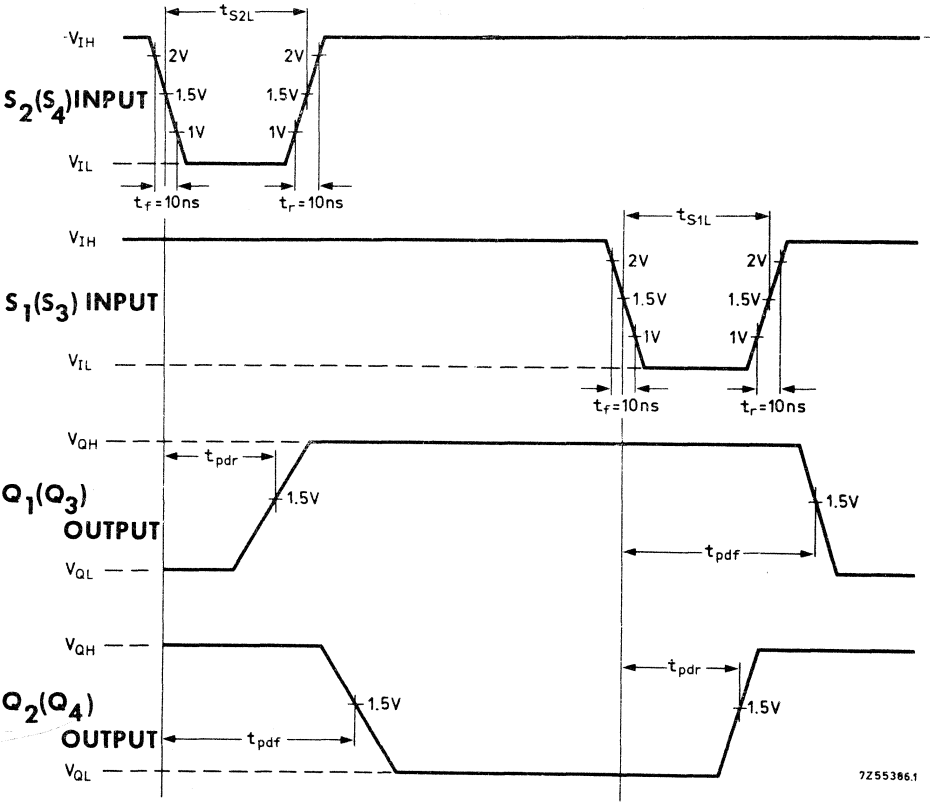


[1]) Including probe and jig capacitance

Equivalent load for N = 10

CHARACTERISTICS (continued)

DYNAMIC DATA

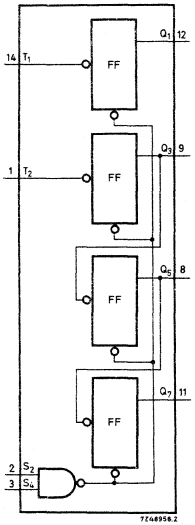


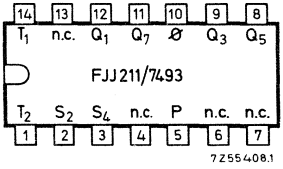
Waveforms illustrating switching times

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE ASYNCHRONOUS 4-BIT BINARY COUNTER

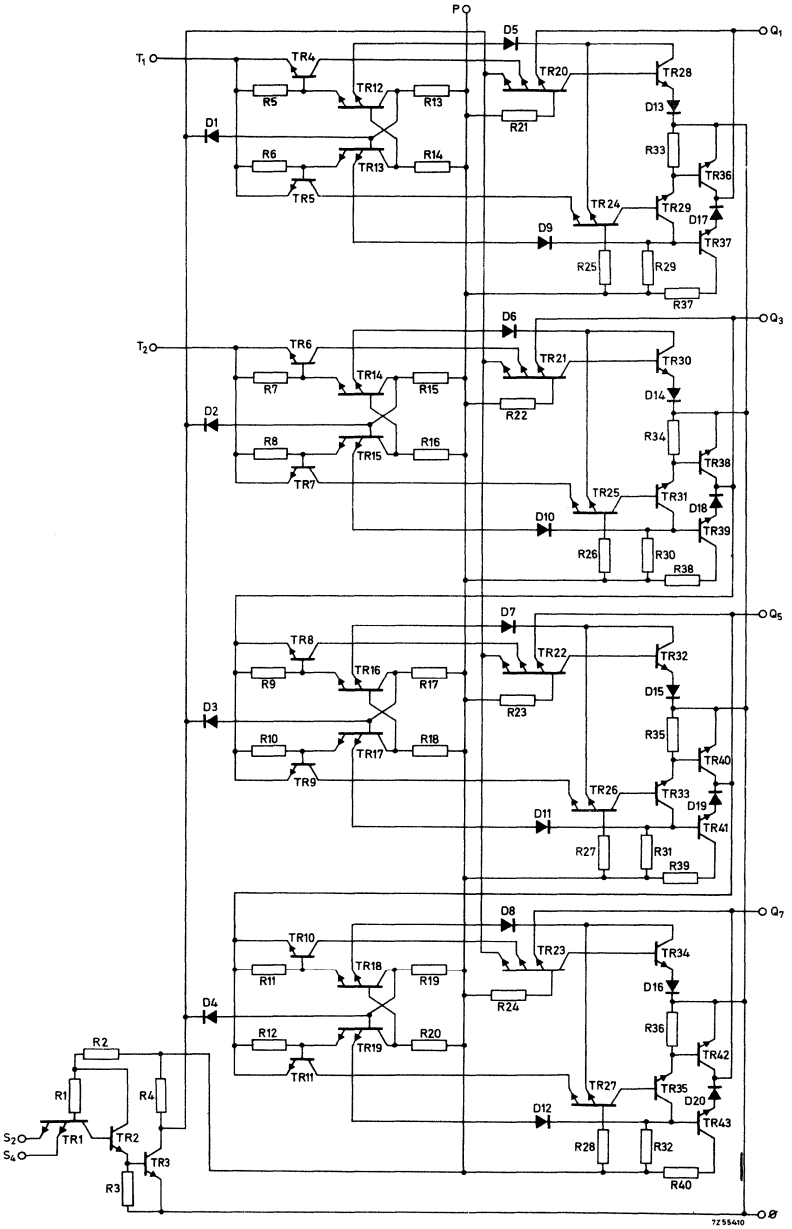




QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Maximum operating frequency	f	≥ 10	MHz
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 128	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



The FJJ211/7493 is a high-speed asynchronous 4-bit binary counter with four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-eight counter. By using an external connection a count of sixteen can be obtained. A gated line, direct reset inhibits the count and simultaneously all flip-flop outputs return to the LOW state.

For use as a 4-bit ripple-through counter, externally connect Q_1 to T_2; apply the count pulses to T_1. As shown by the function table below, the outputs at Q_1, Q_3, Q_5 and Q_7 represent division by 2, 4, 8 and 16 respectively.

For use as 3-bit ripple-through counter, apply the count pulses to T_2.

Simultaneous divisions by 2, 4 and 8 are available at the outputs Q_3, Q_5 and Q_7. The first flip-flop (T_1 and Q_1) can be used independently if the reset function (S_2 and S_4) coincides with reset of the 3-bit ripple-through counter.

FUNCTION TABLES

count	outputs			
	Q_1	Q_3	Q_5	Q_7
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Notes:
1. Q_1 connected to T_2
2. To reset all outputs in the LOW state, S_2 and S_4 inputs must be HIGH.
3. Either S_2 or S_4 (or both) must be LOW to count.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_T;V_S	max.	5.5	V [1]
Peak negative input voltage (T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}		−55 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

1) In addtion the input voltage between any two T inputs or between any two S inputs: max. 5.5 V.
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source-resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

		T_{amb} (°C)			Conditions and References	
		0	25	70	V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW						
S_2; S_4; T_1	V_{S2Lmax}, V_{S4Lmax}, V_{T1Lmax}	0.8	0.8	0.8 V	4.75	
T_2	V_{T2Lmax}	0.6	0.6	0.6 V	4.75	
Input threshold HIGH						
S_2; S_4; T_1	V_{S2Hmin}, V_{S4Hmin}, V_{T1Hmin}	2.0	2.0	2.0 V	4.75	
T_2	V_{T2Hmin}	2.2	2.2	2.2 V	4.75	
Output LOW						
Q_1; Q_3; Q_5; Q_7	V_{Q1Lmax}, V_{Q3Lmax}, V_{Q5Lmax}, V_{Q7Lmax}	0.4	0.4	0.4 V	4.75	Q_1 connected to T_2; $I_Q = I_{QLmax}$
Output HIGH						
Q_1; Q_3; Q_5; Q_7	V_{Q1Hmin}, V_{Q3Hmin}, V_{Q5Hmin}, V_{Q7Hmin}	2.4	2.4	2.4 V	4.75	Q_1 connected to T_2; $I_Q = -I_{QHmax}$
Currents						
Input LOW: S_2, S_4	$-I_{S2Lmax}$, $-I_{S4Lmax}$	1.6	1.6	1.6mA	5.25	$V_S = V_{QLmax}$
T_1	$-I_{T1Lmax}$	3.2	3.2	3.2 mA	5.25	$V_T = V_{QLmax}$
T_2	$-I_{T2Lmax}$					
Input HIGH: S_2, S_4	I_{S2Hmax}, I_{S4Hmax}	40	40	40 μA	5.25	$V_S = V_{QHmin}$
T_1	I_{T1Hmax}	80	80	80 μA	5.25	$V_T = V_{QHmin}$
T_2	I_{T2Hmax}	160	160	160 μA	5.25	$V_T = V_{QHmin}$
Output LOW						
Q_1; Q_3; Q_5; Q_7	I_{Q1Lmax}, I_{Q3Lmax}, I_{Q5Lmax}, I_{Q7Lmax}	16	16	16 mA	4.75	

CHARACTERISTICS (continued)

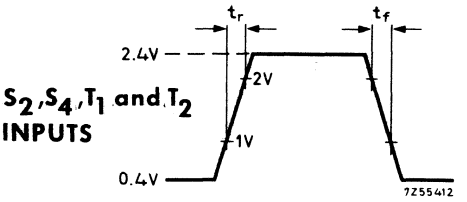
		T_{amb} (°C)			Conditions and References	
		0	25	70	V_P (V)	
STATIC DATA (continued)						
Output HIGH						
Q_1; Q_3; Q_5; Q_7	$-I_{Q1H}$ max $-I_{Q3H}$ max $-I_{Q5H}$ max $-I_{Q7H}$ max	400	400	400 µA	4.75	
Output short circuited						
Q_1; Q_3; Q_5; Q_7 (See note 2)	$-I_{Q1scmin}$ $-I_{Q3scmin}$ $-I_{Q5scmin}$ $-I_{Q7scmin}$	18	18	18 mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
	$-I_{Q1scmax}$ $-I_{Q3scmax}$ $-I_{Q5scmax}$ $-I_{Q7scmax}$	57	57	57 mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
SUPPLY DATA						
Supply current	I_P typ.	-	32	- mA	5	All inputs and outputs open
DYNAMIC DATA						
Rise propagation	t_{pdr} typ.	-	75	- ns	5	$C_L = 15$ pF; $R_L = 390\,\Omega$
delay time (note 1)	t_{pdr} <	-	135	- ns	5	$C_L = 15$ pF; $R_L = 390\,\Omega$
Fall propagation	t_{pdf} typ.	-	75	- ns	5	
delay time (note 1)	t_{pdf} <	-	135	- ns	5	
Rise time	t_r <	-	10	- ns	5	f = 1 MHz;
Fall time	t_f <	-	10	- ns	5	duty cycle: 0.5
Trigger time HIGH	t_{T1H}; t_{T2H} <	-	50	- ns	5	
Trigger time LOW	t_{T1L}; t_{T2L} <	-	50	- ns	5	
Width of pulse S_2 and S_4, LOW	t_{S2L}; t_{S4L} <	-	50	- ns	5	

Note 1:
All four outputs loaded. Output Q_1 connected to input T_2.

Note 2:
Not more than one output should be short circuited at a time.

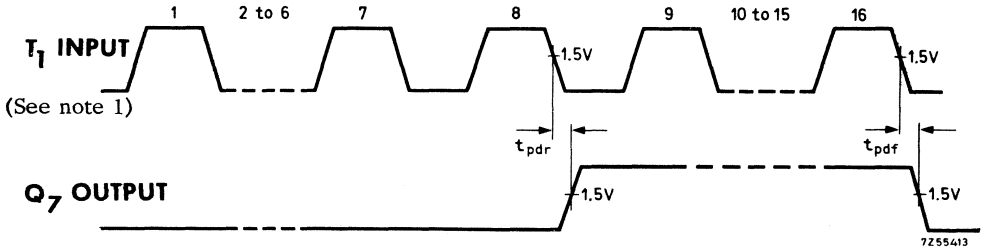
CHARACTERISTICS (continued)

DYNAMIC DATA



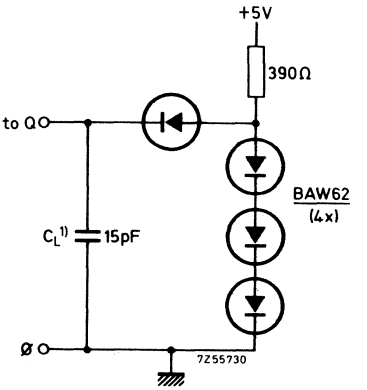
Pulse generator:

$t_r < 10$ ns
$t_f < 10$ ns
f = 1 MHz
duty cycle $\delta = 0.5$



Waveforms inllustrating measurement of t_{pdr} and t_{pdf}

Note 1:
T_1 input (Q_1 output connected to T_2 input)



To outputs Q_3, Q_5 and Q_7 the same loading circuit.

[1]) Including probe and jig capacitance.

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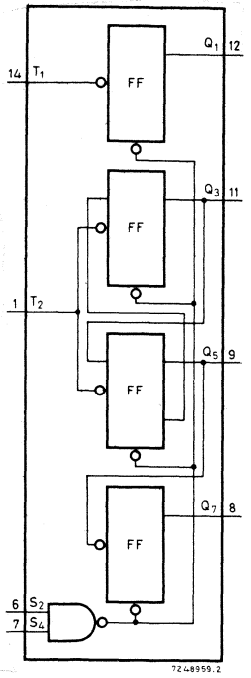
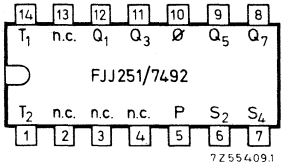


SINGLE ASYNCHRONOUS 4-BIT BINARY COUNTER

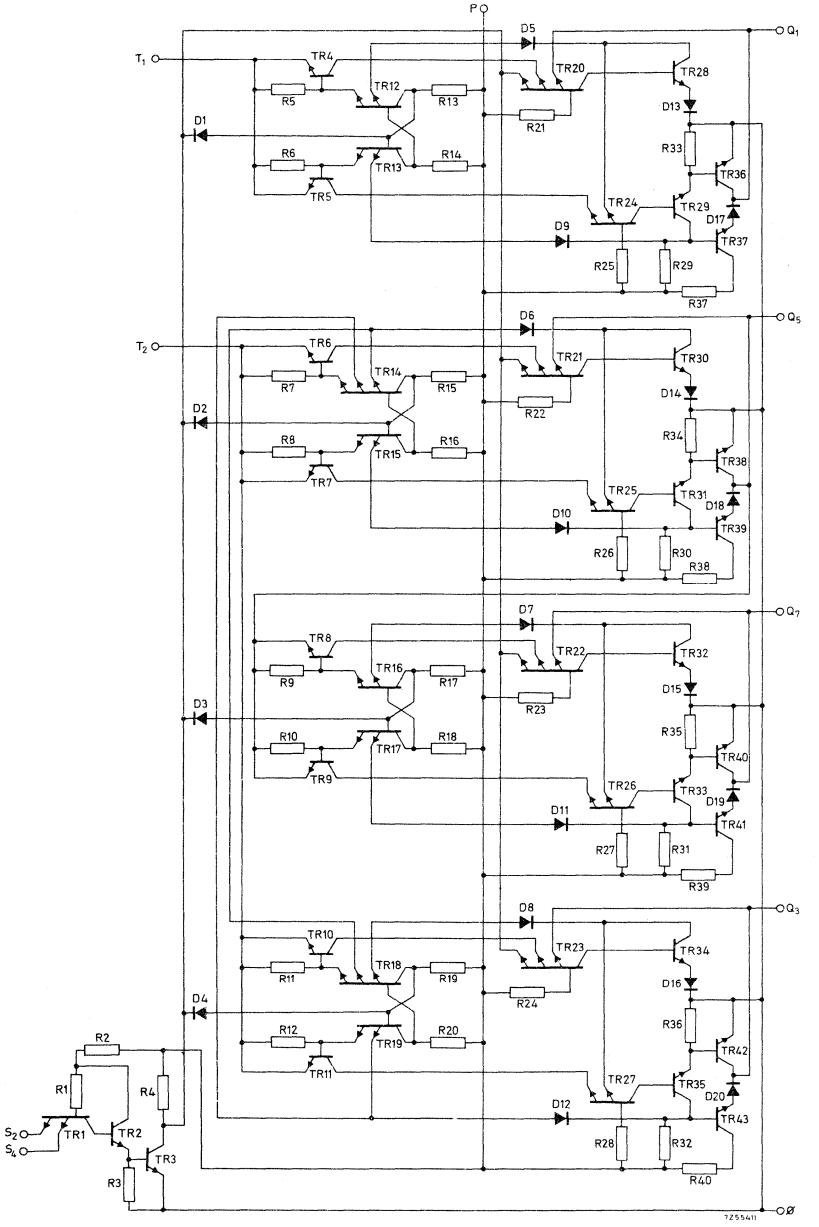


PACKAGE OUTLINE:

14 lead plastic dual in-line (type A)
(See General Section)

QUICK REFERENCE DATA			
Supply voltage	V_P	$5.0 \pm 5\%$	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Maximum operating frequency	f	$\geq$ 10	MHz
Available d.c. fan-out (full temperature range)	N_a	$\geq$ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 155	mW

CIRCUIT DIAGRAM



The FJJ251/7492 is a high-speed asynchronous 4-bit binary counter with four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-six counter. By using an external connection a count of twelve can be obtained. A gated line, direct reset inhibits the count and simultaneously all flip-flop outputs return to the LOW state.

For use as a divide-by-twelve counter, externally connect Q_1 to T_2; apply the count pulses to T_1.

Simultaneous divisions by 2, 6 and 12 are available at the outputs Q_1, Q_5 and Q_7 as shown in the function table below. For use as a divide-by-six counter, apply the count pulses to T_2.

Simultaneous divisions by 3 and 6 are available at the outputs Q_5 and Q_7.

The first flip-flop (T_1 and Q_1) can be used independently if the reset function coincides with reset of the divide-by-six counter.

FUNCTION TABLE

count	outputs			
	Q_1	Q_3	Q_5	Q_7
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Notes:

1. Q_1 connected to T_2
2. To reset all outputs in the LOW state, S_2 and S_4 inputs must be HIGH.
3. Either S_2 or S_4 (or both) must be LOW to count.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_T; V_S	max.	5.5	V [1]
Peak negative input voltage (T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition the input voltage between any two T inputs or between any two S inputs: max. 5.5 V.

[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\Omega$.

CHARACTERISTICS

		T_{amb} (°C) 0	25	75	Conditions and References V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW						
S_2; S_4; T_1	V_{S2Lmax}, V_{S4Lmax}, V_{T1Lmax}	0.8	0.8	0.8 V	4.75	
T_2	V_{T2Lmax}	0.6	0.6	0.6 V	4.75	
Input threshold HIGH						
S_2; S_4; T_1	V_{S2Hmin}, V_{S4Hmin}, V_{T1Hmin}	2.0	2.0	2.0 V	4.75	
T_2	V_{T2Hmin}	2.2	2.2	2.2 V	4.75	
Output LOW						
Q_1; Q_3; Q_5; Q_7	V_{Q1Lmax}, V_{Q3Lmax}, V_{Q5Lmax}, V_{Q7Lmax}	0.4	0.4	0.4 V	4.75	Q_1 connected to T_2 $I_Q = I_{QLmax}$
Output HIGH						
Q_1; Q_3; Q_5; Q_7	V_{Q1Hmin}, V_{Q3Hmin}, V_{Q5Hmin}, V_{Q7Hmin}	2.4	2.4	2.4 V	4.75	Q_1 connected to T_2 $I_Q = -I_{QHmax}$
Currents						
Input LOW: S_2, S_4	$-I_{S2Lmax}$, $-I_{S4Lmax}$	1.6	1.6	1.6 mA	5.25	$V_S = V_{QLmax}$
T_1	$-I_{T1Lmax}$	3.2	3.2	3.2 mA	5.25	$V_T = V_{QLmax}$
T_2	$-I_{T2Lmax}$	6.4	6.4	6.4 mA	5.25	$V_T = V_{QLmax}$
Input HIGH: S_2, S_4	I_{S2Hmax}, I_{S4Hmax}	40	40	40 µA	5.25	$V_S = V_{QHmin}$
T_1	I_{T1Hmax}	80	80	80 µA	5.25	$V_T = V_{QHmin}$
T_2	I_{T2Hmax}	160	160	160 µA	5.25	$V_T = V_{QHmin}$
Output LOW						
Q_1; Q_3; Q_5; Q_7	I_{Q1Lmax}, I_{Q3Lmax}, I_{Q5Lmax}, I_{Q7Lmax}	16	16	16 mA	4.75	

CHARACTERISTICS (continued)

		T_{amb} (°C) 0	25	75		V_P (V)	Conditions and References
STATIC DATA (continued)							
Output HIGH							
Q_1; Q_3; Q_5; Q_7	$-I_{Q1Hmax}$ ⎫ $-I_{Q3Hmax}$ ⎪ $-I_{Q5Hmax}$ ⎪ $-I_{Q7Hmax}$ ⎭	400	400	400	mA	4.75	
Output short circuited							
Q_1; Q_3; Q_5; Q_7 (see note 2)	$-I_{Q1scmin}$ ⎫ $-I_{Q3scmin}$ ⎪ $-I_{Q5scmin}$ ⎪ $-I_{Q7scmin}$ ⎭	18	18	18	mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
	$-I_{Q1scmax}$ ⎫ $-I_{Q3scmax}$ ⎪ $-I_{Q5scmax}$ ⎪ $-I_{Q7scmax}$ ⎭	57	57	57	mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
SUPPLY DATA							
Supply current	I_P typ.	-	31	-	mA	5	All inputs and outputs open
	<	51	51	51	mA	5	
DYNAMIC DATA							
Rise propagation delay time (note 1)	t_{pdr} typ.	-	60	-	ns	5	$C_L = 15$ pF; $R_L = 390\ \Omega$
	t_{pdr} <	-	100	-	ns	5	
Fall propagation delay time (note 1)	t_{pdf} typ.	-	60	-	ns	5	
	t_{pdf} <	-	100	-	ns	5	
Rise time	t_r <	-	10	-	ns	5	f = 1 MHz; duty cycle: 0.5
Fall time	t_f <	-	10	-	ns	5	
Trigger time HIGH	t_{T1H}; t_{T2H} <	-	50	-	ns	5	
Trigger time LOW	t_{T1L}; t_{T2L} <	-	50	-	ns	5	
Width of pulse S_2 and S_4, LOW	t_{S2L}; t_{S4L} <	-	50	-	ns	5	

Note 1:

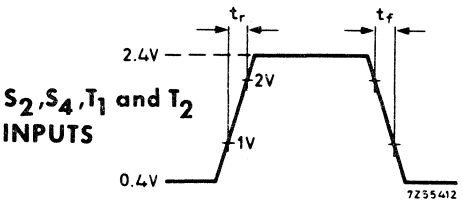
All four output loaded. Output Q_1 connected to input T_2.

Note 2:

Not more than one output should be short circuited at a time.

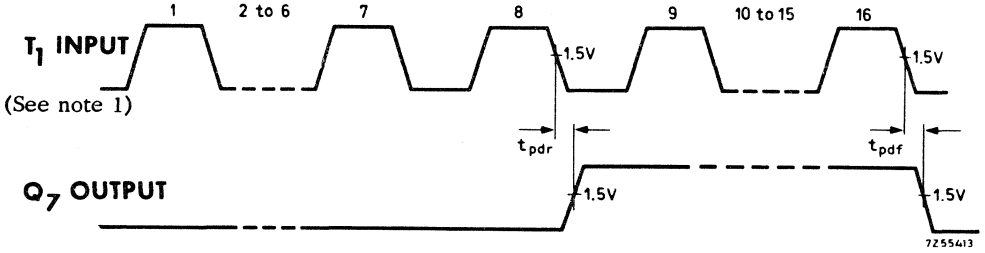
CHARACTERISTICS (continued)

DYNAMIC DATA



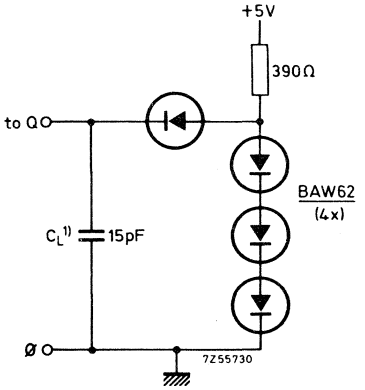
Pulse generator:

t_r < 10 ns
t_f < 10 ns
f = 1 MHz
duty cycle δ = 0.5



Waveforms inllustrating measurement of t_{pdr} and t_{pdf}

Note 1:
T_1 input (Q_1 output connected to T_2 input)



To outputs Q_3, Q_5 and Q_7 the same loading circuit.

[1]) Including probe and jig capacitance.

DUAL JK MASTER-SLAVE FLIP-FLOP

For data of this type please refer to FJJ121/7473

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

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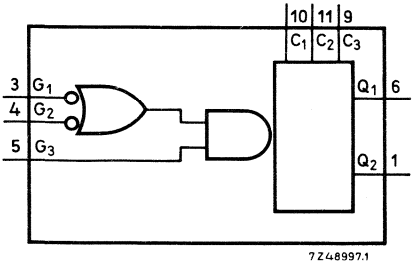
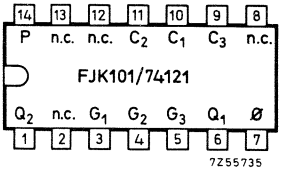
MONOSTABLE MULTIVIBRATOR





QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available fan-out (each output)	N_a	≥ 10	
Average power consumption (50% duty cycle)	P_{av}	typ. 90	mW

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

The FJK101/74121 monostable multivibrator features D.C. voltage level triggering which is not directly related to the input pulse transition time. The input gating allows the choice of triggering either on the positive or negative-going edge of the input pulse, as well as providing an inhibit facility. Both positive and negative output pulses are available with a full fan-out of 10 and TTL line driving capabilities.
G_1 and G_2 are negative-edge trigger inputs and will trigger the one-shot when either or both go LOW as long as G_3 is HIGH. G_3 is a positive-edge Schmitt-trigger input for slow edges or level detection, and will trigger the one-shot when G_3 goes HIGH as long as G_1 or G_2 are LOW.
Output pulse duration may be varied between 40 ns and 40 s and is determined by the value of external components used (see TIMING NOTES on page 6).

FUNCTION TABLE

inputs						outputs
t_n			t_{n+1}			
G_1	G_2	G_3	G_1	G_2	G_3	
H	H	L	H	H	H	inhibit
L	X	H	L	X	L	"
X	L	H	X	L	L	"
L	X	L	L	X	H	one-shot
X	L	L	X	L	H	"
H	H	H	X	L	H	"
H	H	H	L	X	H	"
X	L	L	X	H	L	inhibit
L	X	L	H	X	L	"
X	L	H	H	H	H	"
L	X	H	H	H	H	"
H	H	L	X	L	L	"
H	H	L	L	X	L	"

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial

t_n = time before input transition
t_{n+1} = time after input transition

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. input voltage	V_G	max.	5.5	V [1]
Negative transient input voltage	$-V_{GM}$	max.	2.0	V [2]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (negative-going)							
any input	V_{GLmin}	0.8	0.8	0.8	V	4.75	
G_1; G_2	V_{GLtyp}	–	1.4	–	V	5.0	
G_3	V_{GLtyp}	–	1.35	–	V	5.0	
Input threshold HIGH (positive-going)							
any input	V_{GHmax}	2.0	2.0	2.0	V	4.75	
G_1; G_2	V_{GHtyp}	–	1.4	–	V	5.0	
G_3	V_{GHtyp}	–	1.55	–	V	5.0	
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	I_Q = 16 mA
	V_{QLtyp}	–	0.22	–	V	5.0	
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	I_Q = −400 µA
	V_{QHtyp}	–	3.3	–	V	5.0	
Currents							
Input LOW							
G_1; G_2	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	V_I = 0.4 V
G_3	$-I_{GLmax}$	3.2	3.2	3.2	mA	5.25	
Input HIGH							
G_1; G_2	I_{GHmax}	40	40	40	µA	5.25	V_I = 2.4 V
G_3	I_{GHmax}	80	80	80	µA	5.25	
any input	I_{GHmax}	1	1	1	mA	5.25	V_I = 5.5 V
Output LOW	I_{QLmax}	16	16	16	mA		
Output short-circuit [1])	$-I_{Qsc\ min}$	18	18	18	mA	5.25	
	$-I_{Qsc\ max}$	55	55	55	mA	5.25	
SUPPLY DATA							
Supply current							
quiescent (unfired)	I_P typ.	13	13	13	mA	5.0	
	I_P <	25	25	25	mA	5.0	
fired	I_P typ.	13	23	13	mA	5.0	
	I_P <	40	40	40	mA	5.0	

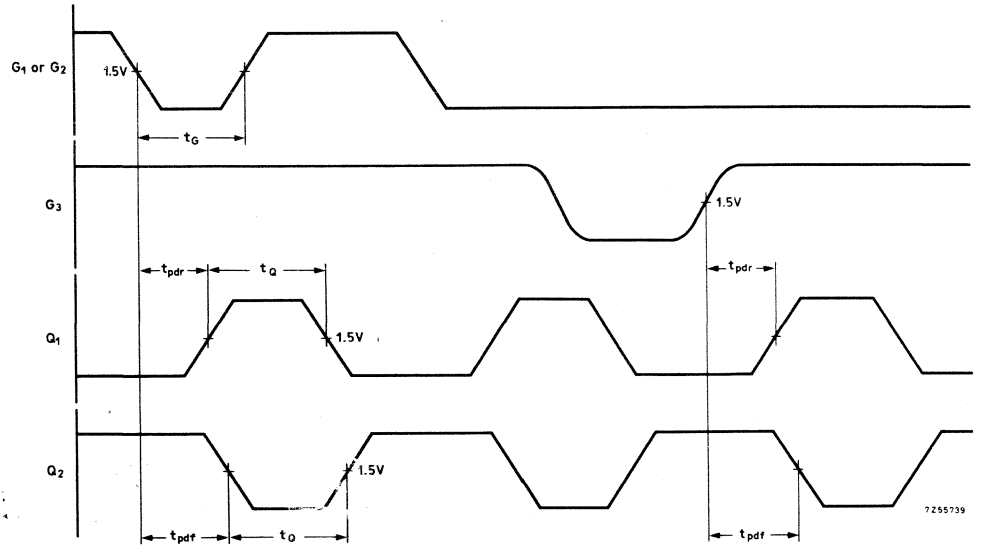
[1]) Only one input to be shorted at a time.

CHARACTERISTICS (continued)

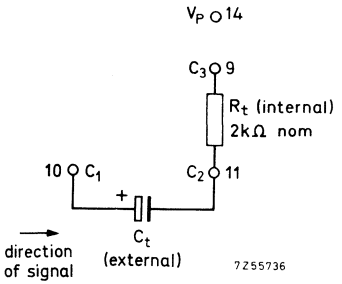
		T_{amb} (°C) 0	25	70		V_P (V)	Conditions and references $C_L = 15\,pF; N_a = 10$
DYNAMIC DATA							
Signal requirements							
Input pulse width	t_G >	–	50	–	ns		
Input pulse rise/fall time							
G_1; G_2	$\frac{dV_G}{dt}$ <	–	1	–	V/µs		
G_3	$\frac{dV_G}{dt}$ <	–	1	–	V/s		
Performance							
Rise propagation delay time							
$G_1, G_2 \longrightarrow Q_1$	t_{pdr} >	–	25	–	ns	5.0	C_t = 80 pF
	t_{pdr} typ.	–	45	–	ns	5.0	
	t_{pdr} <	–	70	–	ns	5.0	
$G_3 \longrightarrow Q_1$	t_{pdr} >	–	15	–	ns	5.0	
	t_{pdr} typ.	–	35	–	ns	5.0	
	t_{pdr} <	–	55	–	ns	5.0	
Fall propagation delay time							
$G_1, G_2 \longrightarrow Q_2$	t_{pdf} >	–	30	–	ns	5.0	
	t_{pdf} typ.	–	50	–	ns	5.0	
	t_{pdf} <	–	80	–	ns	5.0	
$G_3 \longrightarrow Q_2$	t_{pdf} >	–	20	–	ns	5.0	
	t_{pdf} typ.	–	40	–	ns	5.0	
	t_{pdf} <	–	65	–	ns	5.0	
Output pulse width:							
with internal timing resistance	t_Q >	–	70	–	ns	5.0	C_t = 80pF; R_t=open; pin C_3 connected to 5.0 V
	t_Q typ.	–	110	–	ns	5.0	
	t_Q <	–	150	–	ns	5.0	
with zero timing capacitance	t_Q >	–	20	–	ns	5.0	C_t = 0; R_t = open; pin C_3 connected to 5.0 V
	t_Q typ.	–	30	–	ns	5.0	
	t_Q <	–	50	–	ns	5.0	
with external timing resistance	t_Q >	–	600	–	ns	5.0	C_t = 100 pF; R_t = 10 KΩ; pin C_3 open
	t_Q typ.	–	700	–	ns	5.0	
	t_Q <	–	800	–	ns	5.0	
	t_Q >	–	6	–	ms	5.0	C_t = 1 µF; R_t = 10 KΩ; pin C_3 open
	t_Q typ.	–	7	–	ms	5.0	
	t_Q <	–	8	–	ms	5.0	

CHARACTERISTICS (continued)

DYNAMIC DATA

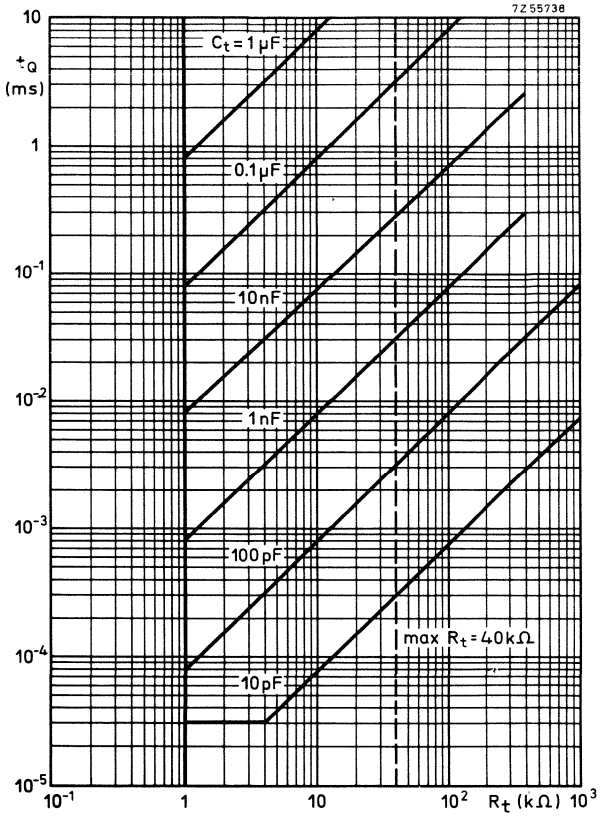


CHARACTERISTICS (continued)
TIMING NOTES



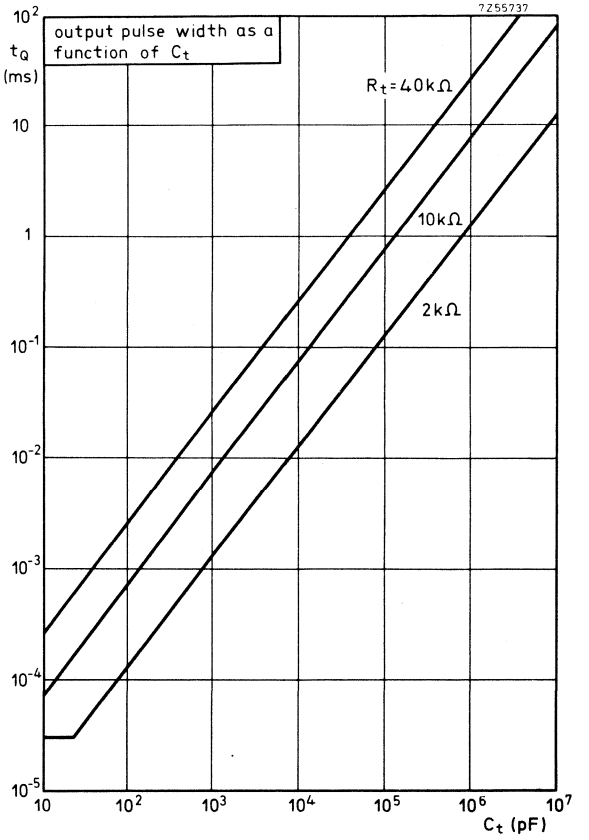
1. An external timing capacitor may be connected between C_1 (pin 10 - positive) and C_2 (pin 11 - negative). Without an external capacitor the output pulse width is typically 30 ns.
2. An internal timing resistor is incorporated between C_3 (pin 9) and C_2 (pin 11) and has a nominal value of 2 kΩ. It may be brought into the circuit by connecting C_3 to V_P (pin 14).
3. For variable pulse widths an external variable resistor should be connected between C_3 and V_P; no external limiting is then required.
4. For accurate repeatable pulse widths connect an external resistor between point C_2 and V_P, leaving point C_3 open.
5. Jitter-free operation is maintained over the full temperature and supply voltage range for timing capacitances from 10 pF to 10 µF and timing resistances from 2 kΩ to 40 kΩ.
   Within these limits the output pulse width follows the relationship $t_Q = C_t.R_t \ell nZ$.
6. A duty cycle of up to 67 % is achieved by using only the internal timing resistance. Duty cycles as high as 90 % are obtained by using R_t = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

CHARACTERISTICS (continued)



output pulse width as a function of R_t

CHARACTERISTICS (continued)



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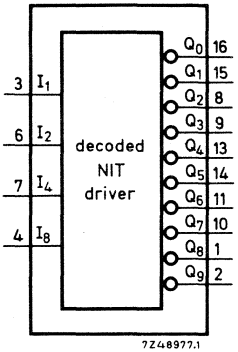
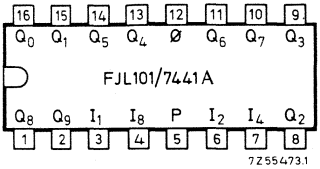
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE DECODER N.I.T. DRIVER [1])





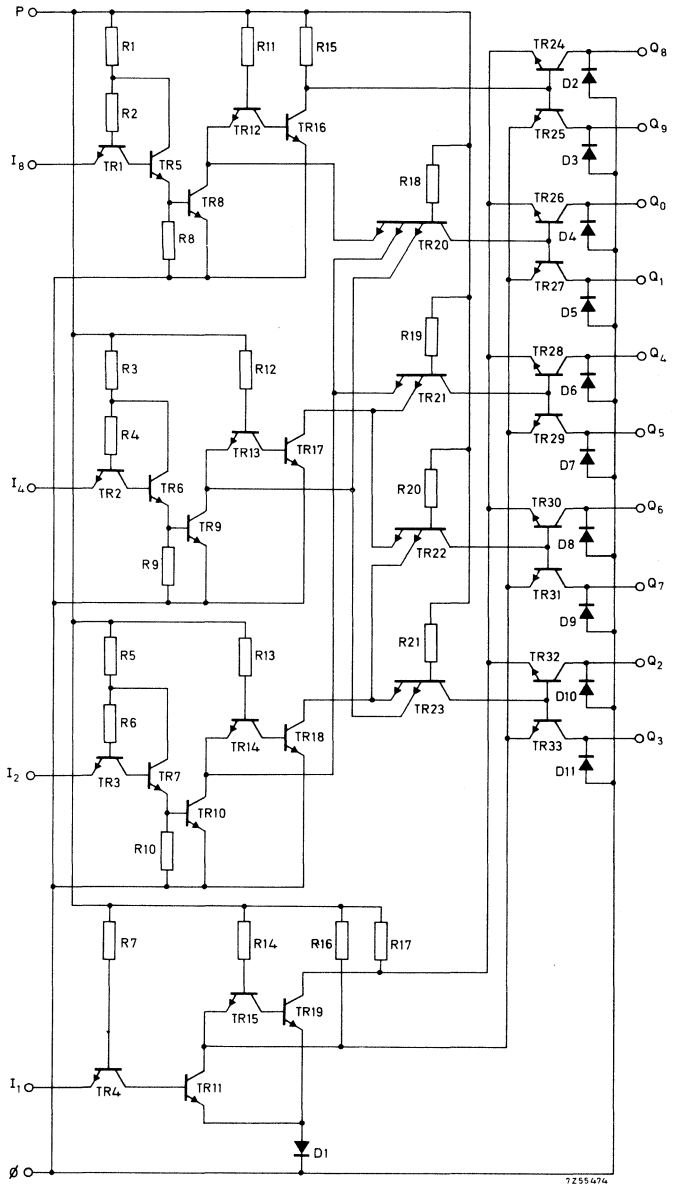
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Supply current	Ip	typ. 19	mA
Drive lines		10	
Output voltage at any output	V_Q	> 55	V

The FJL101/7441A is a BCD (1-2-4-8 code) to decimal decoder incorporating high voltage output transistors for driving numerical indication tubes. It contains a decoding array followed by ten output driver stages which can be used for parallel or serial drive. For parallel drive no external clamping diodes are needed. For serial drive the cathode voltages must be clamped to prevent excessive dissipation that may be caused by the leakage currents of non-ignited cathodes are cut-off.

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) (See General Section)

1) N.I.T.; Numerical Indicator Tube.

CIRCUIT DIAGRAM



FUNCTION TABLE

inputs				output
I_1	I_2	I_4	I_8	ON-state *)
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9

*) All other outputs are off.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_I	max.	5.5	V
Current into any output (OFF state)	I_Q	max.	0.5	mA
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

CHARACTERISTICS

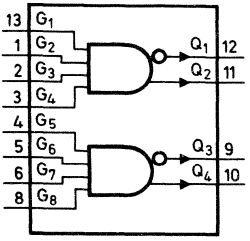
		T_{amb} (°C) 0	25	70	Conditions and References V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW [1])	V_{ILmax}	0.8	0.8	0.8 V	4.75	
Input threshold HIGH [1])	V_{IHmin}	2.0	2.0	2.0 V	4.75	
Output LOW (ON-state) [1])	V_{QLmax}	2.5	2.5	2.5 V	4.75	I_{QL} = 7 mA; V_{IL} = 0.8 V; V_{IH} = 2.0 V
Currents						
Input LOW I_1	$-I_{I1Lmax}$	3.2	3.2	3.2 mA	5.25	V_{IL} = 0.4 V
I_2, I_4, I_8	$-I_{I2Lmax}$, $-I_{I4Lmax}$, $-I_{I8Lmax}$	1.6	1.6	1.6 mA	5.25	V_{IL} = 0.4 V
Input HIGH I_1	I_{I1Hmax}	80	80	80 µA	5.25	V_{IH} = 2.4 V
	I_{I1Hmax}	1	1	1 mA	5.25	V_{IH} = 5.5 V
I_2, I_4, I_8	I_{I2Hmax}, I_{I4Hmax}, I_{I8Hmax}	40	40	40 µA	5.25	V_{IH} = 2.4 V
I_2, I_4, I_8	I_{I2Hmax}, I_{I4Hmax}, I_{I8Hmax}	1	1	1 mA	5.25	V_{IH} = 5.5 V
Output leakage current HIGH (OFF-state) [1])	$-I_{QHmax}$	200	200	200 µA	5.25	V_Q = 55 V, V_{IL} = V_{ILmax}; V_{IH} = V_{IHmax}
SUPPLY DATA						
Supply current	I_P typ.	-	22	- mA	5.0	All inputs and outputs open

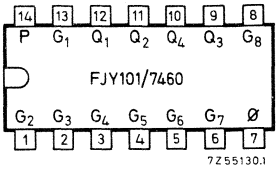
[1]) See function table on page 3, V_{IL} and V_{IH} to be maintained as in function table.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL 4-INPUT AND-OR-NOT EXPANDER





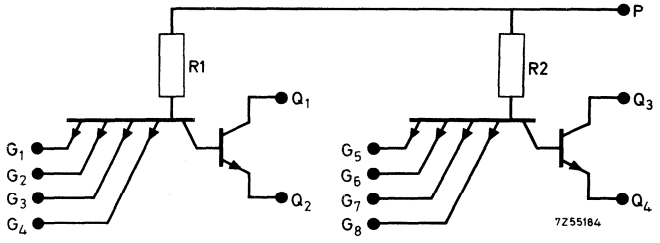
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Average propagation delay time when used with FJH151 or FJH171 N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ. 15	ns
D.C. noise margin [1]) (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption; (each expander) T_{amb} = 25 °C	P_{av}	typ. 4.0	mW

The FJY101/7460 is a dual 4-input AND-OR-NOT expander for use with the FJH151/7450 and FJH171/7453. Up to 4 expanders may be connected to the expandable gates of FJH151/7450 and FJH171/7453.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

[1]) When used with FJH151/7450 or FJH171/7453 as applicable.

CIRCUIT DIAGRAM



RATINGS Limiting values in accrodance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0 V
Input voltage	V_G	max.	5.5 V[1])
Peak negative G input voltage	$-V_{GM}$	max.	2 V[2])
Storage temperature	T_{stg}	−55 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

[1]) In addition the voltage between any two inputs: max. 5.5 V.
[2]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS [1])

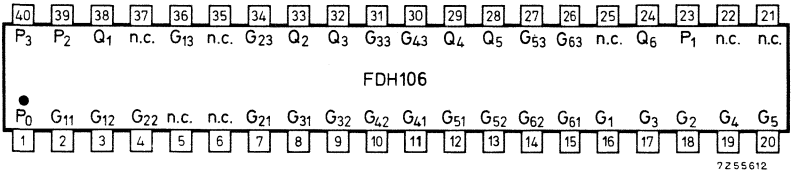
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	V_G = 0.40 V
Input HIGH	I_{GHmax}	40	40	40	μA	5.25	V_G = 2.4 V
SUPPLY DATA							
Supply current							
Input LOW	I_{PL} typ.	2.0	2.0	2.0	mA	5.0	V_G = 0
	I_{PL} <	4.0	4.0	4.0	mA	5.0	
Input HIGH	I_{PH} typ.	1.2	1.2	1.2	mA	5.0	V_G = 5.0 V
	I_{PH} <	2.5	2.5	2.5	mA	5.0	
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ.	–	15	–	ns	5.0	C_L = 15 pF, N = 10
	<	–	30	–	ns		
Fall propagation delay time	t_{pdf} typ.	–	10	–	ns	5.0	
	<	–	20	–	ns		

[1]) When used in conjunction with the FJH151/7450

MOS FD family

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

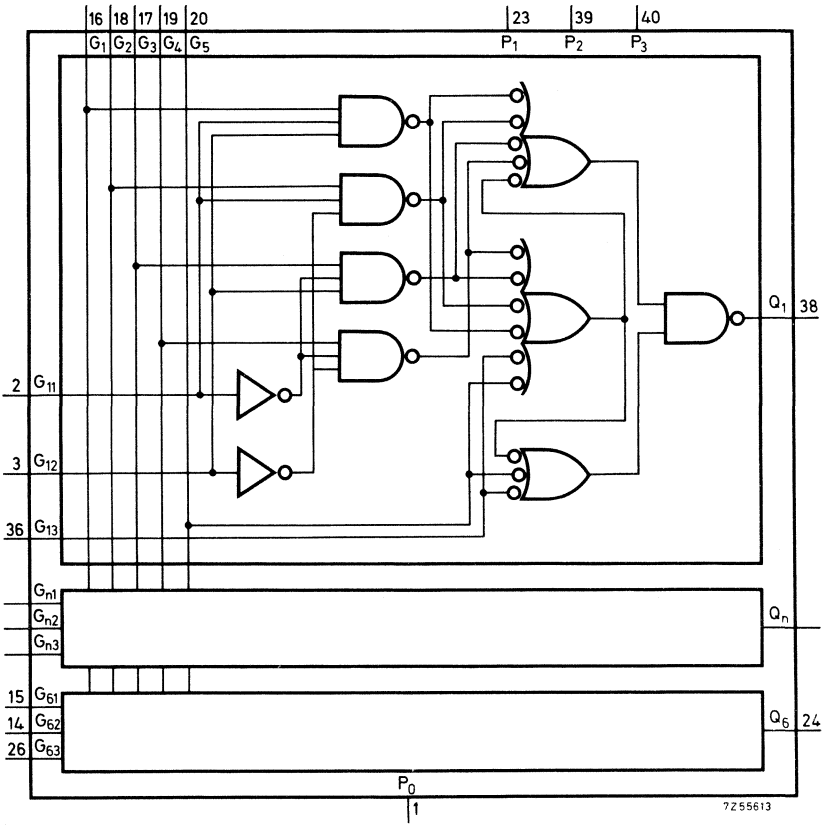
ARITHMETIC/LOGIC ARRAY



P_0 and metal lid on top of the package are connected

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay				
C_L = 50 pF	t_{pd}	typ.	250	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Average power consumption per function				
at 1 MHz switching rate	P_{av}	typ.	35	mW

PACKAGE OUTLINE: 40 lead ceramic dual in-line (See General Section)


16
18
17
19
20
23
39
40
G1
G2
G3
G4
G5
P1
P2
P3
Q1
38
2
G11
3
G12
36
G13
Gn1
Gn2
Gn3
Qn
15
G61
14
G62
26
G63
Q6
24
P0
1
7Z55613

GENERAL DESCRIPTION

The FDH106 consists of six, identical, 3-input gate networks. Five coded control lines determine the function of the six gate networks. Each network may function as a full adder/subtractor, or, if used as a 2-input gate, it can provide all logic functions of 2 variables.
Thus one of 32 different functions can be selected by the control lines; the selected function is available six times.
The output voltage swing is determined by the output buffer supply voltage. All inputs are protected against over-voltage caused by static charges.
Inputs G_1 to G_5 have pull-down resistors connected to P_3, so that they assume the LOW state when left floating.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_3	$-I_{P3}$	max.	40	mA
Output current per output	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	°C/W

FUNCTION TABLE

G_5 G_4 G_3 G_2 G_1	logic equation (positive logic)	logic function	
		positive logic	negative logic
L L L L L	Q_n = HIGH	–	–
L L L L H	$Q_n = \overline{G_{n1}} + \overline{G_{n2}}$	NAND	NOR
L L L H L	$Q_n = \overline{G_{n1}} + G_{n2}$	–	–
L L L H H	$Q_n = \overline{G_{n1}}$	Complement G_{n1}	Complement G_{n1}
L L H L L	$Q_n = G_{n1} + G_{n2}$	OR	AND
L L H L H	$Q_n = \overline{G_{n1}} \cdot G_{n2} + G_{n1} \cdot \overline{G_{n2}}$	exclusive-OR	comparator
L L H H L	$Q_n = G_{n2}$	transfer G_{n2}	transfer G_{n2}
L L H H H	$Q_n = \overline{G_{n1}} \cdot G_{n2}$	–	–
L H L L L	$Q_n = G_{n1} + \overline{G_{n2}}$	–	–
L H L L H	$Q_n = \overline{G_{n2}}$	Complement G_{n2}	Complement G_{n2}
L H L H L	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}} + G_{n1} \cdot G_{n2}$	comparator	exclusive-OR
L H L H H	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}}$	NOR	NAND
L H H L L	$Q_n = G_{n1}$	transfer G_{n1}	transfer G_{n1}
L H H L H	$Q_n = G_{n1} \cdot \overline{G_{n2}}$	–	–
L H H H L	$Q_n = G_{n1} \cdot G_{n2}$	AND	OR
L H H H H	Q_n = LOW	–	–

FUNCTION TABLE (continued)

G_5	G_4	G_3	G_2	G_1	logic equation (positive logic)	logic function: positive logic	logic function: negative logic
H	L	L	L	L	$Q_n = \overline{G_{n3}}$	Complement G_{n3}	Complement G_{n3}
H	L	L	L	H	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n3}} + \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$	–	–
H	L	L	H	L	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n3}} + G_{n2} \cdot \overline{G_{n3}} + G_{n1} \cdot \overline{G_{n2}} \cdot G_{n3}$	–	–
H	L	L	H	H	$Q_n = G_{n1} \cdot G_{n3} + \overline{G_{n1}} \cdot \overline{G_{n3}}$	comparator	exclusive-OR
H	L	H	L	L	$Q_n = G_{n1} \cdot \overline{G_{n3}} + G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot G_{n3}$	–	–
H	L	H	L	H	$Q_n = G_{n1} \cdot G_{n2} \cdot G_{n3} + G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + + \overline{G_{n1}} \cdot G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot G_{n3}$	add	add
H	L	H	H	L	$Q_n = G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n2}} \cdot G_{n3}$	exclusive-OR	comparator
H	L	H	H	H	$Q_n = G_{n1} \cdot G_{n3} + \overline{G_{n2}} \cdot G_{n3} + \overline{G_{n1}} \cdot G_{n2} \cdot \overline{G_{n3}}$	–	–
H	H	L	L	L	$Q_n = G_{n1} \cdot \overline{G_{n3}} + \overline{G_{n2}} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot G_{n2} \cdot G_{n3}$	–	–
H	H	L	L	H	$Q_n = G_{n2} \cdot G_{n3} + \overline{G_{n2}} \cdot \overline{G_{n3}}$	comparator	exclusive-OR
H	H	L	H	L	$Q_n = G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}} + G_{n1} \cdot \overline{G_{n2}} \cdot G_{n3} + + \overline{G_{n1}} \cdot G_{n2} \cdot G_{n3} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}}$	subtract	subtract
H	H	L	H	H	$Q_n = G_{n1} \cdot G_{n3} + G_{n2} \cdot G_{n3} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}}$	–	–
H	H	H	L	L	$Q_n = G_{n1} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot G_{n3}$	exclusive-OR	comparator
H	H	H	L	H	$Q_n = \overline{G_{n1}} \cdot G_{n3} + G_{n2} \cdot G_{n3} + G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}}$	–	–
H	H	H	H	L	$Q_n = \overline{G_{n1}} \cdot G_{n3} + \overline{G_{n2}} \cdot G_{n3} + G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}}$	–	–
H	H	H	H	H	$Q_n = G_{n3}$	transfer G_{n3}	transfer G_{n3}

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; $V_{P2} = V_{P3}$ = −12 to −14 V (see note 1); T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1]	max.	conditions and references
Input logic levels					
HIGH	V_{GH}	−2	0	+0.3 V	
LOW	V_{GL}	−28	–	−9 V	
Output levels					
HIGH	V_{QH}	−1.0	–	0 V	
LOW	V_{QL}	−14	–	−10 V	
Input capacitance					
G_1;G_2;G_3;G_4;G_5	C_{G1} to C_{G5}	–	5.5	7 pF	bias: V_G=0V; f=1MHz
all other inputs	C_{G11} to C_{G63}	–	3.5	5 pF	bias: V_G=0V; f=1MHz
Input leakage current	$-I_{GL}$	–	–	1 µA	V_G=−15V; T_{amb}=25°C; all other terminals at V_{P0}
Output resistance					
HIGH	R_{QH}	–	1.0	– kΩ	V_Q = −1 V
LOW	R_{QL}	–	2.0	– kΩ	V_Q = −10 V
Supply current (see note 2)	$-I_{P1}$	–	4.6	7.0 mA	f=1MHz; T_{amb}=25°C
	$-I_{P2}$	–	2.0	2.5 mA	
	$-I_{P3}$	–	4.2	6.0 mA	
Output transition times:					
fall time	t_{THL}	–	150	– ns	
rise time	t_{TLH}	–	150	– ns	
Delay times:					
fall time	t_{DHL}	–	250	400 ns	see note 3
rise time	t_{DLH}	–	250	400 ns	
Control input sink current	$-I_{G1}$ to $-I_{G5}$	–	32	– µA	bias: V_G = −2 V

Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

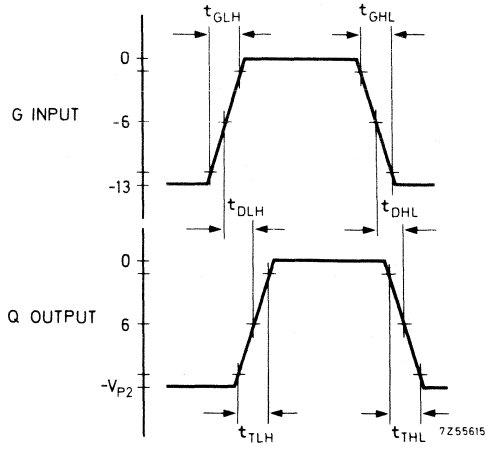
Note 2: Output buffer power supply current is almost entirely dependent on the external load.

Note 3: Delays are measured at −6 V levels of input and output signals.

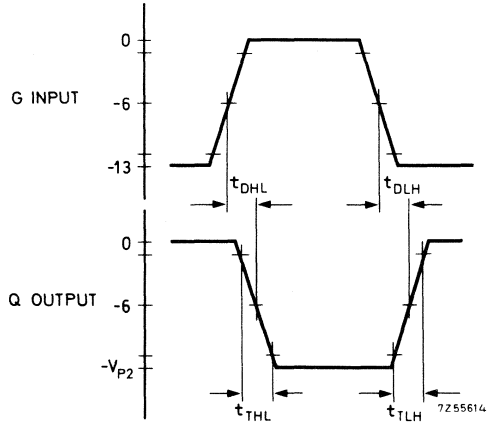
[1]) All typ. values under test conditions: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = V_{P3} = −12 to −14 V; t_{GLH} = t_{GHL} = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

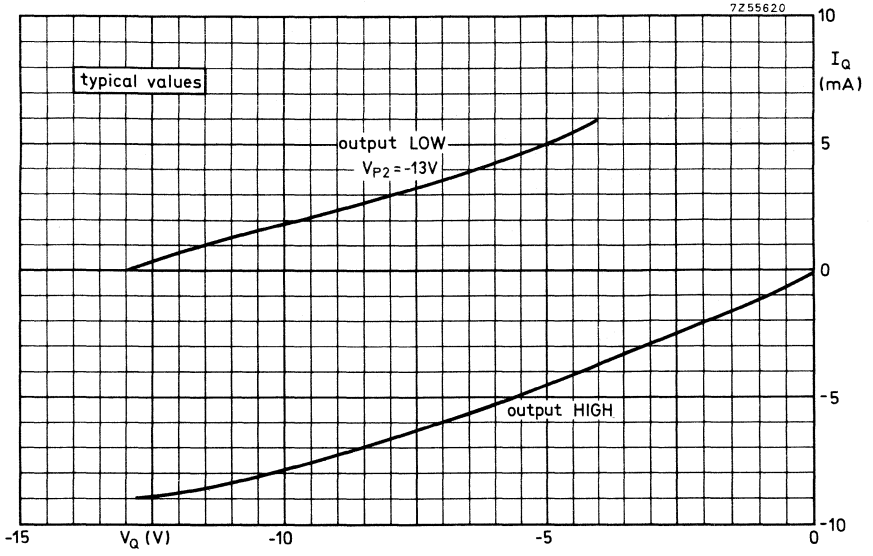
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

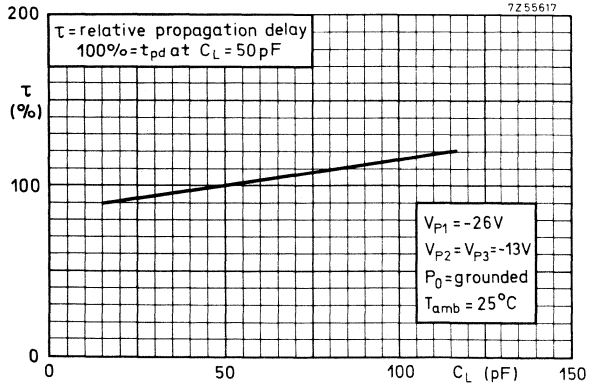
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH106 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

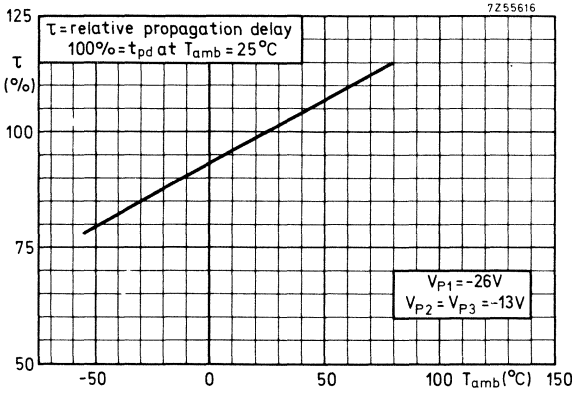


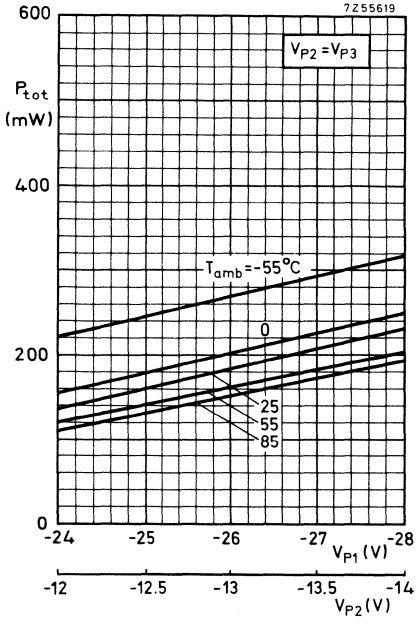
TYPICAL PERFORMANCE at load of C_L in parallel with 1 MΩ to P_0.



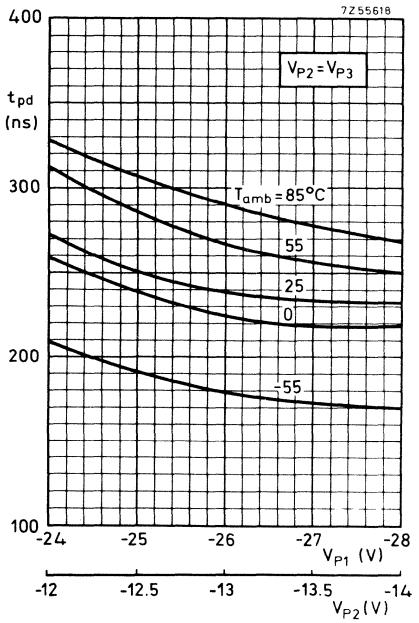
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





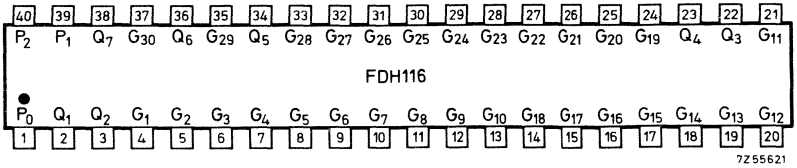
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

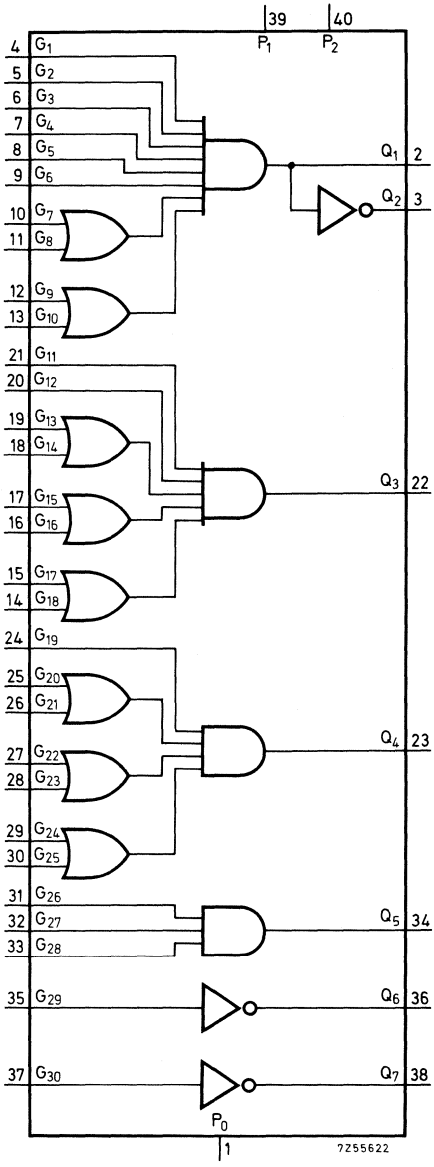
CONTROL LOGIC ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Power dissipation (f = 1 MHz)	P_{tot}	typ.	150	mW
Average propagation delay	t_{pd}	typ.	250	ns
D.C. noise margin	M_H; M_L	>	1.0	V

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)


39
40
P1
P2
4 G1
5 G2
6 G3
7 G4
8 G5
9 G6
10 G7
11 G8
12 G9
13 G10
21 G11
20 G12
19 G13
18 G14
17 G15
16 G16
15 G17
14 G18
24 G19
25 G20
26 G21
27 G22
28 G23
29 G24
30 G25
31 G26
32 G27
33 G28
35 G29
37 G30
Q1 2
Q2 3
Q3 22
Q4 23
Q5 34
Q6 36
Q7 38
P0
1
7Z55622

GENERAL DESCRIPTION

The FDH116 contains all the logic functions shown in the diagram and described in the logic function on page 4. It is intended to perform the control logic in all MOS digital systems. The output voltage swing is determined by the output buffer supply voltage. All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5 to −30		V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	°C/W

LOGIC FUNCTIONS

Positive logic

$$Q_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot (G_7 + G_8) \cdot (G_9 + G_{10})$$

$$Q_2 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot (G_7 + G_8) \cdot (G_9 + G_{10})}$$

$$Q_3 = G_{11} \cdot G_{12} \cdot (G_{13} + G_{14}) \cdot (G_{15} + G_{16}) \cdot (G_{17} + G_{18})$$

$$Q_4 = G_{19} \cdot (G_{20} + G_{21}) \cdot (G_{22} + G_{23}) \cdot (G_{24} + G_{25})$$

$$Q_5 = G_{26} \cdot G_{27} \cdot G_{28}$$

$$Q_6 = \overline{G_{29}}$$

$$Q_7 = \overline{G_{30}}$$

Negative logic

$$Q_1 = G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 \cdot G_8 + G_9 \cdot G_{10}$$

$$Q_2 = \overline{G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 \cdot G_8 + G_9 \cdot G_{10}}$$

$$Q_3 = G_{11} + G_{12} + (G_{13} \cdot G_{14}) + (G_{15} \cdot G_{16}) + (G_{17} \cdot G_{18})$$

$$Q_4 = G_{19} + (G_{20} \cdot G_{21}) + (G_{22} \cdot G_{23}) + (G_{24} \cdot G_{25})$$

$$Q_5 = G_{26} + G_{27} + G_{28}$$

$$Q_6 = \overline{G_{29}}$$

$$Q_7 = \overline{G_{30}}$$

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V (see note 1); T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

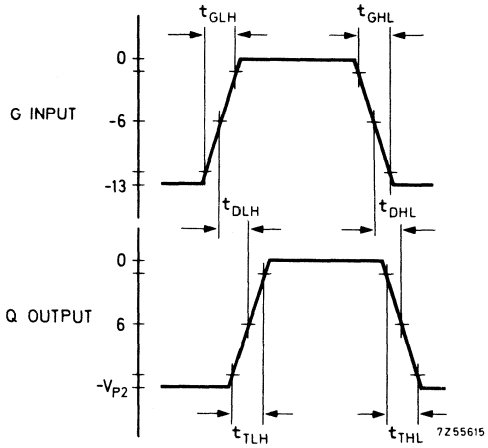
	Symbol	min.	typ. [1]	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	–	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance						
G_{29}; G_{30}	C_{G29}, C_{G30}	–	5	7	pF	bias: V_G = 0 V
all other inputs	C_{G1} to C_{G28}	–	3.5	5	pF	f = 1 MHz
Input leakage current	$-I_{GL}$	–	–	1	μA	V_G = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	1	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	2	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	4.6	6.5	mA	f=1MHz; T_{amb}=25°C
	$-I_{P2}$	–	2.3	3.0	mA	see note 2
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times:						
G → Q_1; Q_3; Q_4; Q_5	t_{DHL}, t_{DLH}	–	150	250	ns	see note 3
G → Q_6; Q_7	t_{DHL}, t_{DLH}	–	125	250	ns	
G → Q_2	t_{DHL}, t_{DLH}	–	175	300	ns	

[1]) All typ. values measured at: T_{amb} = 25 °C; V_{P1} = −26 V; V_{P2} = −13 V

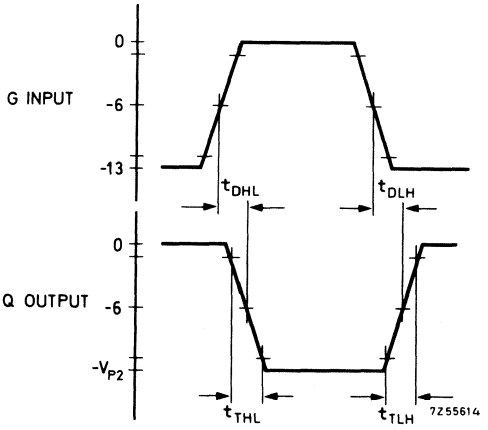
Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.
Note 2: Output buffer power supply current is almost entirely dependent on the external load.
Note 3: Delays are measured at −6 V levels of input and output signals.
(see also timing diagram on page 6).

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. **Input signal rise time:** t_{GLH}
   The time between the 90 % and 10 % voltage points as the input pulse goes from LOW to HIGH.

2. **Input signal fall time:** t_{GHL}
   The time between the 10 % and 90 % voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from LOW to HIGH.

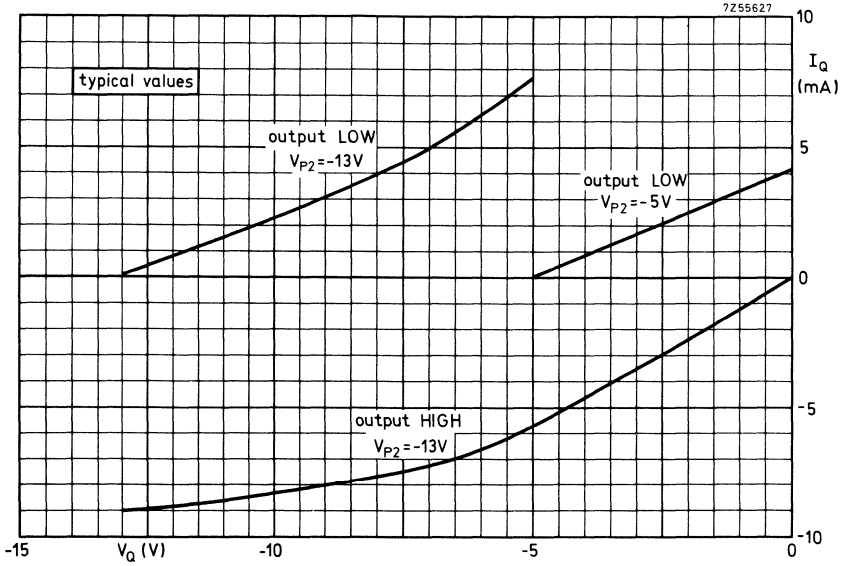
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its -6 V point and the time the output passes -6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90 % and 10 % voltage points as the output goes from LOW to HIGH.

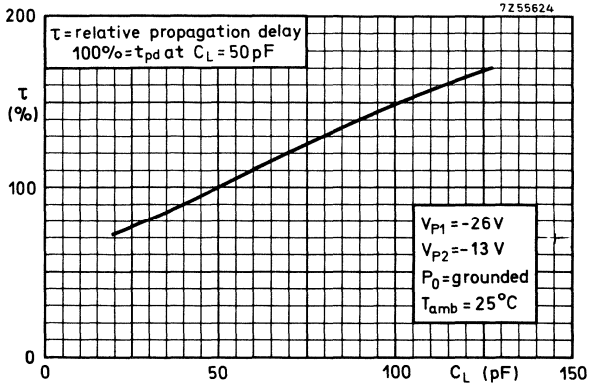
6. Output fall transition time: t_{THL}
   The time between the 10 % and 90 % voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH116 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

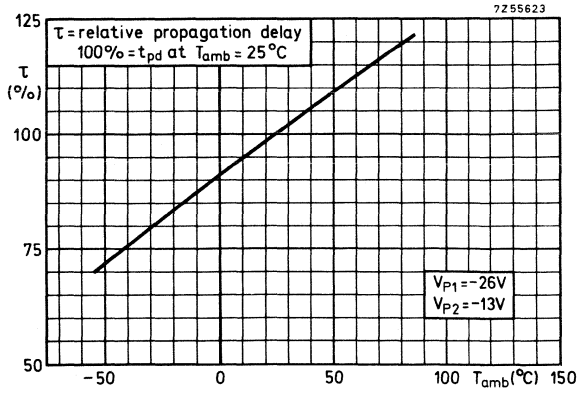


TYPICAL PERFORMANCE at load of C_L in parallel with 1 MΩ to P_0.

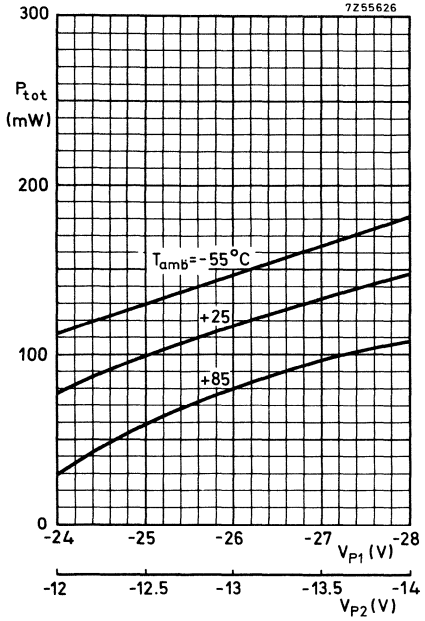


TYPICAL PERFORMANCE (continued)

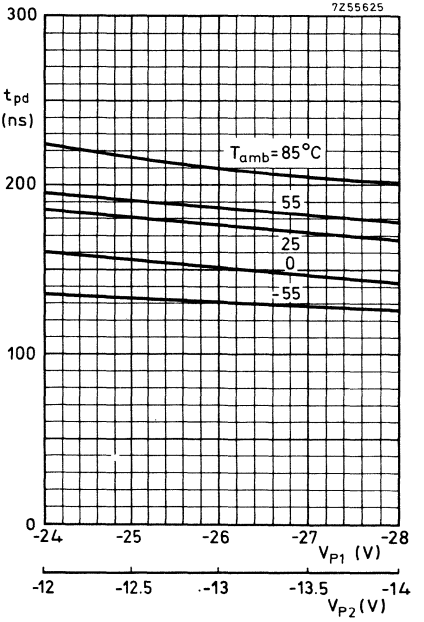
Test conditions: P_0 = grounded; standard load of 50 pF in parallel with 1 MΩ to P_0.



Rated proparation delay as a function of ambient temperature.



Power dissipation as a function of the supply voltage V_{P1} and V_{P2}

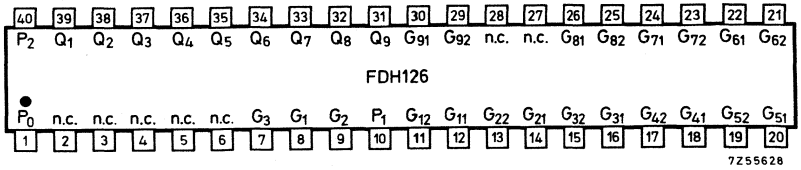


Propagation delay of Q_2 (slowest output) as a function of the supply voltages V_{P1} and V_{P2}.

Note: output buffer power dissipation not included, since it is entirely dependent of loading conditions

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

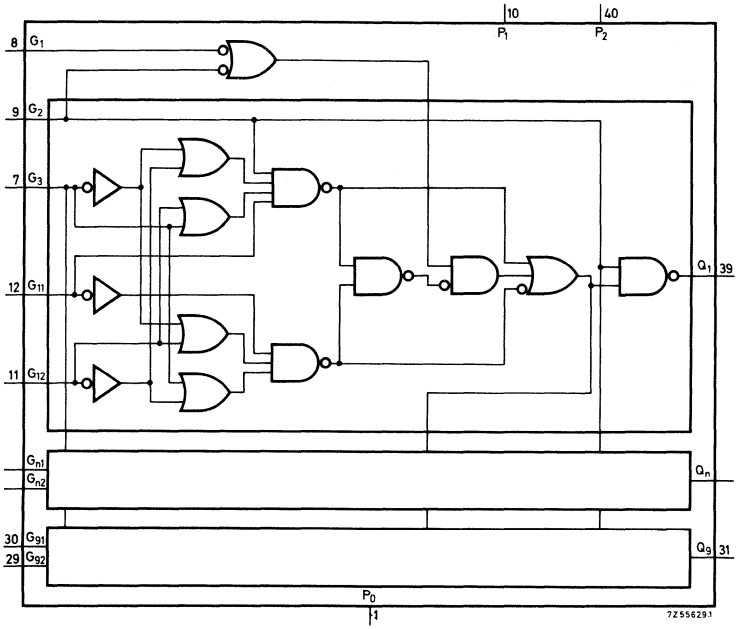
CARRY ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF; T_{amb} = 25 °C	t_{pd}	typ.	250	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power dissipation (f = 1 MHz)	P_{tot}	typ.	260	mW

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)


10
P1
40
P2
8 G1
9 G2
7 G3
12 G11
11 G12
Gn1
Gn2
30 G91
29 G92
Q1 39
Qn
Q9 31
P0
1
7Z556291

GENERAL DESCRIPTION

The FDH126 contains CARRY propagation circuits for a nine stage binary adder/subtractor. It can be cascaded for longer word lengths.
The device is intended to cooperate with the FDH106; e.g. three FDH106 and two FDH126 packages can be put together to make an 18-bit parallel adder/subtractor.
By combining all the CARRY circuits in the same package, a very fast CARRY propagation is obtained.
All inputs are protected against over-voltage caused by static changes.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5 to	−30	V
Power dissipation up to T_{amb} = 70 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Current per output	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	°C/W

FUNCTION TABLE

G_2	G_3	Q_{n-1}	G_{n1}	G_{n2}	Q_n
H	X	H	H	X	H
H	H	H	L	H	L
H	H	H	L	L	H
H	H	L	H	H	L
H	H	L	H	L	H
H	X	L	L	X	L
H	L	H	L	H	H
H	L	H	L	L	L
H	L	L	H	H	H
H	L	L	H	L	L
L	X	X	X	X	L

For n = 1:

$Q_{n-1} = G_1$

H = HIGH state (the less negative voltage)
L = LOW state (the more negative voltage)
X = state is immaterial

LOGIC FUNCTION

Positive logic:

$$Q_n = G_2 \cdot \{G_{n1} \cdot (\overline{G_3} \cdot G_{n2} + G_3 \cdot \overline{G_{n2}}) + Q_{n-1}\,(G_{n1} + \overline{G_3} \cdot G_{n2} + G_3 \cdot \overline{G_{n2}})\}$$

Negative logic:

$$Q_n = G_2 + G_{n1} \cdot (G_3 \cdot G_{n2} + \overline{G_3} \cdot \overline{G_{n2}}) + Q_{n-1}\,(G_{n1} + G_3 \cdot G_{n2} + \overline{G_3} \cdot \overline{G_{n2}})$$

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C
P_0 = grounded; standard load for Q_8 and Q_9: 50 pF in parallel with 1MΩ to P_0; for Q_1 to Q_7, 25 pF in parallel with 1MΩ to P_0.

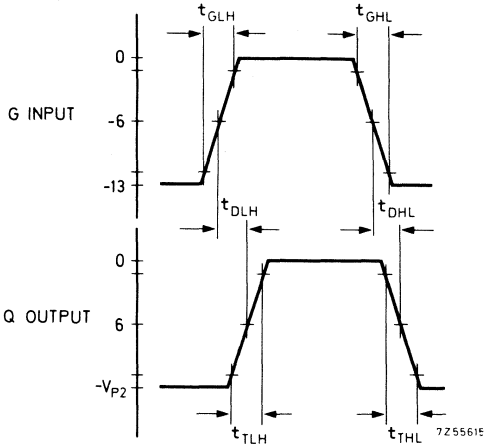
	Symbol	min.	typ.[1]	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	0	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance						
G_1; G_{11} to G_{92}	C_G	–	4.5	6.0	pF	bias: V_G=0 V; f=1 MHz
G_2	C_{G2}	–	6.8	9.0	pF	
G_3	C_{G3}	–	9.5	12.5	pF	
Input leakage current	$-I_{GL}$	–	–	1	μA	V_G=−15 V; T_{amb}=25 °C all other terminals at V_{P0}
Output resistance						
Q_1 to Q_7	R_{QH}	–	1.4	–	kΩ	V_Q = −1 V
	R_{QL}	–	3.7	–	kΩ	V_Q = −10 V
Q_8; Q_9	R_{QH}	–	0.5	–	kΩ	V_Q = −1 V
	R_{QL}	–	1.7	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	8.0	13.0	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	4.0	6.0	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: (any input to output)						
fall time	t_{DHL}	–	250	500	ns	see note
rise time	t_{DLH}	–	250	500	ns	

1) All typ. values measured at: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

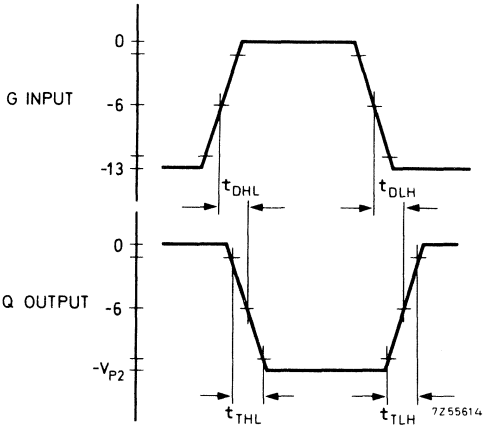
Note: Delays are measured at −6 V levels of input and output signals.
(see also timing diagrams on page 6)

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

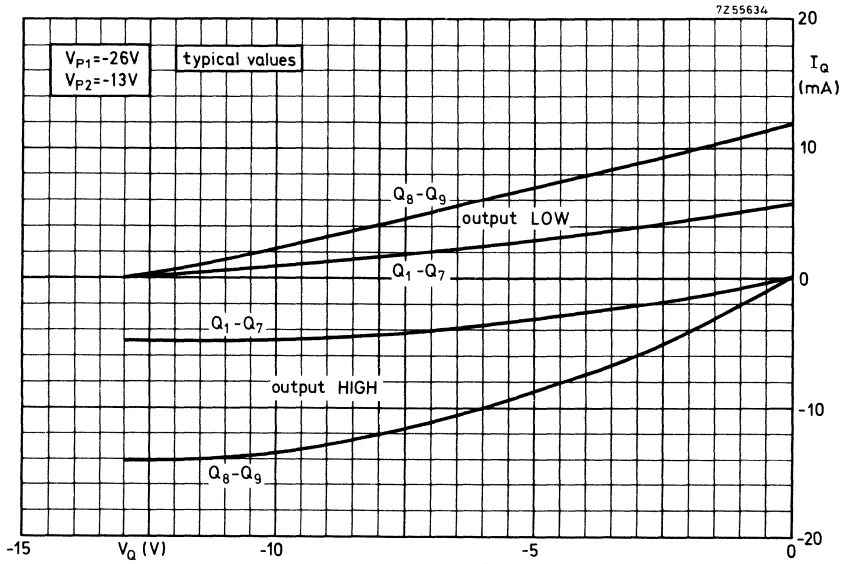
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

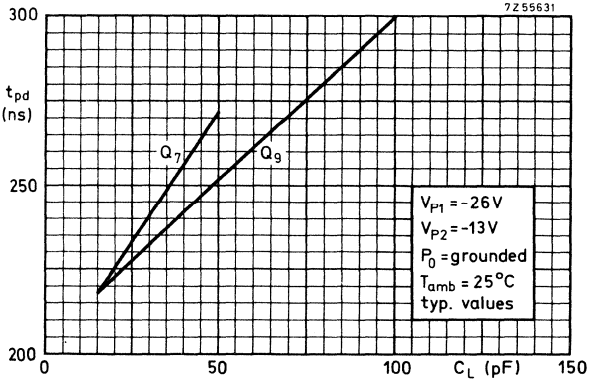
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH126 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

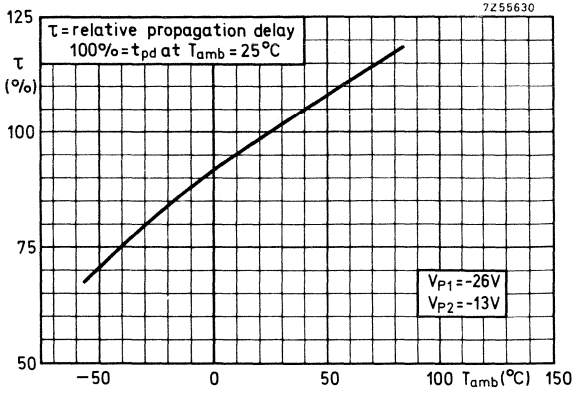


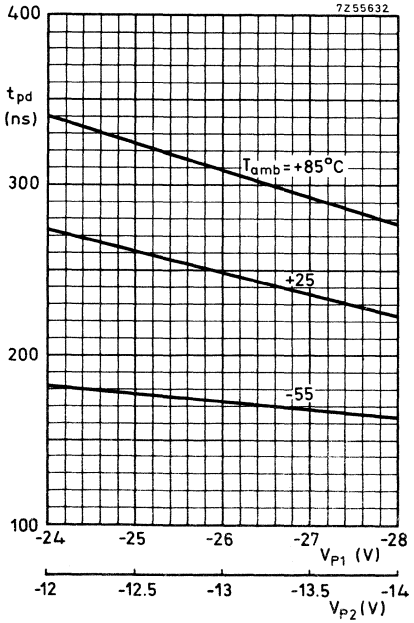
TYPICAL PERFORMANCE at load: C_L in parallel with 1 MΩ to P_0.



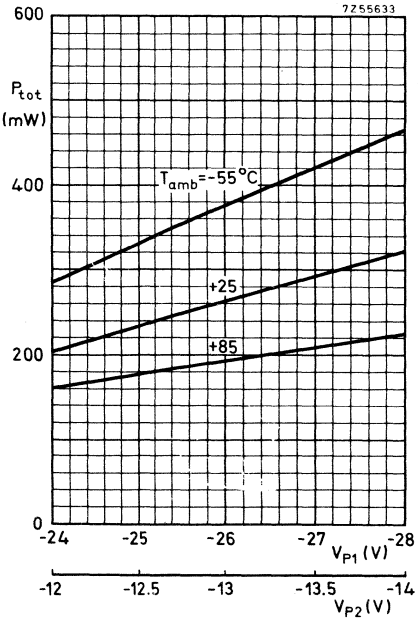
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





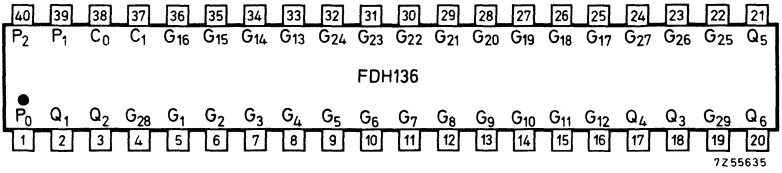
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

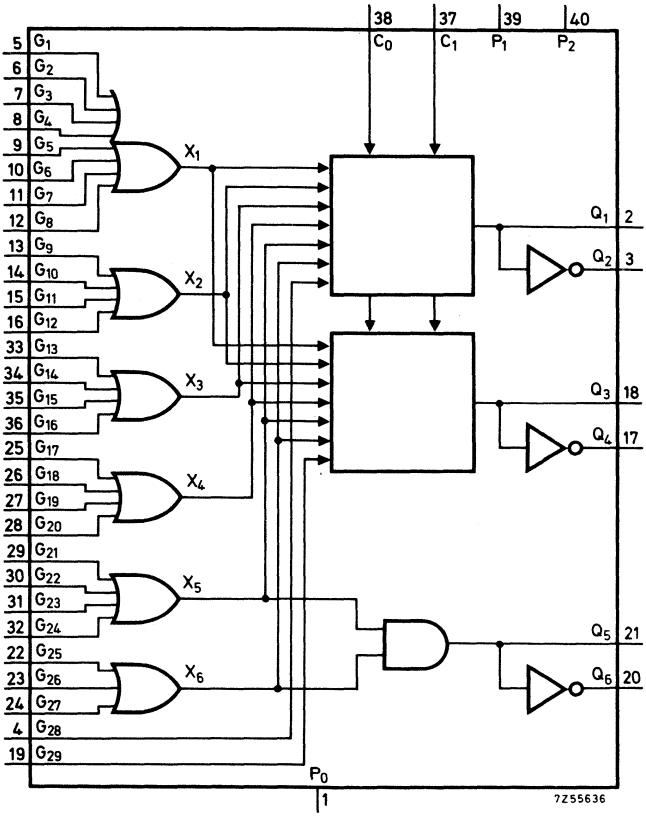
AND-OR GATING ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF; T_{amb} = 25 °C	t_{pd}	typ.	180	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power consumption (f = 1 MHz)	P_{tot}	typ.	230	mW

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)


38 C0
37 C1
39 P1
40 P2
5 G1
6 G2
7 G3
8 G4
9 G5
10 G6
11 G7
12 G8
13 G9
14 G10
15 G11
16 G12
33 G13
34 G14
35 G15
36 G16
25 G17
26 G18
27 G19
28 G20
29 G21
30 G22
31 G23
32 G24
22 G25
23 G26
24 G27
4 G28
19 G29
X1
X2
X3
X4
X5
X6
Q1 2
Q2 3
Q3 18
Q4 17
Q5 21
Q6 20
P0 1
7Z55636

GENERAL DESCRIPTION

The FDH136 contains general purpose, expandable OR/AND/NAND gates.
Two control lines C_0 and C_1 provide four different logic configurations, as shown in the function table.
Complementary outputs are available.
All inputs are protected against over-voltages caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

FUNCTION TABLE

C_0	C_1	logic equation	
		positive logic	negative logic
X	X	$X_1 = G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 + G_8$	$X_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot G_7 \cdot G_8$
		$X_2 = G_9 + G_{10} + G_{11} + G_{12}$	$X_2 = G_9 \cdot G_{10} \cdot G_{11} \cdot G_{12}$
		$X_3 = G_{13} + G_{14} + G_{15} + G_{16}$	$X_3 = G_{13} \cdot G_{14} \cdot G_{15} \cdot G_{16}$
		$X_4 = G_{17} + G_{18} + G_{19} + G_{20}$	$X_4 = G_{17} \cdot G_{18} \cdot G_{19} \cdot G_{20}$
		$X_5 = G_{21} + G_{22} + G_{23} + G_{24}$	$X_5 = G_{21} \cdot G_{22} \cdot G_{23} \cdot G_{24}$
		$X_6 = G_{25} + G_{26} + G_{27}$	$X_6 = G_{25} \cdot G_{26} \cdot G_{27}$
		$Q_5 = X_5 \cdot X_6$	$Q_5 = X_5 + X_6$
		$Q_6 = \overline{X_5} + \overline{X_6}$	$Q_6 = \overline{X_5} \cdot \overline{X_6}$
L	L	$Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot G_{28}$	$Q_1 = X_1 + X_2 + X_3 + G_{28}$
		$Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{G_{28}}$	$Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{G_{28}}$
		$Q_3 = X_4 \cdot X_5 \cdot X_6 \cdot G_{29}$	$Q_3 = X_4 + X_5 + X_6 + G_{29}$
		$Q_4 = \overline{X_4} + \overline{X_5} + \overline{X_6} + \overline{G_{29}}$	$Q_4 = \overline{X_4} \cdot \overline{X_5} \cdot \overline{X_6} \cdot \overline{G_{29}}$

FUNCTION TABLE (continued)

C_0	C_1	logic equation	
		positive logic	negative logic
L	H	$Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot X_5 \cdot X_6 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{X_4} + \overline{X_5} + \overline{X_6} + \overline{G_{28}}$ $Q_3 = X_1 \cdot X_2 \cdot G_{29}$ $Q_4 = \overline{X_1} + \overline{X_2} + \overline{G_{29}}$	$Q_1 = X_1 + X_2 + X_3 + X_4 + X_5 + X_6 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{X_4} \cdot \overline{X_5} \cdot \overline{X_6} \cdot \overline{G_{28}}$ $Q_3 = X_1 + X_2 + G_{29}$ $Q_4 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{G_{29}}$
H	L	$Q_1 = X_1 \cdot X_2 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{G_{28}}$ $Q_3 = X_3 \cdot X_4 \cdot G_{29}$ $Q_4 = \overline{X_3} + \overline{X_4} + \overline{G_{29}}$	$Q_1 = X_1 + X_2 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{G_{28}}$ $Q_3 = X_3 + X_4 + G_{29}$ $Q_4 = \overline{X_3} \cdot \overline{X_4} \cdot \overline{G_{29}}$
H	H	$Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{X_4} + \overline{G_{28}}$ $Q_3 = X_5 \cdot X_6 \cdot G_{29}$ $Q_4 = \overline{X_5} + \overline{X_6} + \overline{G_{29}}$.	$Q_1 = X_1 + X_2 + X_3 + X_4 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{X_4} \cdot \overline{G_{28}}$ $Q_3 = X_5 + X_6 + G_{29}$ $Q_4 = \overline{X_5} \cdot \overline{X_6} \cdot \overline{G_{29}}$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load : 50 pF in parallel with 1 MΩ to P_0.

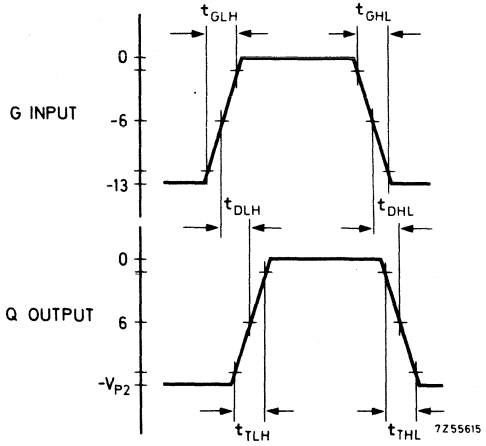
	Symbol	min.	typ.[1])	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}, V_{CH}	−2	–	+0.3	V	
LOW	V_{GL}, V_{CL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance	G_G, C_C	–	3	5.5	pF	bias: $V_G = V_C = 0$ V; f = 1 MHz
Leakage current	$-I_{GL}$, $-I_{CL}$	–	–	1	mA	$V_G = V_C = -15$ V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	0.4	–	kΩ	V_Q = −1V
LOW	R_{QL}	–	1	–	kΩ	V_Q = −10V
Supply currents	$-I_{P1}$	–	4.5	7.5	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	8	13	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times: (any input to output)						
fall time	t_{DHL}	–	180	400	ns	
rise time	t_{DLH}	–	180	400	ns	
Control input sink current: G_1;G_2;G_4;G_5; G_7;G_8;G_{10};G_{12},G_{13}; G_{15};G_{17};G_{19};G_{21};G_{23}; G_{26};C_0;C_1	$-I_G$, $-I_C$	–	25	–	µA	$V_G = V_C = -2$ V; see note

[1]) Typical values are measured at V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

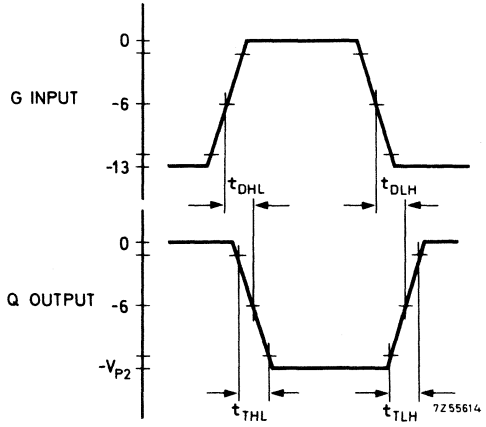
Note: Inputs mentioned are provided with a pull-down resistor to terminal P_2. These inputs, when not used, may be left floating; they will then be in the LOW state.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

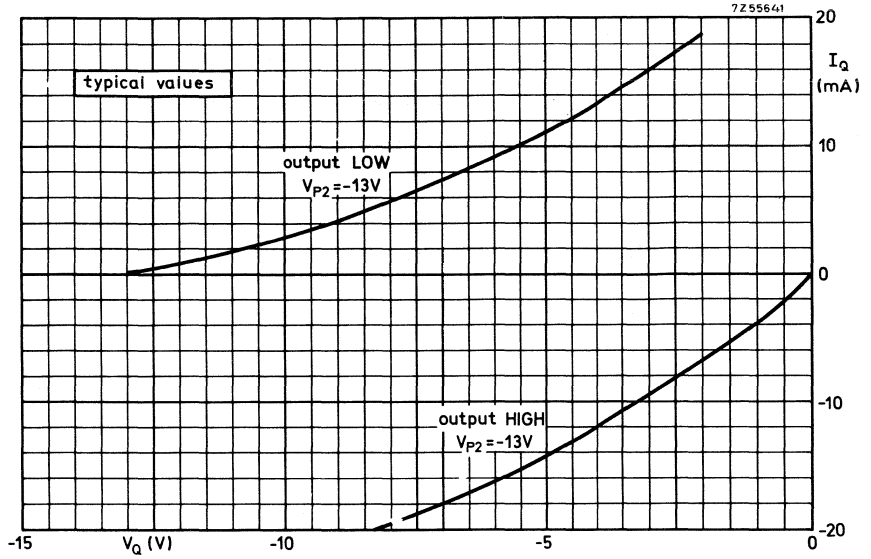
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

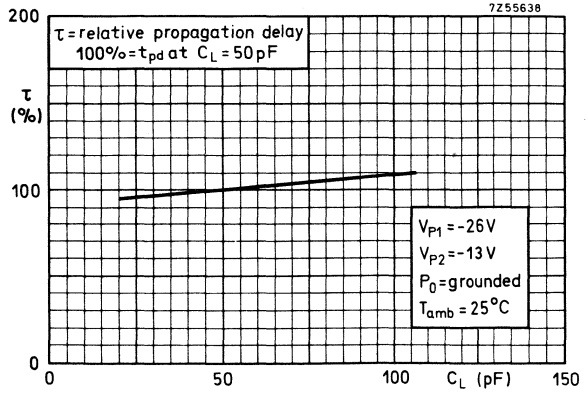
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH136 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

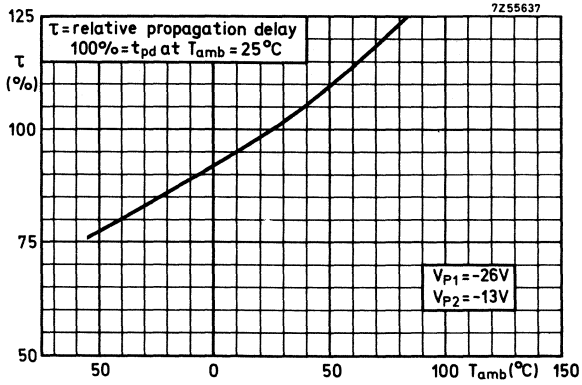


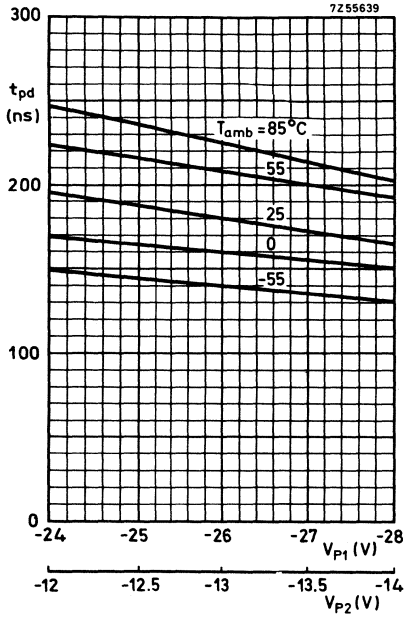
TYPICAL PERFORMANCE at load C_L in parallel with 1 MΩ to P_0.



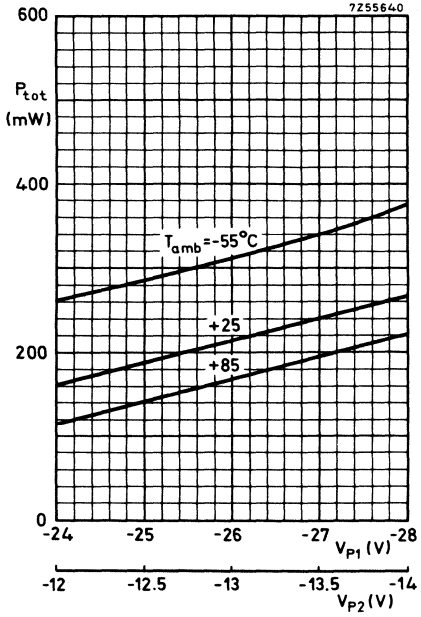
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load of 50 pF in parallel with 1 MΩ to P_0.





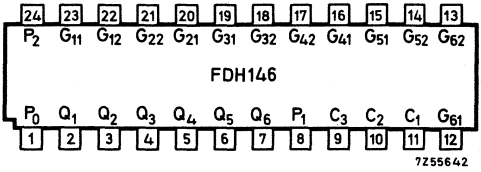
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

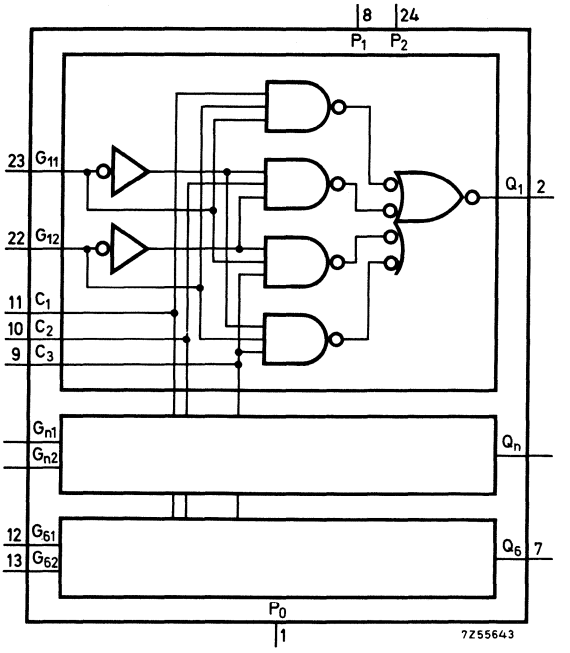
VARIABLE GATE ARRAY



P_0 and metal lid on bottom of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF; T_{amb} = 25 °C	t_{pd}	typ.	250	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Average power consumption per function (f = 1 MHz)	P_{av}	typ.	35	mW

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section)


8
24
P1
P2
23
G11
22
G12
11
C1
10
C2
9
C3
Q1
2
Gn1
Gn2
Qn
12
G61
13
G62
Q6
7
P0
1
7Z55643

GENERAL DESCRIPTION

The FDH146 consists of six, identical, 2-input gate networks. Three coded control lines determine the function of the six gate networks, so that eight different functions can be selected; the selected function is available six times.
The control inputs have pull-down resistors connected to P_2, so that they assume the LOW state, when left floating.
All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max. 1	W
Junction temperature	T_j	max. 150	°C
Storage temperature	T_{stg}	−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max. 40	mA
Output current per output	$\pm I_Q$	max. 20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	= 125	°C/W

FUNCTION TABLE

C_3	C_2	C_1	logic equation (positive logic)	logic function	
				positive logic	negative logic
L	L	L	$Q_n = 1$	–	–
L	L	H	$Q_n = \overline{G_{n1} \cdot G_{n2}}$	NAND	NOR
L	H	L	$Q_n = G_{n1} + G_{n2}$	OR	AND
L	H	H	$Q_n = G_{n1} \cdot \overline{G_{n2}} + \overline{G_{n1}} \cdot G_{n2}$	exclusive-OR	comparator
H	L	L	$Q_n = G_{n1} \cdot G_{n2} + \overline{G_{n1}} \cdot \overline{G_{n2}}$	comparator	exclusive-OR
H	L	H	$Q_n = \overline{G_{n1} + G_{n2}}$	NOR	NAND
H	H	L	$Q_n = G_{n1} \cdot G_{n2}$	AND	OR
H	H	H	$Q_n = 0$	–	–

CHARACTERISTICS

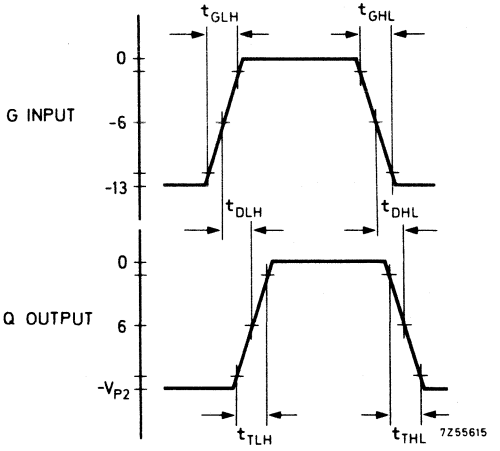
Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load : 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1]	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	0	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance						
C_1; C_2	C_{C1}, C_{C2}	–	5.5	7	pF	bias: V_G = 0V; f = 1MHz
C_3	C_{C3}	–	9.5	11	pF	
G_{11} to G_{62}	C_{G11} to C_{G62}	–	3.5	5	pF	
Input leakage current	$-I_{GL}$	–	–	1	μA	V_G=−15V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	1.0	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	2.0	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	4.6	7.0	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	6.2	8.5	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times (any input to output)						
fall time	t_{DHL}	–	250	400	ns	
rise time	t_{DLH}	–	250	400	ns	
Control input sink current: C_1, C_2	$-I_{C1}$; $-I_{C2}$	–	32	–	μA	V_G = −2 V
C_3	$-I_{C3}$	–	64	–	μA	

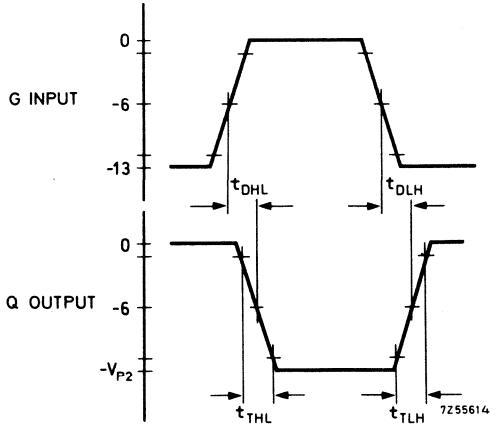
[1]) All typ. values are measured at: T_{amb} = 25 °C and V_{P1} = −26 V, V_{P2} = −13 V.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input pulse rise time: t_{GLH}
   The time between the 90 % and 10 % voltage points as the input pulse goes from LOW to HIGH.

2. Input pulse fall time: t_{GHL}
   The time between the 10 % and 90 % voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

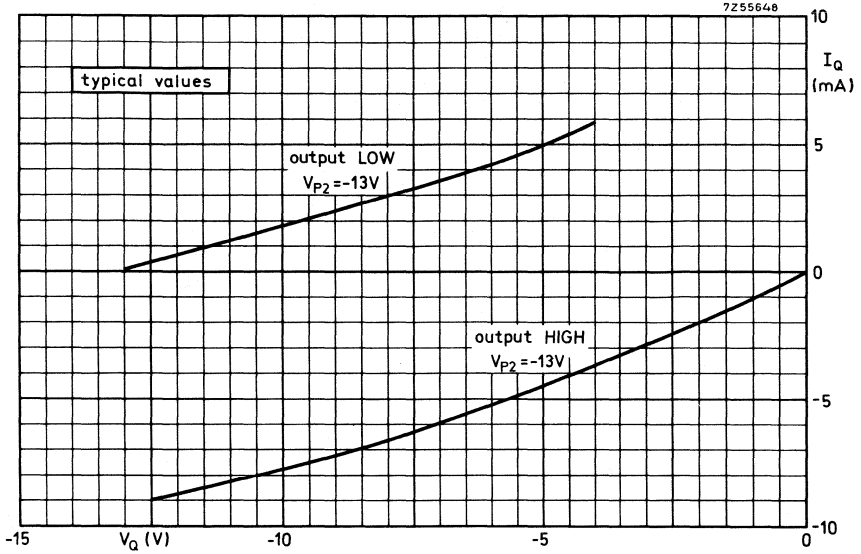
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90 % and 10 % voltage points as the output goes from LOW to HIGH.

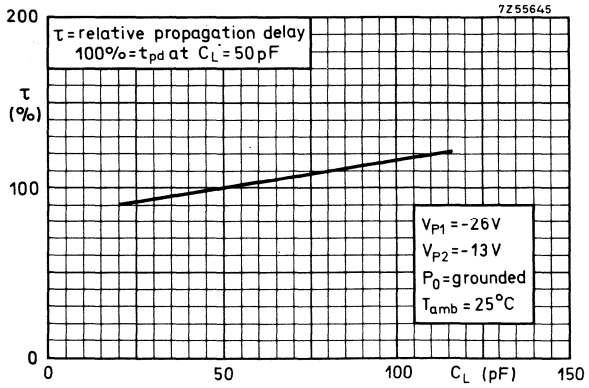
6. Output fall transition time: t_{THL}
   The time between the 10 % and 90 % voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH146 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

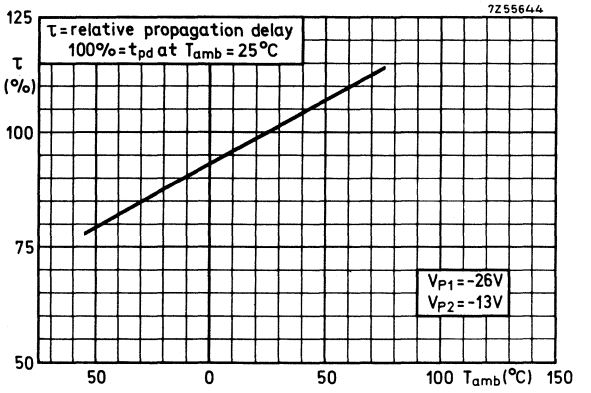


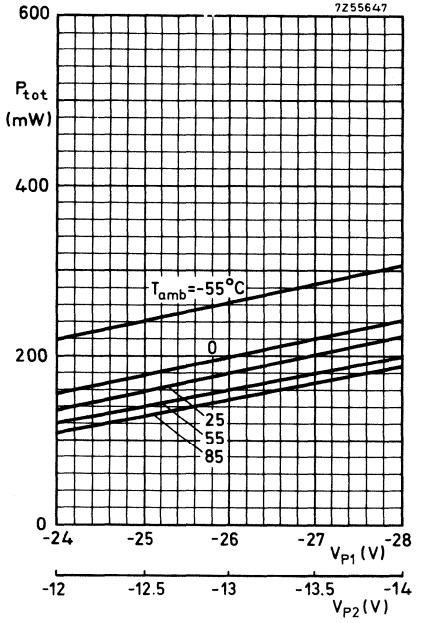
TYPICAL PERFORMANCE at load: C_L in parallel with 1 MΩ to P_0



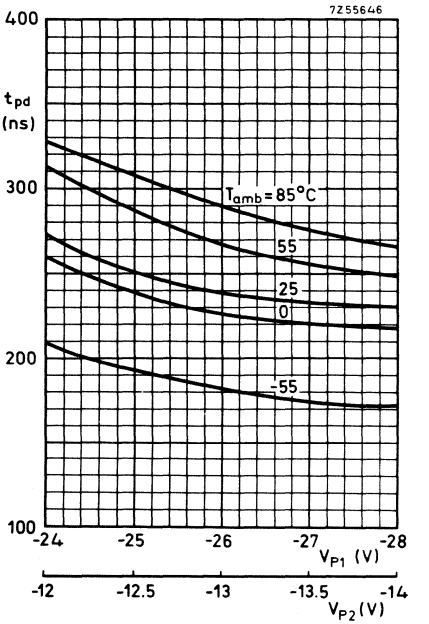
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





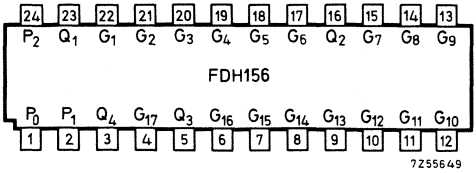
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

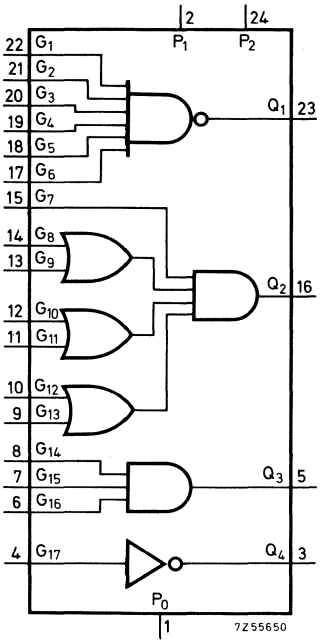
FIXED LOGIC ARRAY



P_0 and metal lid on bottom of the package connected

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF	t_{pd}	typ.	150	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power dissipation f = 1 MHz; C_L = 50 pF	P_{tot}	typ.	160	mW

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section)


2
24
22 G1
21 G2
20 G3
19 G4
18 G5
17 G6
15 G7
14 G8
13 G9
12 G10
11 G11
10 G12
9 G13
8 G14
7 G15
6 G16
4 G17
P1
P2
Q1 23
Q2 16
Q3 5
Q4 3
P0
1
7Z55650

GENERAL DESCRIPTION

The FDH156 contains all the logic functions shown in the diagram and described in the logic functions below. It is intended to perform logic functions in all MOS digital systems. The output voltage swing is determined by the output buffer supply voltage (V_{P2}).
All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	°C/W

LOGIC FUNCTIONS

Positive logic

$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6}$

$Q_2 = G_7 \cdot (G_8 + G_9) \cdot (G_{10} + G_{11}) \cdot (G_{12} + G_{13})$

$Q_3 = G_{14} \cdot G_{15} \cdot G_{16}$

$Q_4 = \overline{G_{17}}$

Negative logic

$Q_1 = \overline{G_1 + G_2 + G_3 + G_4 + G_5 + G_6}$

$Q_2 = G_7 + (G_8 \cdot G_9) + (G_{10} \cdot G_{11}) + (G_{12} \cdot G_{13})$

$Q_3 = G_{14} + G_{15} + G_{16}$

$Q_4 = \overline{G_{17}}$

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V (see note 1); T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1])	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	0	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance	C_G	–	5	7	pF	bias: V_G=0; f = 1 MHz
Input leakage current	$-I_{GL}$	–	–	1	μA	V_G=−15V; T_{amb}=25°C all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	1	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	2	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	4.6	6.5	mA	f = 1 MHz; T_{amb} = 25°C see note 2
	$-I_{P2}$	–	2.3	3.0	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times (fall and rise times)						
G → Q_1	t_{DHL}, t_{DLH}	–	175	300	ns	see note 3
G → Q_2; Q_3	t_{DHL}, t_{DLH}	–	150	250	ns	
G → Q_4	t_{DHL}, t_{DLH}	–	125	250	ns	

Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

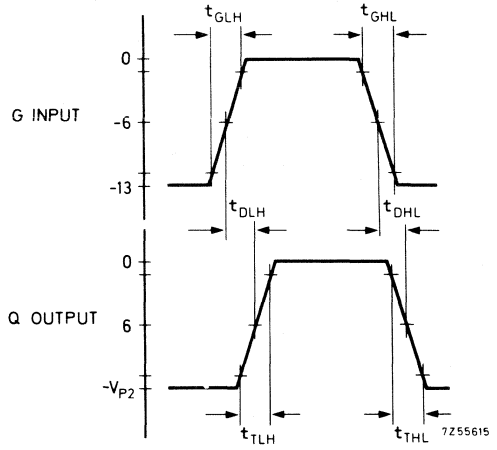
Note 2: Output buffer supply current is almost entirely dependent on the external load.
The value shown is for a load: 50 pF in parallel with 1 MΩ to P_0.

Note 3: Delays are measured at −6 V levels of input and output signals.
(see also timing diagram on page 5)

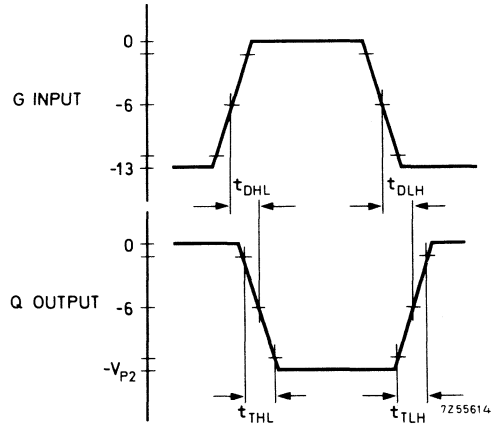
[1]) All typ. values are measured at: T_{amb} = 25 °C ; V_{P1} = −26 V; V_{P2} = −13 V.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

$V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $t_{GLH} = t_{GHL} = 150$ ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at −6 V point and the time the output passes −6 V when going from LOW to HIGH.

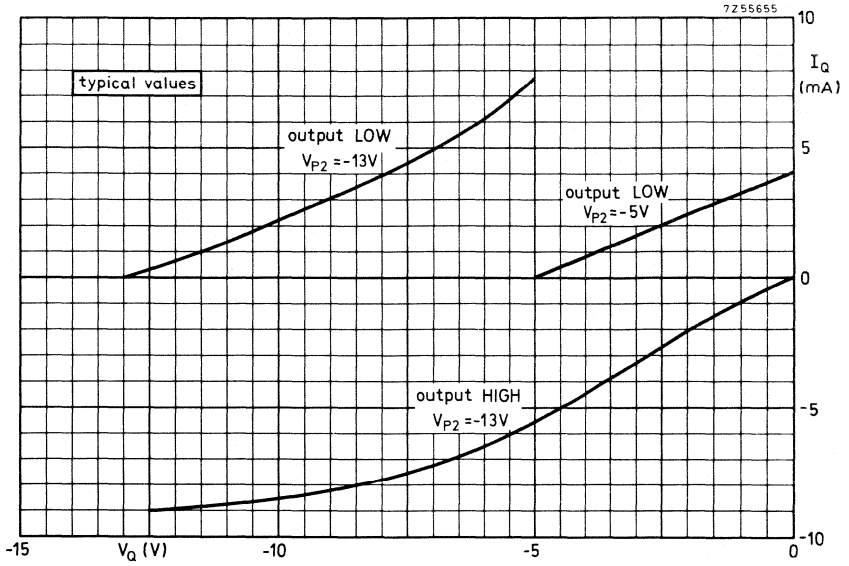
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

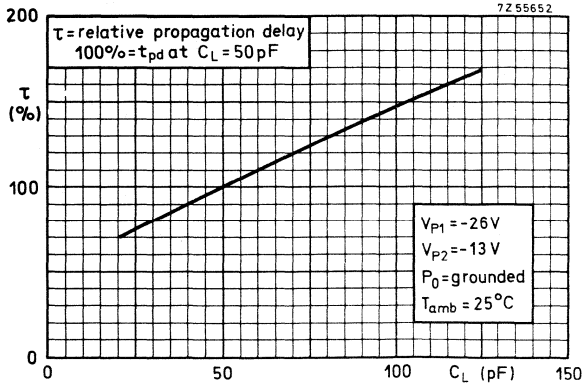
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH156 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

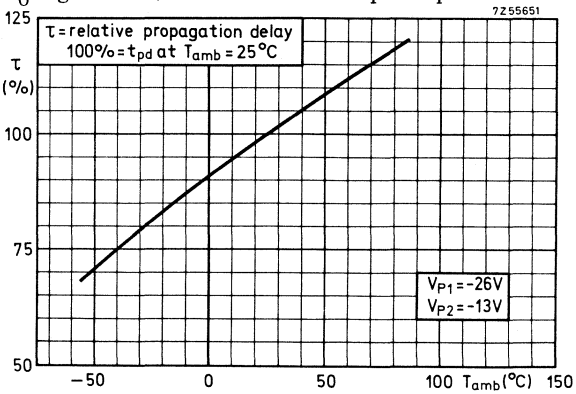


TYPICAL PERFORMANCE at load: C_L in parallel with 1 MΩ to P_0.

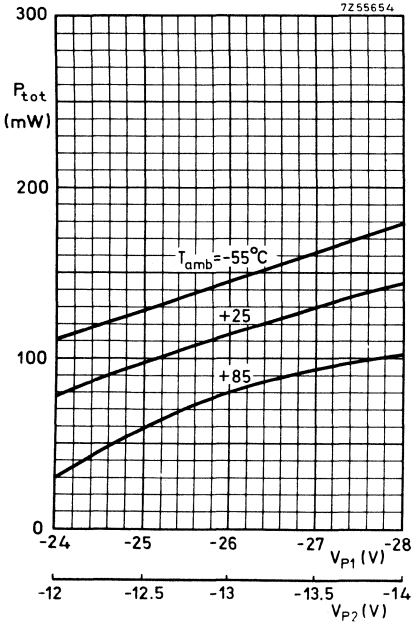


TYPICAL PERFORMANCE (continued)

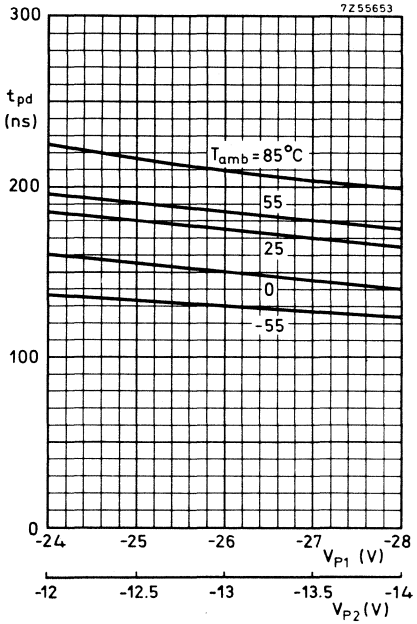
Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.



Rated propagation delay as a function of ambient temperature.



Power dissipation as a function of the supply voltages V_{P1} and V_{P2}

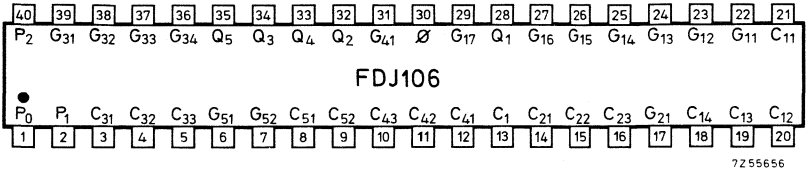


Propagation delay of Q_2 (slowest output) as a function of the supply voltages V_{P1} and V_{P2}.

Note: output buffer power dissipation not included, since it is entirely dependent of loading conditions

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

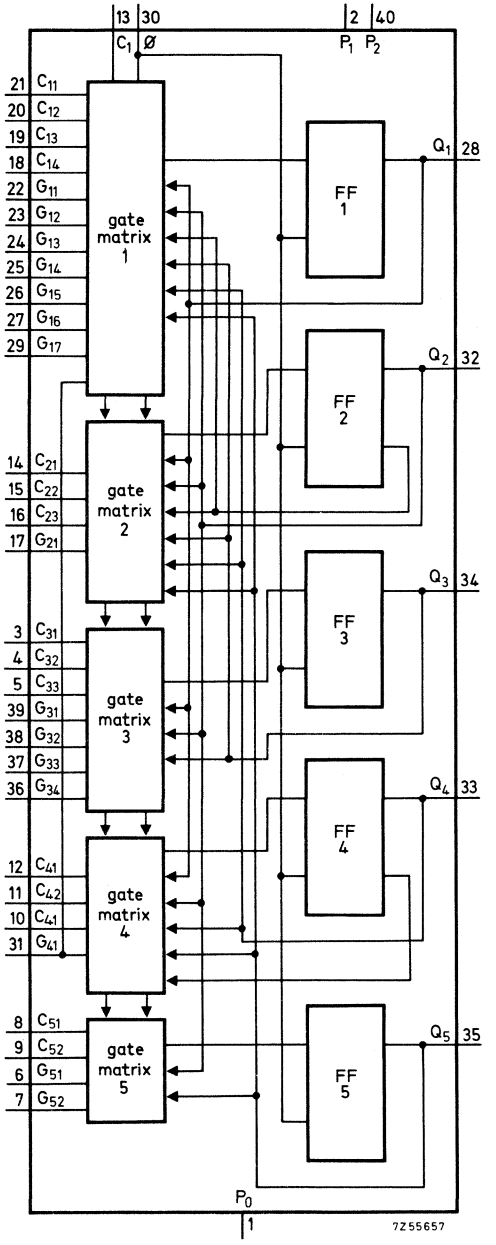
REGISTER ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}		−24 to −28	V
Operating ambient temperature	T_{amb}		−55 to +85	°C
Cycle time		typ.	400	ns
Propagation delay time at C_L = 50 pF	t_{pd}	typ.	150	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power dissipation $f\phi$ = 1 MHz; C_L = 50 pF	$P_{tot.}$	typ.	180	mW

PACKAGE OUTLINE : 40 lead ceramic dual in-line (See General Section)


13 30
C1 Ø
2 40
P1 P2
21 C11
20 C12
19 C13
18 C14
22 G11
23 G12
24 G13
25 G14
26 G15
27 G16
29 G17
gate matrix 1
FF 1
Q1 28
14 C21
15 C22
16 C23
17 G21
gate matrix 2
FF 2
Q2 32
3 C31
4 C32
5 C33
39 G31
38 G32
37 G33
36 G34
gate matrix 3
FF 3
Q3 34
12 C41
11 C42
10 C41
31 G41
gate matrix 4
FF 4
Q4 33
8 C51
9 C52
6 G51
7 G52
gate matrix 5
FF 5
Q5 35
P0
1
7Z55657

GENERAL DESCRIPTION

The FDJ106 is an array of 5 flip-flops, designed to act as a synchronous bit slice of a CPU.
Each of the 5 D-type flip-flops has at least one external input and output, as well as individually controlled transfer and input SELECT logic.
The input gating matrix can therefore enable transfers from external inputs or from other registers in the same array.
The register array contains one bit of each of the five main registers in most computers:

FF1 - accumulator
FF2 - memory data register
FF3 - multiplier/quotient register
FF4 - program counter
FF5 - instruction register

All inputs are protected against over-voltage caused by static charge.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0			+0.5 to	− 30	V
Power dissipation up to T_{amb} = 25 °C	$P_{tot.}$	max.		1	W
Junction temperature	T_j	max.		150	°C
Storage temperature	T_{stg}		−65 to	+150	°C
Total current through terminal P_2	$-I_{P2}$	max.		40	mA
Current per output	$\pm I_Q$	max.		20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

LOGIC FUNCTION

REGISTER INPUT SELECTION TABLE

The FDJ106 outputs will conform to the following input transfer function table. With the given set of control inputs, including C_1, which is common to all gate matrices, each flip-flop will have at its D-input the signal shown in the table below.
With the control inputs established, the output of each register will assume the state of its input after the positive going edge of ϕ.

control input (for any gate matrix)				Flip-flop inputs									
				C_1 : HIGH					C_1 : LOW				
C_{n4}	C_{n3}	C_{n2}	C_{n1}	FF1	FF2	FF3	FF4	FF5	FF1	FF2	FF3	FF4	FF5
L	L	L	L	H					G_{41}				
L	L	L	H	G_{17}					G_{17}				
L	L	H	L	G_{16}					G_{16}				
L	L	H	H	G_{15}					G_{15}				
L	H	L	L	G_{14}					G_{14}				
L	H	L	H	G_{13}					G_{13}				
L	H	H	L	G_{12}					G_{12}				
L	H	H	H	G_{11}					G_{11}				
H	L	L	L	H	H	G_{34}	H		Q_1	$\overline{Q_2}$	G_{34}	$\overline{Q_4}$	
H	L	L	H	H	H	G_{33}	H		Q_1	H	G_{33}	H	
H	L	H	L	Q_5	Q_5	G_{32}	G_{41}		Q_1	G_{21}	G_{32}	L	
H	L	H	H	Q_4	Q_{21}	G_{31}	H		Q_1	Q_2	G_{31}	Q_4	
H	H	L	L	$\overline{Q_2}$	Q_4	H	Q_1	G_{52}	Q_1	Q_2	Q_3	Q_4	G_{52}
H	H	L	H	Q_2	Q_1	Q_2	Q_2	G_{51}	Q_1	Q_2	Q_3	Q_4	G_{51}
H	H	H	L	Q_3	Q_3	Q_1	Q_5	Q_2	Q_1	Q_2	Q_3	Q_4	Q_5
H	H	H	H	Q_1	Q_2	Q_3	Q_4	Q_5	Q_1	Q_2	Q_3	Q_4	Q_5

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

DRIVE REQUIREMENTS	Symbol	min.	typ.[1])	max.		Conditions and references
Data and control input logic levels (except C_1)						
HIGH	V_{GH}, V_{CH}	−2	–	+0.3	V	
LOW	V_{GL}, V_{CL}	−28	–	−9	V	
C_1 input levels						
HIGH	V_{C1H}	−2	–	0.3	V	
LOW	V_{C1L}	−28	–	−24	V	
Clock pulse width	$t_{\phi L}$	0.25	–	1.0	µs	see timing diagram on page 7
Clock pulse transition times	$t_{\phi LH}$, $t_{\phi HL}$	–	–	0.1	µs	see timing diagram on page 7
Clock pulse voltage levels: HIGH	$V_{\phi H}$	−2	–	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	

[1]) All typical values are measured at: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

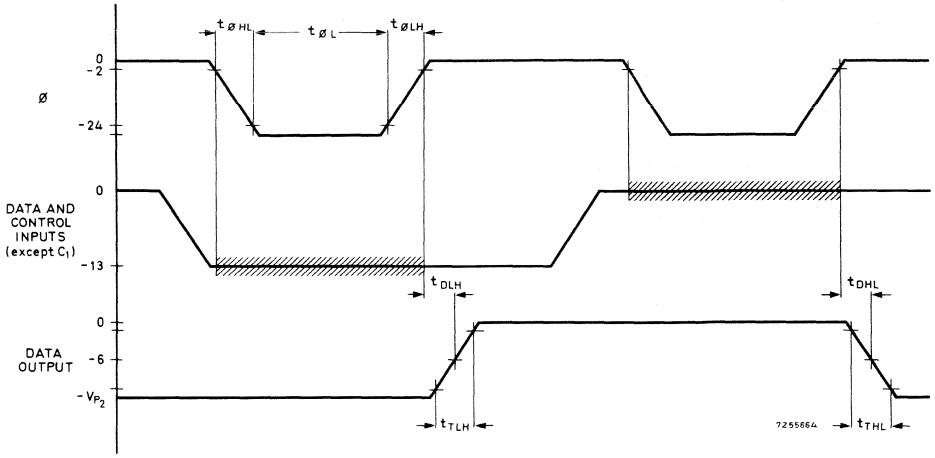
Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load : 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1]	max.		Conditions and references
Output logic levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance						
data and control (except C_1)	C_G, C_C	–	4	7.5	pF	bias: $V_G = V_C$ = 0 V; f = 1 MHz
C_1	C_{C1}	–	7	10	pF	bias: V_{C1} = 0 V; f = 1 MHz
clock input	C_ϕ	–	20	25	pF	bias: V_ϕ = 0 V; f = 1 MHz
Input leakage current						
data and control (except C_1)	$-I_{GL}, -I_{CL}$	–	–	1	µA	bias: $V_G = V_C$ = −15 V; T_{amb} = 25 °C; all other terminals at V_{P0}
C_1	$-I_{C1L}$	–	–	100	µA	bias: V_{C1} = −28 V; T_{amb} = 25 °C; all other terminals at V_{P0}
clock input	$-I_{\phi L}$	–	–	100	µA	bias: V_ϕ = −28 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	1.0	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	1.0	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	6.0	10.0	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	1.6	2.5	mA	f = 1 MHz; T_{amb} = 25 °C
Output transition times: fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times:						
fall time	t_{DHL}	–	150	300	ns	
rise time	t_{DLH}	–	150	300	ns	

[1]) All typical values are measured at: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



Note:
The indicated points on the vertical axis are specified in the glossary of terms.

Timing diagram notes:

1. Data and control inputs must remain valid for the shaded interval to ensure proper entry.
2. C_1 may be switched in the same manner as all other inputs, providing it completes its switching transition before input G_{41} becomes LOW, for any given clock pulse.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V.

2. Clock pulse rise time: $t_{\phi LH}$
   The time between the −24 V and −2 V voltage points as the clock pulse goes from LOW to HIGH.

3. Clock pulse fall time: $t_{\phi HL}$
   The time between the −2 V and −24 V voltage points as the clock pulse goes from HIGH to LOW.

4. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

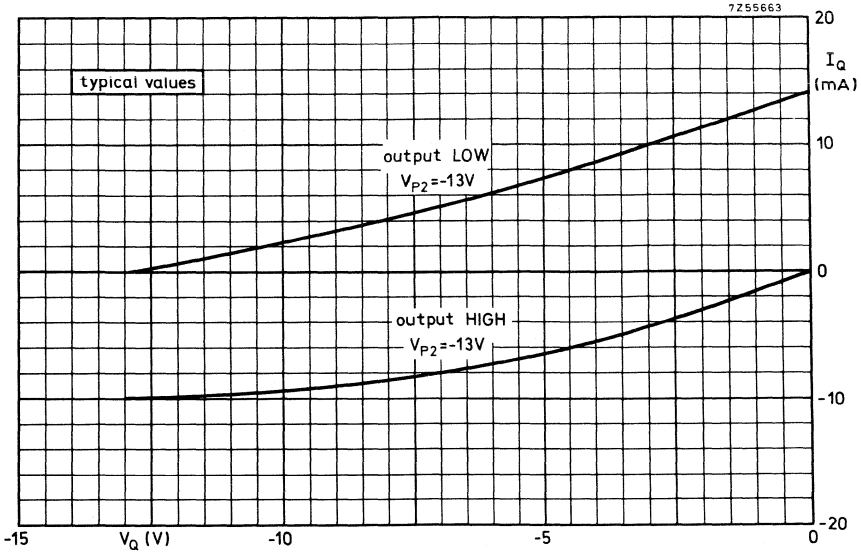
5. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

6. Fall delay time: t_{DHL}
   The delay between the time the positive going edge of the clock pulse arrives at −2 V and the output −6 V voltage point as the output goes from HIGH to LOW.

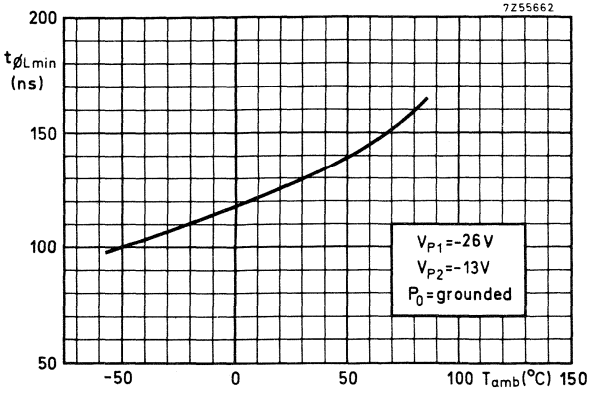
7. Rise delay time: t_{DLH}
   The delay between the time the positive going edge of the clock pulse arrives at −2 V and the output −6 V voltage point as the output goes from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

The FDJ106 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

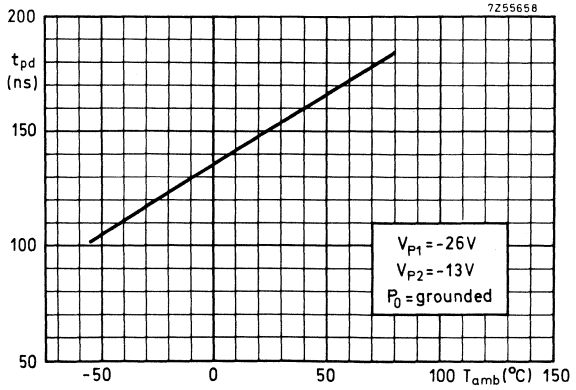


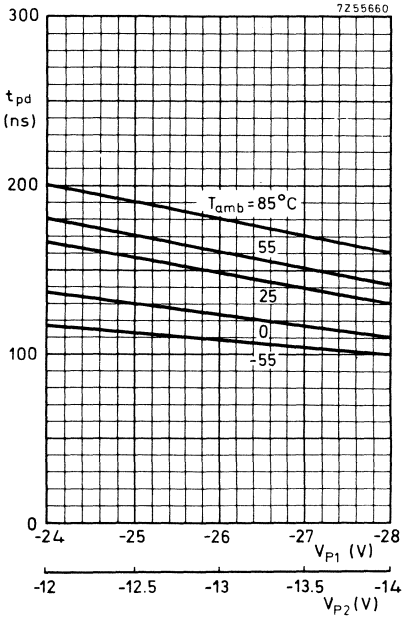
TYPICAL PERFORMANCE



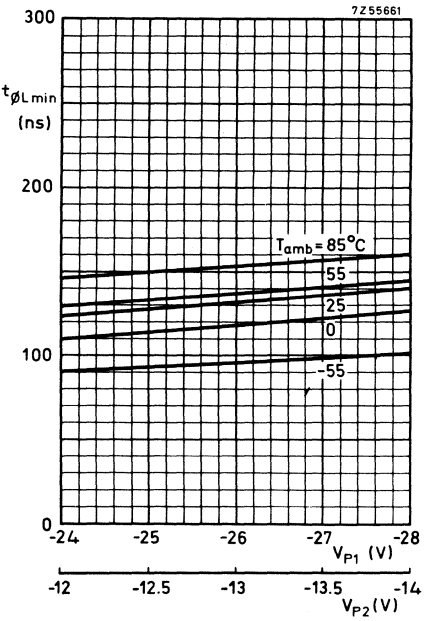
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





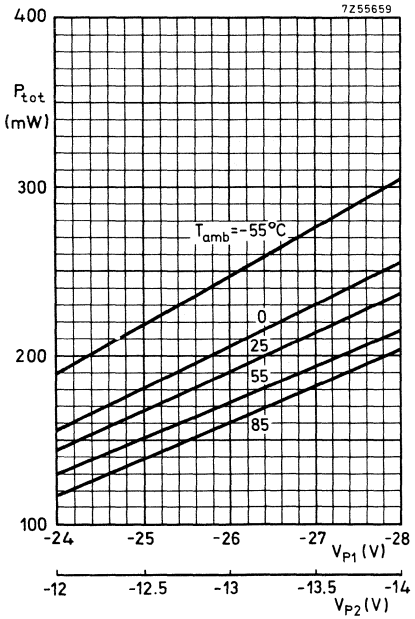
Propagation delay as a function of the supply voltages V_{P1} and V_{P2}



Minimum clock pulse width as a function of the supply voltages V_{P1} and V_{P2}

TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

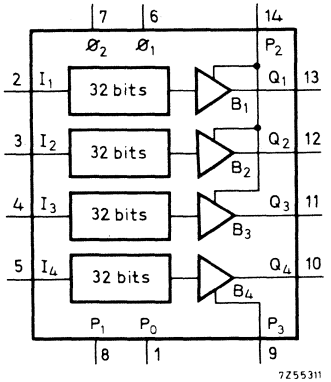


Power dissipation as a function of the supply voltages V_{P1} and V_{P2}

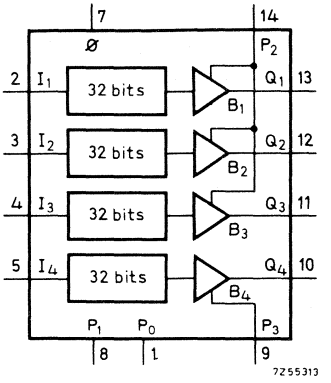
The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

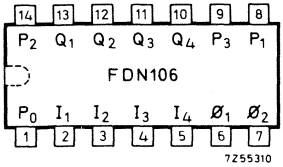
QUADRUPLE 32-BIT DYNAMIC SHIFT REGISTERS

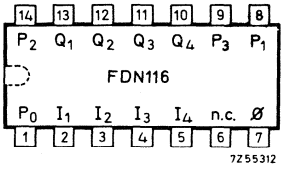
FDN106



FDN116







P_0 and metal package bottom are connected.

QUICK REFERENCE DATA			
Supply voltage	V_{P_1}	−24 to −28	V
D.C. noise margin	M_L; M_H	> 1	V
Clock rate: FDN106	f_ϕ	0.01 to 3	MHz
FDN116	f_ϕ	0.01 to 1	MHz
Power consumption per bit at 1 MHz: FDN106	P_{av}	typ. 0.6	mW
FDN116	P_{av}	typ. 1.0	mW
Power dissipation	P_{tot}	max. 300	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE: 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN106 and FDN116 packages comprise 4 separate 32-bit shift registers that can be used independently or can be externally connected to make registers up to 128-bits long. Clock and power lines are common to all four registers. The output buffers are bi-directional, low impedance NRZ [1]), that by suitable biasing will directly drive MOS, DTL or TTL loads or, because they have separate supply voltages (V_{P_2}; V_{P_3}), a combination of MOS and bipolar. V_{P_2} and V_{P_3} are output buffer voltages only, and the output LOW signal is independent of the width and amplitude of the clock pulse.

The FDN106 uses a two-phase external clock, has low power dissipation and will operate at high speed.

The FDN116 uses a single phase external clock, and is for applications not calling for the low power economy and high speed of the FDN106.

With the FDN106; FDN116; the FDN126; FDN136 (variable length 1 to 64-bit dynamic shift registers) and the FDN146; FDN156 (256-bit dynamic shift registers) shift registers of any length can be built from off-the shelf parts.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0		+0.5 to	−30	V
Power disspation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminals P_2 and P_3	$-I_{P2}$, $-I_{P3}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	156	°C/W

[1]) Non return to zero.

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	Type number	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	FDN106	0.01	–	3 MHz	
	f_ϕ	FDN116	0.01	–	1 MHz	
Clock pulse width	$t_{\phi 1L}$	FDN106	0.125	–	25 µs	see timing diagram for parameter def.
	$t_{\phi 2L}$	FDN106	0.125	–	25 µs	
	$t_{\phi L}$	FDN116	0.50	–	50 µs	
Clock pulse fall time	$t_{\phi HL}$		–	–	0.10 µs	see note 1, 2
Clock pulse rise time	$t_{\phi LH}$		–	–	0.10 µs	see note 2
Clock delay time	$t_{\phi 1\phi 2}$	FDN106	0	–	25 µs	
Clock delay time	$t_{\phi 2\phi 1}$	FDN106	0	–	25 µs	
Clock pulse space	$t_{\phi H}$	FDN116	0.50	–	50 µs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$		−2	0	+0.3 V	
LOW	$V_{\phi L}$	FDN106	−28	−26	−24 V	
	$V_{\phi L}$	FDN116	−28	−12	−9 V	
Data input logic levels						
HIGH	V_{IH}		−1.5	0	+0.3 V	
LOW	V_{IL}		−28	−12	−9 V	
Data lead time	$t_{\ell I}$	FDN106	10	–	– ns	
	$t_{\ell I}$	FDN116	20	–	– ns	
Data hold time	t_{hI}	FDN116	75	–	– ns	

Note 1

The fall time specified for the FDN116 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers the clock pulse fall time may be longer.

Note 2

For FDN106 above f_ϕ = 1.54 MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS

Test conditions: V_{P_1} = −24 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load of 20 kΩ in parallel with 50 pF to P_0

	Symbol	Type number	min.	typ.	max.	Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}		−0.5	–	0 V	
LOW	V_{QL}		−14	–	−10 V	
Data input capacitance	C_I		–	2	3.5 pF	bias: V_I = 0 V; f = 1 MHz
Clock input capacitance	$C_{\phi 1}$, $C_{\phi 2}$	FDN106	–	38	50 pF	bias: V_ϕ = 0 V; f = 1 MHz
	C_ϕ	FDN116	–	6	8 pF	bias: V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}$, $C_{\phi 2}$	FDN106	–	28	37 pF	bias: V_ϕ = −26 V; f = 1 MHz
Leakage currents:						
Data input currents	$-I_{IL}$		–	–	1 μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$		–	–	100 μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}		–	220	500 Ω	
LOW	R_{QL}		–	220	500 Ω	V_{P_2} = V_{P_3} = −5 V
Drive capability (see note 1)	V_{QL}		–	−10	−8 V	R_L = 4 kΩ reference to P_0
	V_{QL}		–	−4.7	−4.4 V	V_{P_2} = V_{P_3} = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2)	$-I_{P_2}$, $-I_{P_3}$		–	3.0	3.5 mA	V_{P_2} = V_{P_3} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN106	–	2.0	4.0 mA	V_{P_1} = −26 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN116	–	5.0	7.0 mA	
Output transition times:						
fall time	t_{THL}		–	100	– ns	
rise time	t_{TLH}		–	100	– ns	
Delay times: fall time	t_{DHL}	FDN106	–	70	– ns	
	t_{DHL}	FDN116	–	300	– ns	
rise time	t_{DLH}	FDN106	–	70	– ns	
	t_{DLH}	FDN116	–	300	– ns	
D.C. noise margin	M_L, M_H		1	–	– V	

CHARACTERISTICS (continued)

Note 1 (see page 4)

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

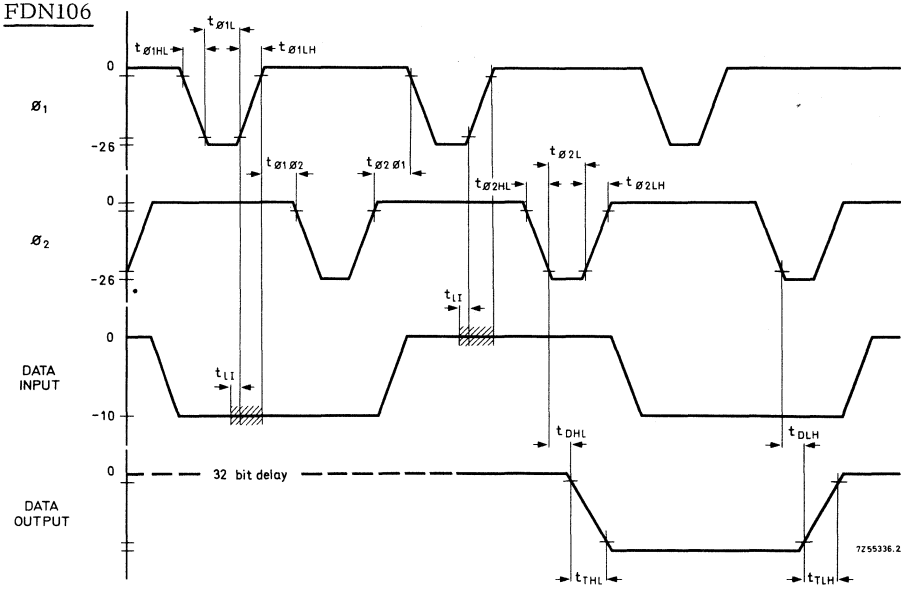
Note 2 (see page 4)

The output buffer power supply currents (I_{P_2}, I_{P_3}) are almost entirely dependent on the external load.

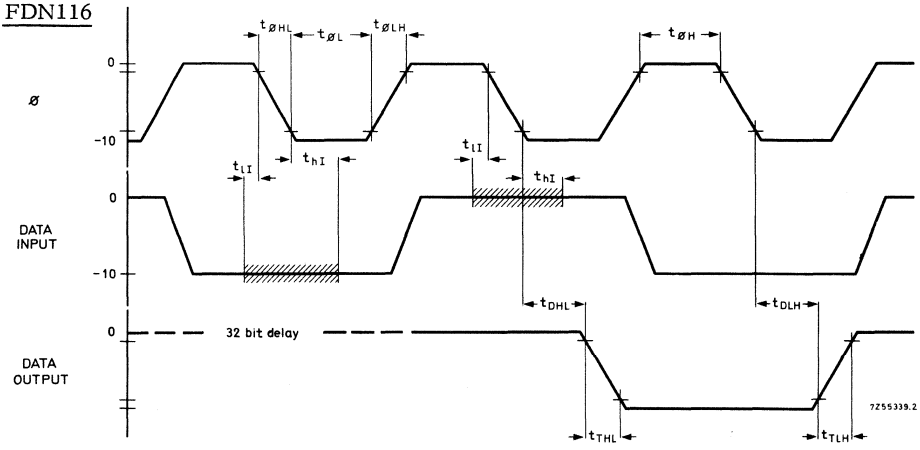
CHARACTERISTICS (continued)

TIMING DIAGRAMS

FDN106



FDN116



Notes

1. The indicated points on the vertical axes are specified in the glossary of terms.
2. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

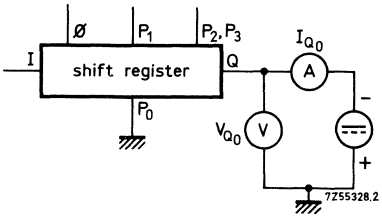
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: FDN106; $V_{\phi L} \leq -24$ V
   FDN116; $V_{\phi L} \leq -9$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$ (FDN106)
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Clock pulse space: $t_{\phi H}$ (FDN116)
   The minimum time between the end of a clock pulse (ϕ) and the start of the next, defined at −2 V.
6. Data lead time: $t_{\ell I}$
   FDN106: The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
   FDN116: The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Data hold time: t_{hI} (FDN116)
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered into the register.
8. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
9. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
10. Fall delay time: t_{DHL}
    FDN106: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
    FDN116: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
11. Rise delay time: t_{DLH}
    FDN106: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.
    FDN116: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

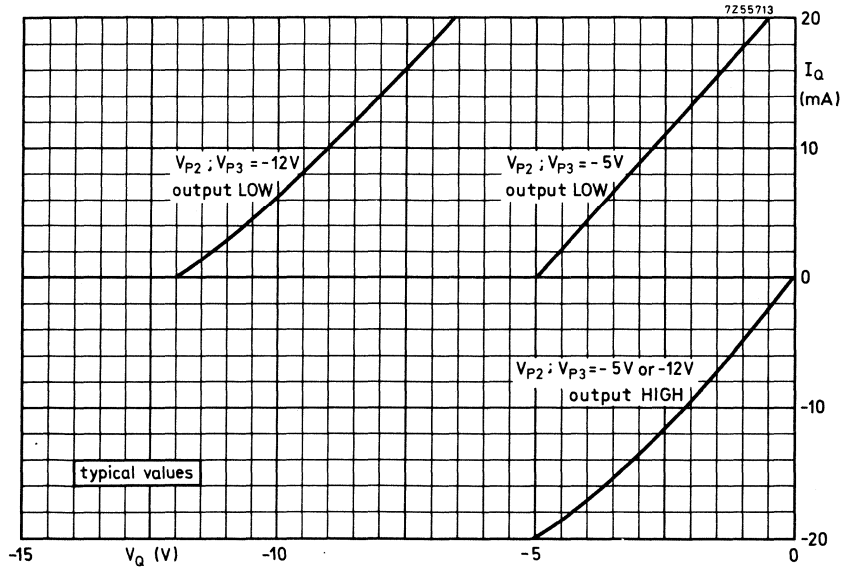
OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN106 and FDN116. They show V_Q versus I_Q for the bias V_{P_2} and V_{P_3} at −5 V and −12 V, for both HIGH and LOW output.

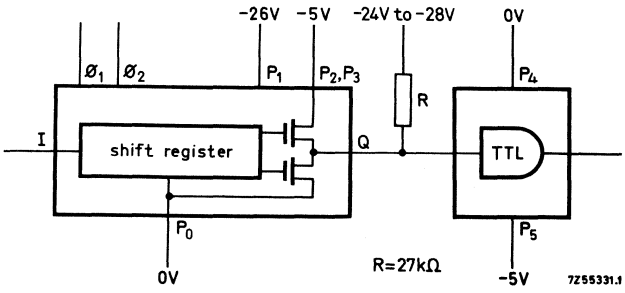
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.

The circuit shown may be used to obtain output curves for other values of V_{P_2} and V_{P_3}.

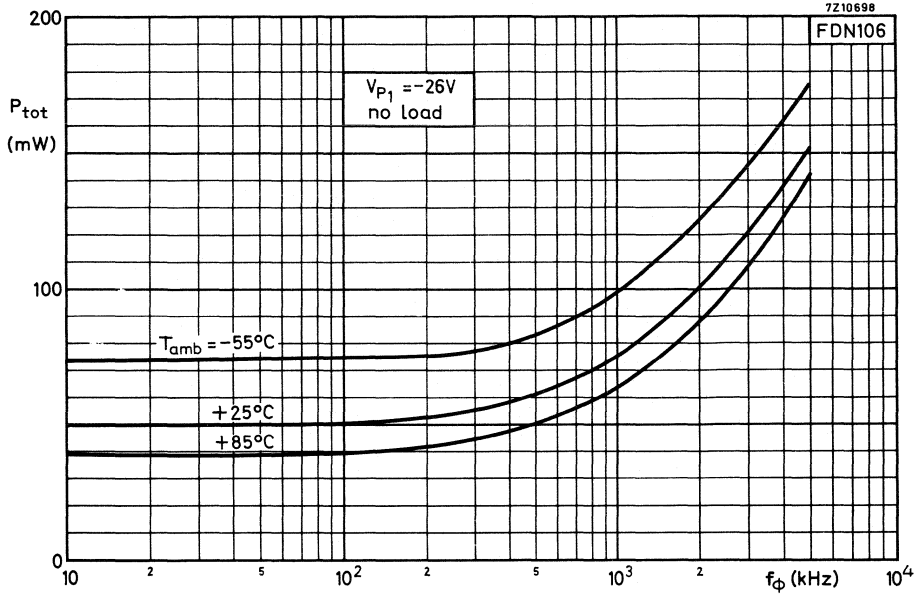


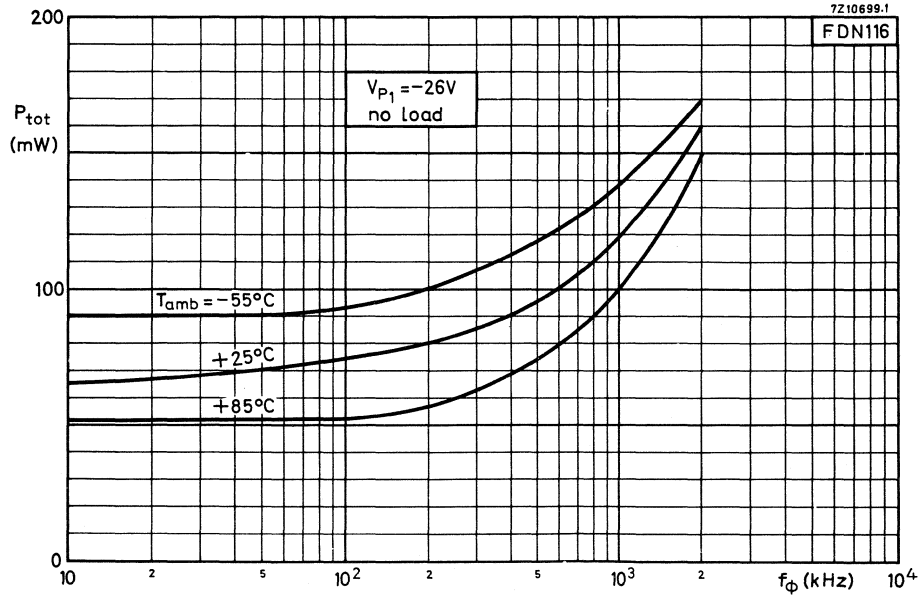


2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.

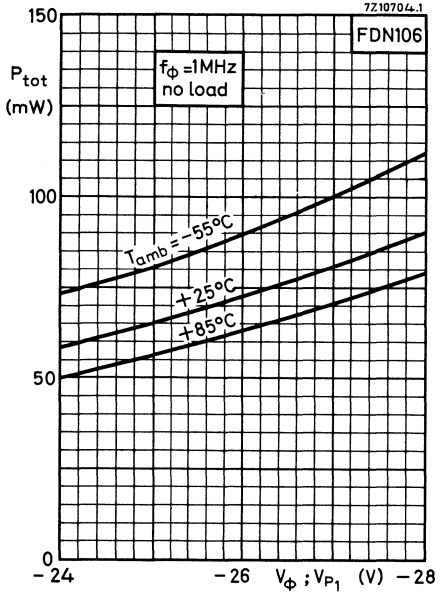


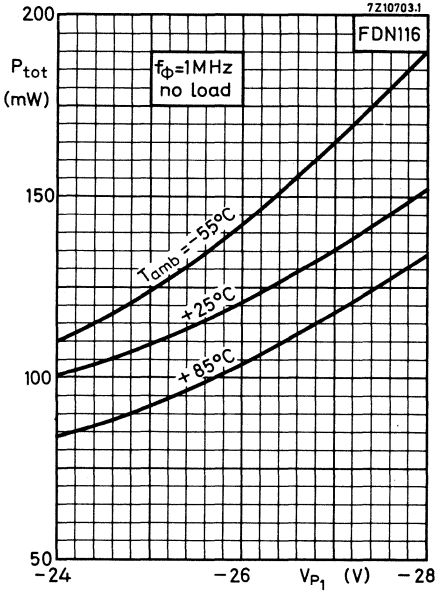
TYPICAL PERFORMANCE

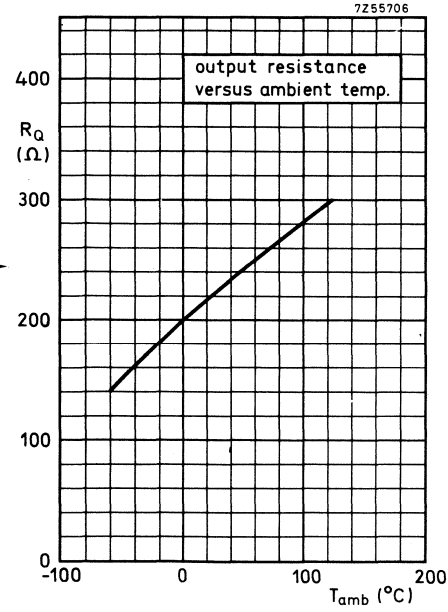


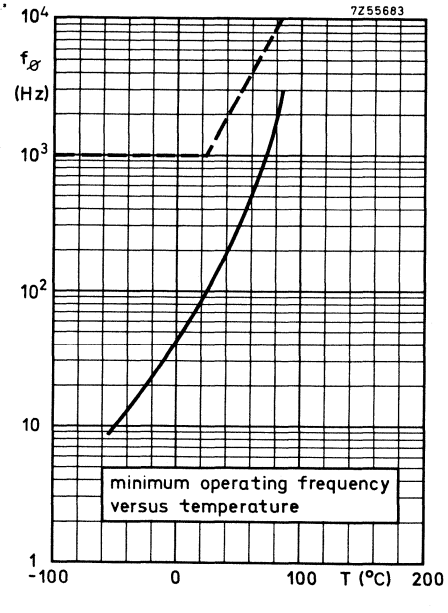


TYPICAL PERFORMANCE (continued)



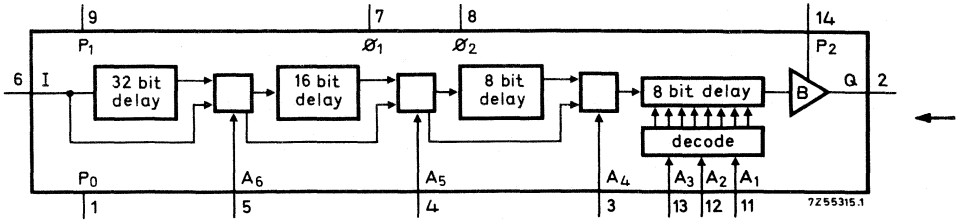


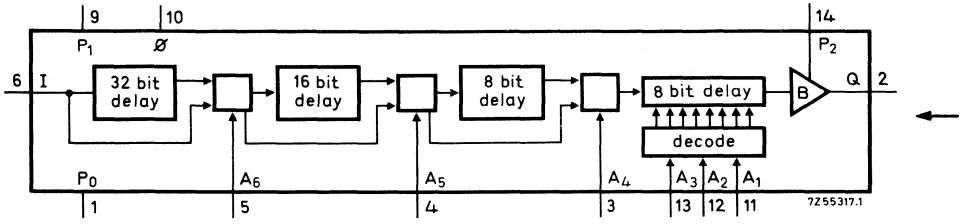


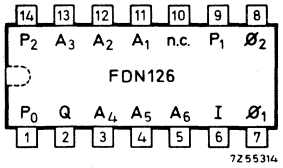


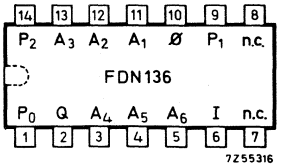
The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

VARIABLE LENGTH 1 TO 64-BIT DYNAMIC SHIFT REGISTERS









P_0 and metal package bottom are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P_1}	−24 to −28		V
D.C. noise margin	M_L; M_H	>	1	V
Clock rate: FDN126	f_ϕ	0.01 to	3	MHz
FDN136	f_ϕ	0.01 to	1	MHz
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE : 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN126 and FDN136 are unique in that the bit length of both registers can be set from 1 to 64 bits by appropriate choice of the logic state of 6 control inputs. The same input and output leads are used, the control inputs determine the number of register stages connected between them.

The FDN126 is essentially for high speed operation and needs a 2 phase external clock.

The FDN136 needs only a low level single phase external clock; it is suitable for applications that do not demand speeds in excess of 1 MHz.

Both circuits use a bi-directional low impedance output buffer which, when appropriately biased, is capable of driving MOS or DTL and TTL loads direct.

With the FDN126; FDN136, the FDN106; FDN116 (quadruple 32-bit dynamic shift registers) and FDN146; FDN156 (256 bit dynamic shift registers) shift registers of any length can be built from off-the-shelf parts.

REGISTER LENGTH CONTROL

The length of the register is controlled by applying binary signals to lines A_1 to A_6. The actual length is one more than the binary sum (see table). The length control bits are gated in at ϕ_1. The length of the register is set up approximately 2 μs +2 clock cycles after application of the control signals. (one clock cycle is one ϕ_1 pulse + one ϕ_2 pulse for the FDN126 and one ϕ pulse for the FDN136)

Table (examples)

weight: 32	16	8	4	2	1	
A_6	A_5	A_4	A_3	A_2	A_1	register length
H	H	H	H	H	H	1-bit
H	H	H	H	H	L	2-bits
H	H	H	L	H	L	6-bits
L	H	H	H	H	H	33-bits
L	L	L	L	L	L	64-bits

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs, control inputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P_2}$	max.	20	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	156	°C/W

DRIVE REQUIREMENTS

	Symbol	Type number	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	FDN126	0.01	–	3 MHz	
	f_ϕ	FDN136	0.01	–	1 MHz	
Clock pulse width	$t_{\phi 1L}$	FDN126	0.1	–	1.0 μs	see timing diagram for parameter def.
	$t_{\phi 2L}$	FDN126	0.125	–	1.0 μs	
	$t_{\phi L}$	FDN136	0.50	–	50 μs	
Clock pulse fall time	$t_{\phi HL}$		–	–	0.10 μs	see note 1, 2
Clock pulse rise time	$t_{\phi LH}$		–	–	0.10 μs	see note 2
Clock delay time	$t_{\phi 1\phi 2}$	FDN126	0	–	49 μs	
Clock delay time	$t_{\phi 2\phi 1}$	FDN126	0	–	49 μs	
Clock pulse space	$t_{\phi H}$	FDN136	0.50	–	50 μs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$		−2	0	+0.3 V	
LOW	$V_{\phi L}$	FDN126	−28	−26	−24 V	
	$V_{\phi L}$	FDN136	−28	−12	−9 V	
Data and control input logic level HIGH	V_{IH};V_{AH}		−1.5	0	+0.3 V	
LOW	V_{IL};V_{AL}		−28	−12	−9 V	
Data lead time	$t_{\ell I}$	FDN126	20	–	– ns	
	$t_{\ell I}$	FDN136	75	–	– ns	
Data hold time	t_{hI}	FDN136	75	–	– ns	

Note

The clock pulse fall time specified for the FDN136 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers, the clock pulse rise and fall times may be longer.

Note 2

For FDN126 above f_ϕ = 1.6 MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS

Test conditions: V_{P_1} = −24 V to −28 V; V_{P_2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load of 20 kΩ in parallel with 50 pF to P_0

	Symbol	Type number	min.	typ.	max.	Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}		−0.5	–	0 V	
LOW	V_{QL}		−14	–	−10 V	
Data input capacitance	C_I		–	2	3.5 pF	bias: V_I = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$, $C_{\phi 2}$	FDN126	–	22	30 pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
	C_ϕ	FDN136	–	6	8 pF	
	$C_{\phi 1}$, $C_{\phi 2}$	FDN126	–	14	20 pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:						
Data input current	$-I_{IL}$		–	–	1 μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	FDN126	–	–	100 μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
	$-I_{\phi L}$	FDN136	–	–	1 μA	V_ϕ = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance:						
HIGH	R_{QH}		–	220	500 Ω	
LOW	R_{QL}		–	220	500 Ω	V_{P_2} = −5 V
Drive capability (see note 1)	V_{QL}		–	−10	−8 V	R_L = 4 kΩ reference to P_0
	V_{QL}		–	−4.7	−4.4 V	V_{P_2} = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2)	$-I_{P_2}$		–	0.8	1.0 mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN126	–	2.5	5.0 mA	V_{P_1} = −26 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN136	–	3.0	6.0 mA	
Output transition times:						
fall time	t_{THL}		–	80	– ns	
rise time	t_{TLH}		–	80	– ns	
Delay times: fall time	t_{DHL}	FDN126	–	70	– ns	
	t_{DHL}	FDN136	–	300	– ns	
rise time	t_{DLH}	FDN126	–	70	– ns	
	t_{DLH}	FDN136	–	300	– ns	
D.C. noise margin	M_L, M_H		1	–	– V	

CHARACTERISTICS (continued)

Note 1 (see page 4)

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

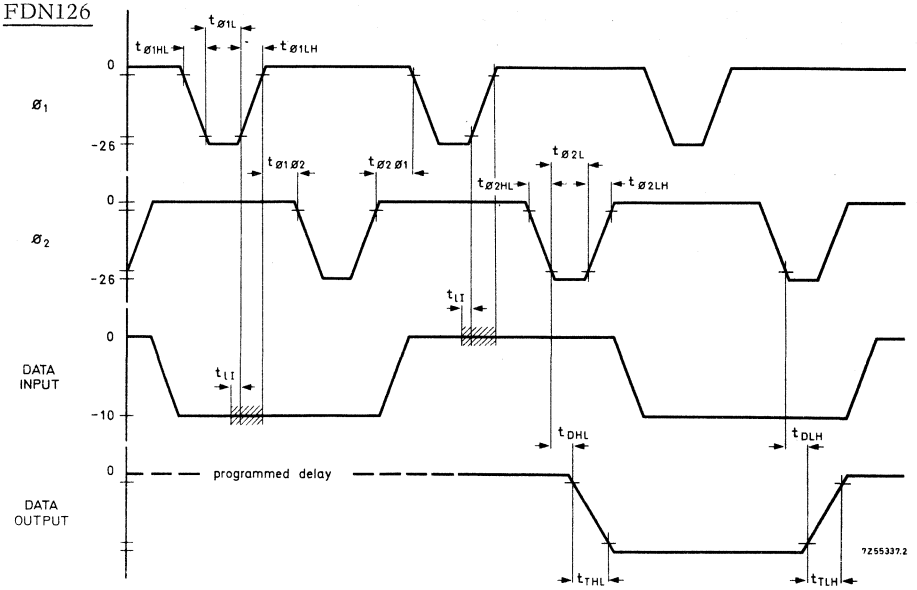
Note 2 (see page 4)

The output buffer power supply current I_{P2} is almost entirely dependent on the external load.

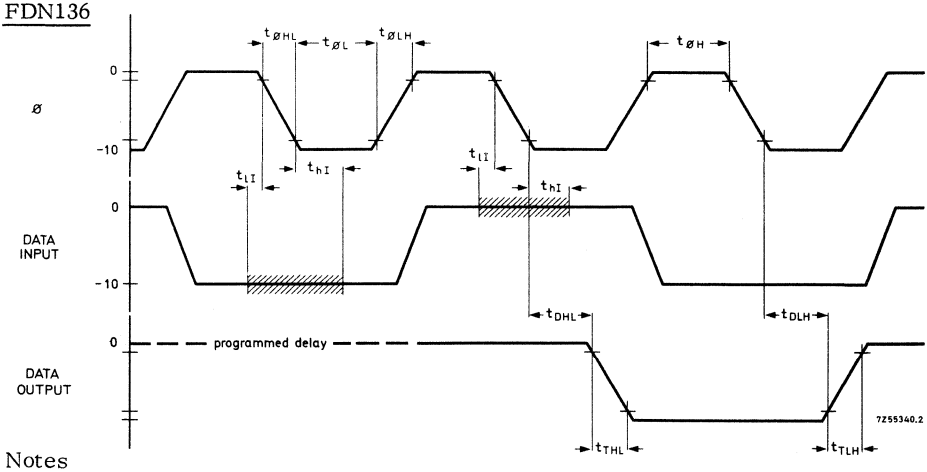
CHARACTERISTICS (continued)

TIMING DIAGRAMS

FDN126



FDN136



Notes

1. The indicated points on the vertical axes are specified in the glossary of terms.
2. During a continuous series of LOW signals the data output may return momentarily to zero once every clock cycle, i.e. when the register output normally changes signal. The data output should be not sampled during this period.
3. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

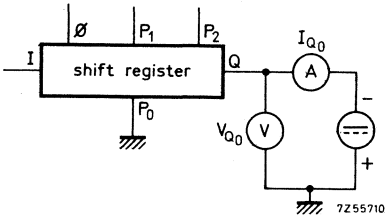
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: FDN126; $V_{\phi L} \leq -24$ V
   FDN136; $V_{\phi L} \leq -9$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$ (FDN126)
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Clock pulse space: $t_{\phi H}$ (FDN136)
   The minimum time between the end of a clock pulse (ϕ) and the start of the next, defined at −2 V.
6. Data lead time: $t_{\ell I}$
   FDN126: The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
   FDN136: The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Data hold time: t_{hI} (FDN136)
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered into the register.
8. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
9. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
10. Fall delay time: t_{DHL}
    FDN126: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
    FDN136: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
11. Rise delay time: t_{DLH}
    FDN126: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.
    FDN136: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

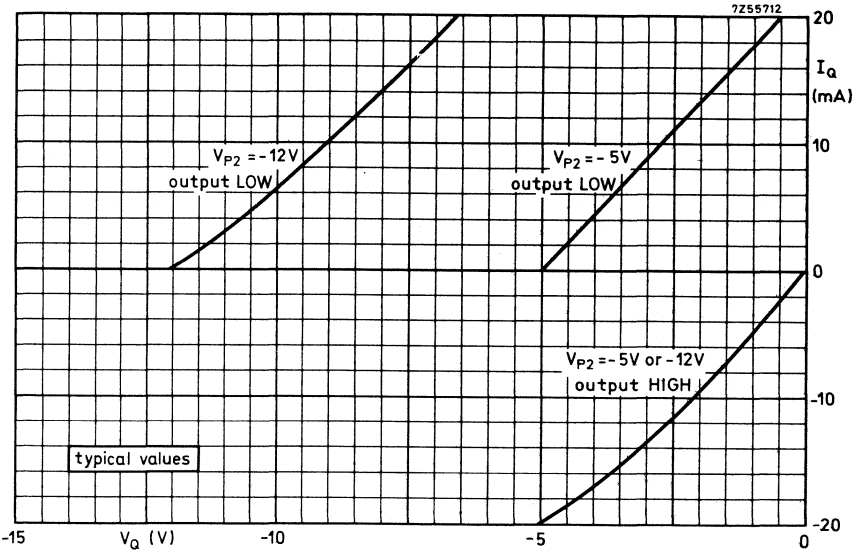
OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN126 and FDN136. They show V_Q versus I_Q for the bias V_{P2} at − 5 V and − 12 V, for both HIGH and LOW output.

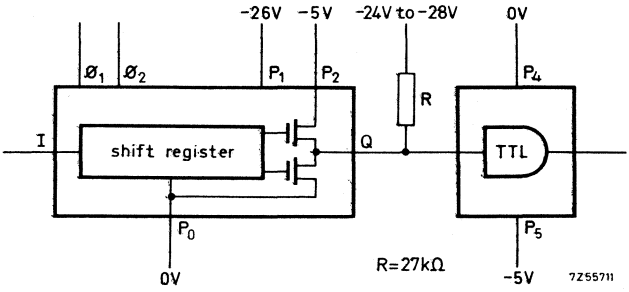
Note: When operating with high output current levels, the maximum power rating must not be exceeded.

The circuit shown may be used to obtain output curves for other values of V_{P2}.

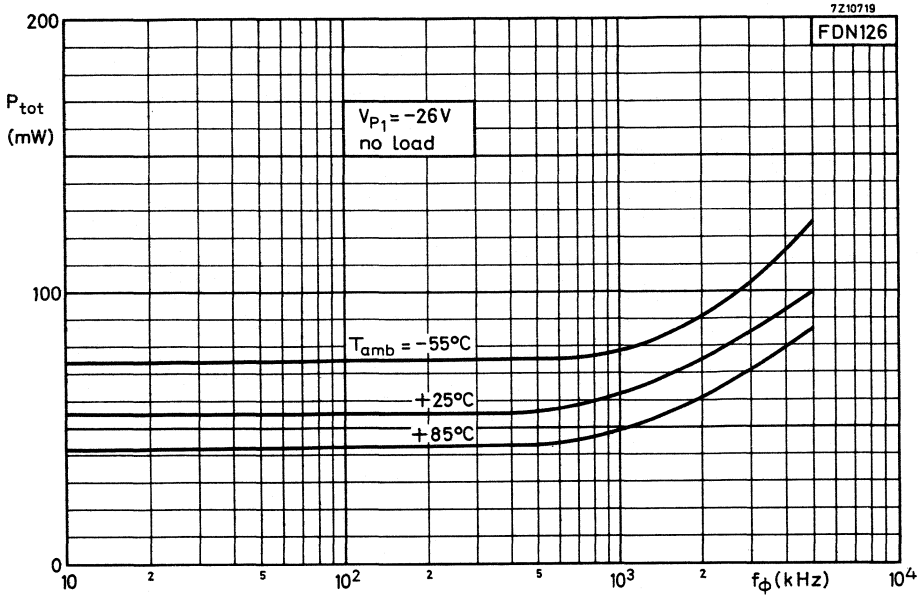


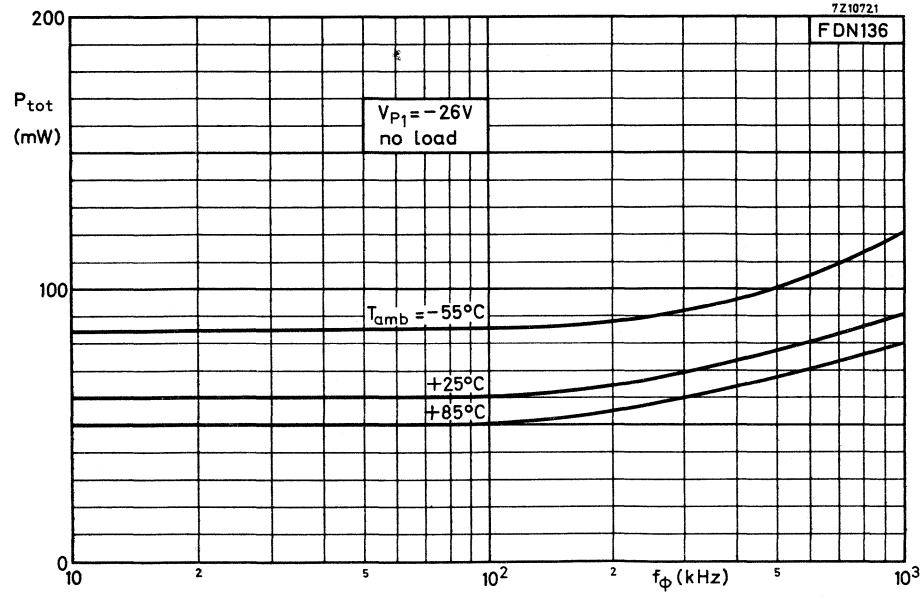


2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.

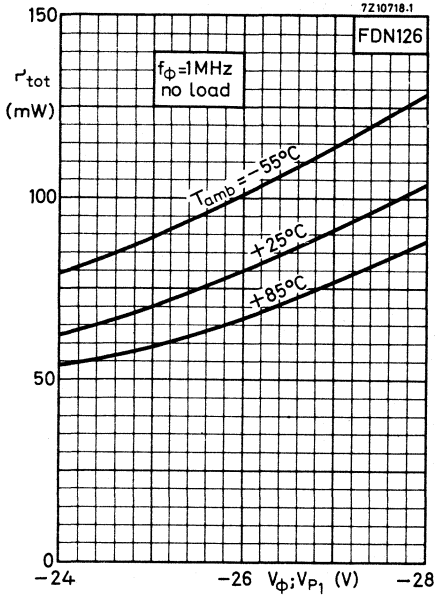


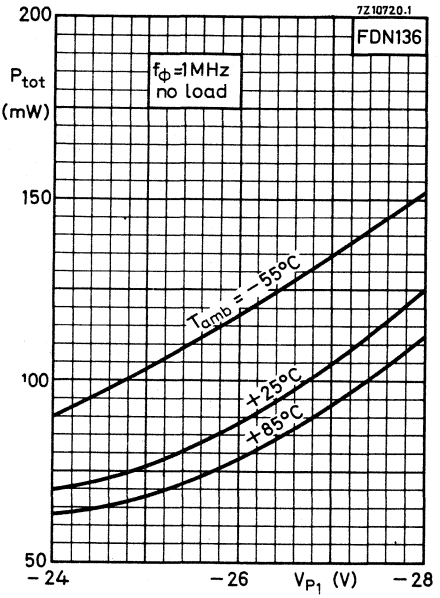
TYPICAL PERFORMANCE

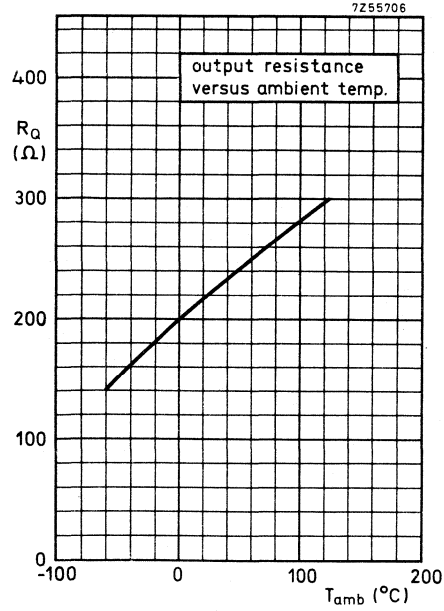


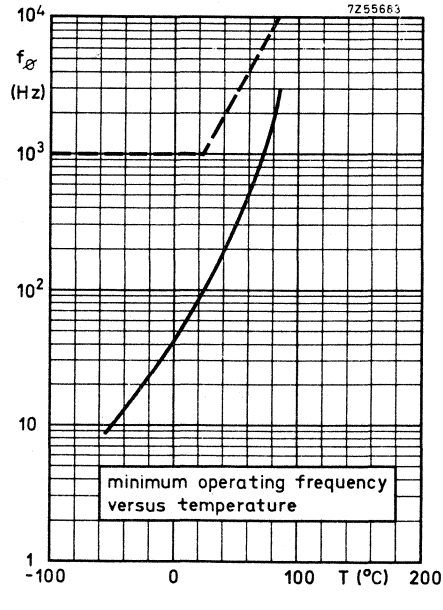


TYPICAL PERFORMANCE (continued)



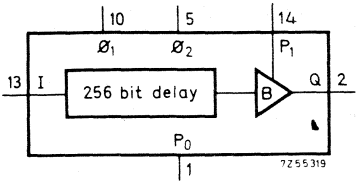


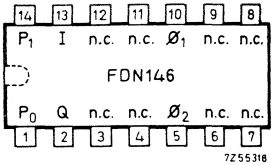


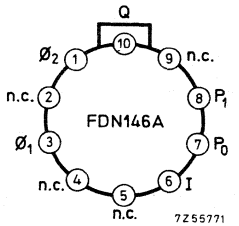


The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

256-BIT DYNAMIC SHIFT REGISTER







Pin numbers refer to FDN146 only

FDN146 : P_0 connected to metal bottom
FDN146A: P_0 connected to metal case

QUICK REFERENCE DATA			
D.C. noise margin	M_L	> 1	V
Clock rate	f_ϕ	0.01 to 3	MHz
Power consumption per bit at 10 kHz	P_{av}	< 0.002	mW
1 MHz	P_{av}	< 0.2	mW
3 MHz	P_{av}	< 0.6	mW
Power dissipation	P_{tot}	max. 300	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

GENERAL DESCRIPTION

The FDN146(A) contains one continuous 256-bit shift register with one serial input and one serial output. It dissipates very little power and uses a two-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads. The buffer supply terminal P_1 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse. With the FDN146(A), the FDN106 (a quadruple 32-bit shift register) and FDN126 (a variable length 1 to 64 bit shift register) shift registers of any length can be built from off-the-shelf parts.

PACKAGE OUTLINE: FDN146: 14 lead metal-ceramic dual in-line (See General Section)
FDN146A: TO-100 (See General Section)

→ **RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C				
	FDN146 : P_{tot}	max.	800	mW
	FDN146A: P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65	+156	°C

→ **THERMAL RESISTANCE**

From junction to ambient	FDN146 : $R_{th\ j\text{-}a}$	=	156	°C/W
	FDN146A: $R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.01	–	3 MHz	
Clock pulse width	$t_{\phi 1L}$	0.125	–	1.0 µs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.125	–	1.0 µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 µs	see note 2
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 µs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	49 µs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	49 µs	
Clock pulse voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−27	−26 V	see note 1
Data input logic levels					
HIGH	V_{IH}	−1.5	0	+0.3 V	
LOW	V_{IL}	−28	−12	−9 V	
Data lead time	$t_{\ell I}$	10	–	– ns	

Note 1

The FDN146(A) can be supplied in versions that will operate with −24 V to −28 V clock pulse LOW signal range.

→ Note 2

Above f_ϕ = 1.54 MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 20 kΩ to P_0

	Symbol	min.	typ.	max.	Conditions and references
ELECTRICAL DATA					
Output levels					
HIGH	V_{QH}	−0.5	–	0 V	
LOW	V_{QL}	−14	–	−10 V	
Data input capacitance	C_I	–	2	3.5 pF	bias: V_I = 0 V; $f\phi$ = 1 MHz
Clock input capacitance	$C_{\phi 1}$, $C_{\phi 2}$	–	70	80 pF	bias: $V\phi$ = 0 V; $f\phi$ = 1 MHz
	$C_{\phi 1}$, $C_{\phi 2}$	–	45	55 pF	bias: $V\phi$ = −26 V; $f\phi$ = 1 MHz
Leakage currents:					
Data input current	$-I_{IL}$	–	–	1 μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100 μA	$V\phi$ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance					
HIGH	R_{QH}	–	250	500 Ω	
LOW	R_{QL}	–	120	300 Ω	V_{P_1} = −5 V
Drive capability see note 1	V_{QL}	–	−4.8	−4.6 V	V_{P_1} = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2)	$-I_{P_1}$	–	1.0	1.5 mA	V_{P_1} = −13 V; $f\phi$ = 1 MHz T_{amb} = 25 °C
Output transition times:					
fall time	t_{THL}	–	70	– ns	
rise time	t_{TLH}	–	70	– ns	
Delay times: fall time	t_{DHL}	–	70	– ns	
rise time	t_{DLH}	–	70	– ns	
D.C. noise margin	M_L; M_H	1	–	– V	

Note 1

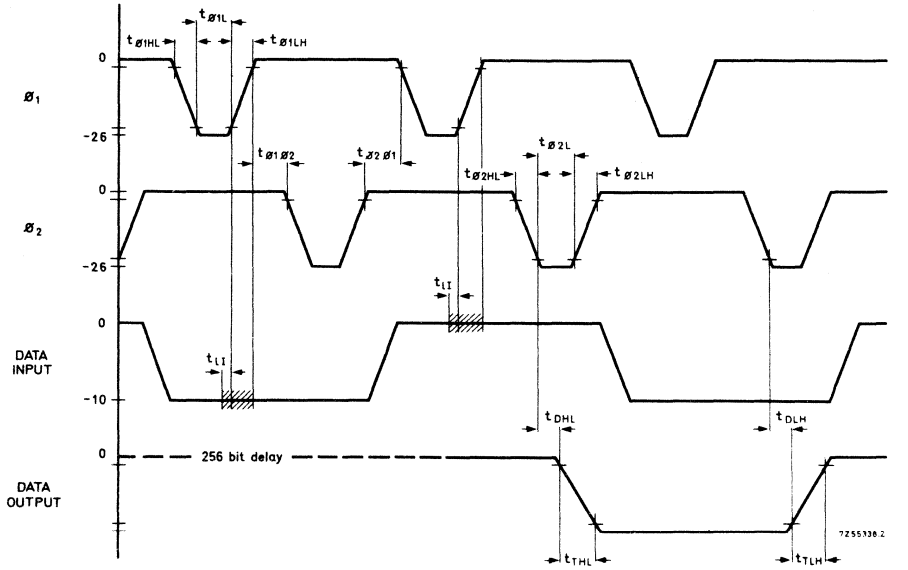
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 6 and 7 for further information on output drive capability.

Note 2

The output buffer power supply current I_{P_1} is almost entirely dependent on the external load. The value shown is for a standard load of 1 MΩ, 50 pF load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.
2. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

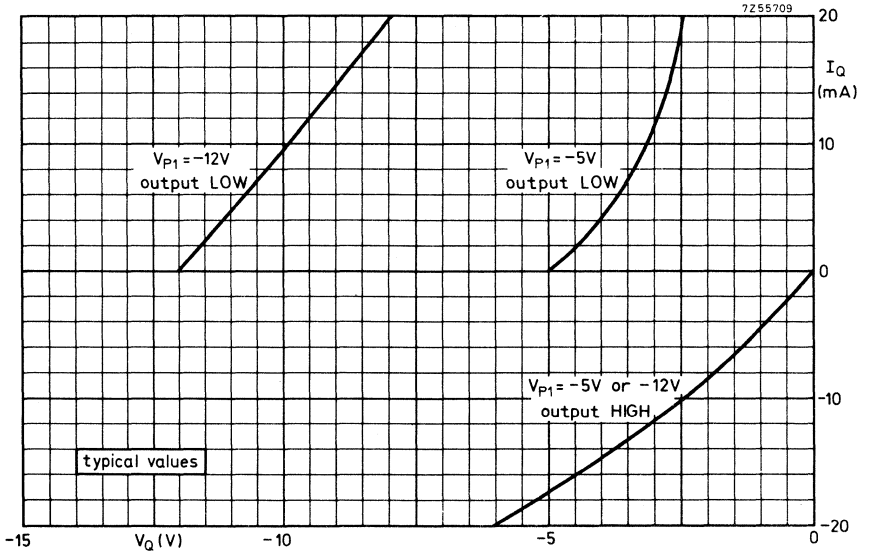
GLOSSARY OF TERMS

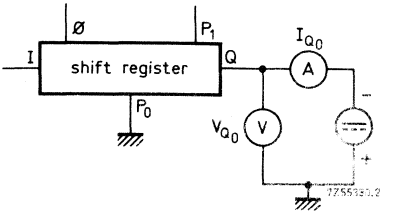
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -26$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
7. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
8. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
9. Rise delay time: t_{DLH}
   The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN146(A). They show V_Q versus I_Q for the bias V_{P1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain output curves for other values of V_{P1}.

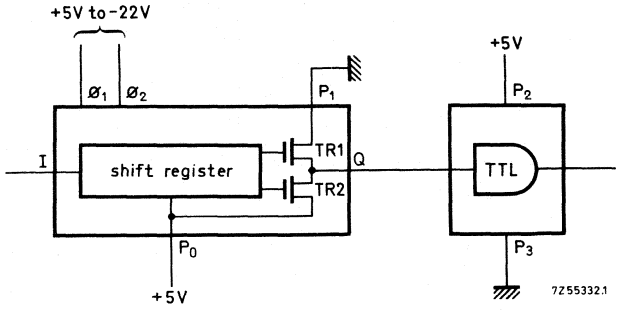
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





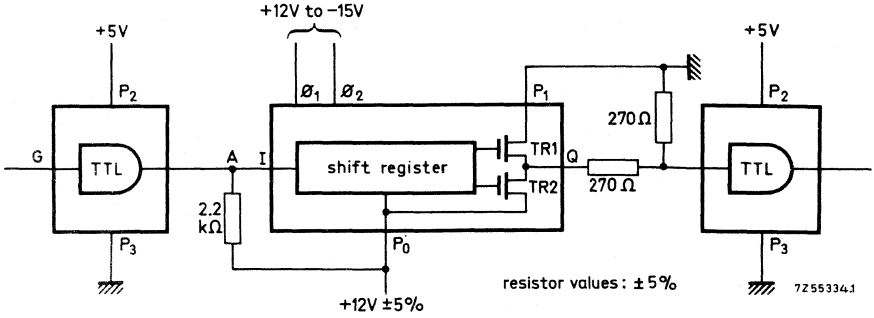
OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P_0}. TR1 and TR2 are the push-pull output driver transistors of the FDN146.



Biasing circuit A

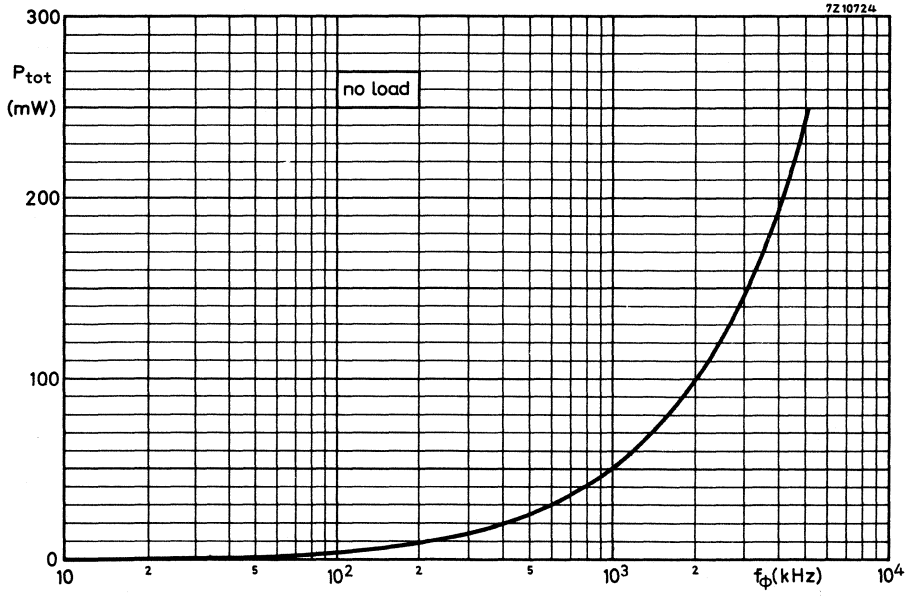
3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both the input and output using only passive interface components.
Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead (point A), most non-R_C type gates of our FC series and most FJ gates satisfy this requirement. Special open collector FJ gates (FJH301, 311, 321) have a minimum ouput breakdown voltage guarantee of 15 V.

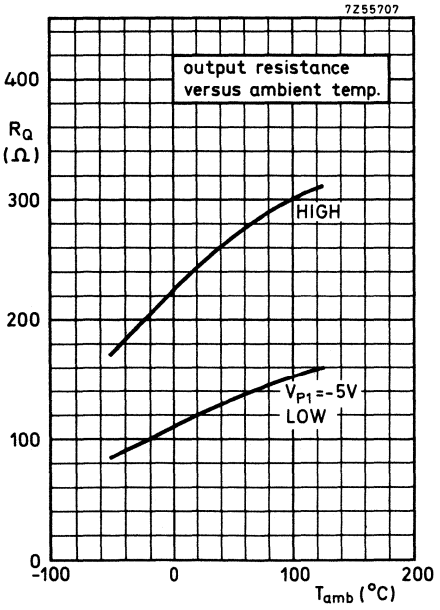


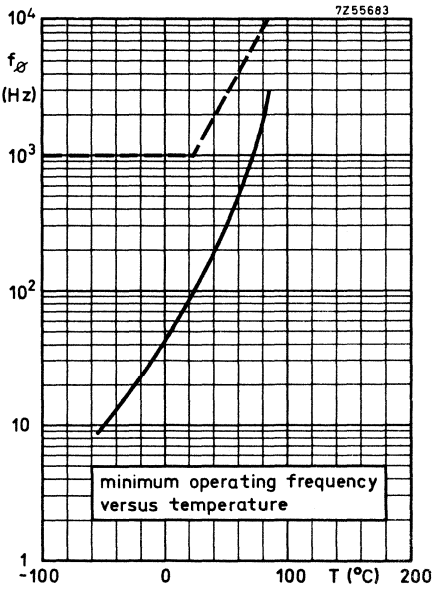
Biasing circuit B

4. To drive MOS loads direct, the bias V_{P_1} should be between −12 and −14 V to P_0.

TYPICAL PERFORMANCE

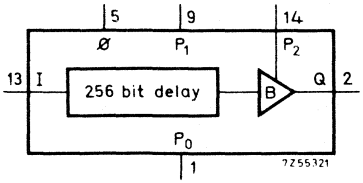


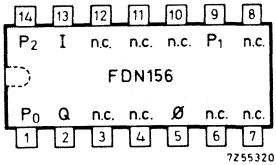


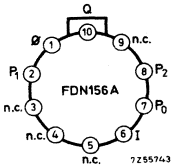


The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

256-BIT DYNAMIC SHIFT REGISTER







Pin numbers refer to FDN156 only

FDN156 : P_0 connected to the metal bottom
FDN156A: P_0 connected to the metal case

QUICK REFERENCE DATA			
Supply voltage	V_{P_1}	−26 to −28	V
D.C. noise margin	M_L	> 1	V
	M_H	> 1.5	V
Clock rate	f_ϕ	0.01 to 1	MHz
Power consumption per bit at f = 10 kHz	P_{av}	< 0.2	mW
f = 1 MHz	P_{av}	< 0.6	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

GENERAL DESCRIPTION

The FDN156A contains one 256-bit shift register with one serial input and one serial output. It dissipates very little power and uses a one-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads.
The buffer supply terminal P_2 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse.
With the FDN156A, the FDN116 (a quadruple 32-bit shift register) and FDN136 (a variable length 1 to 64-bit shift register) shift registers of any length can be built from off-the-shelf parts.

PACKAGE OUTLINE: FDN156: 14 lead metal-ceramic dual in-line (See General Section)
FDN156A: TO-100 (See General Section)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	FDN156 : P_{tot}	max.	800	mW
	FDN156A: P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max.	20	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	FDN156 : $R_{th\ j\text{-}a}$	=	156	°C/W
	FDN156A: $R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.01	–	1 MHz	
Clock pulse width	$t_{\phi L}$	0.5	–	50 µs	See timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 µs	See note 1
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 µs	
Clock pulse space	$t_{\phi H}$	0.5	–	50 µs	
Clock pulse voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−12	−9 V	
Data input logic levels					
HIGH	V_{IH}	−2	0	+0.3 V	
LOW	V_{IL}	−28	−12	−9 V	
Data lead time	$t_{\ell I}$	20	–	– ns	
Data hold time	t_{hI}	75	–	– ns	
Supply voltages	V_{P1}	−28	−26	−24 V	$f\phi \leq$ 750 kHz
	V_{P1}	−28	−27	−26 V	$f\phi \leq$ 750 kHz
	V_{P2}	−28	–	+0.3 V	

Note 1

The fall time specified for the FDN156(A) is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers the clock pulse fall time may be longer.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −26 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.	max.	Conditions and references
ELECTRICAL DATA					
Output levels					
HIGH	V_{QH}	−0.5	−	0 V	
LOW	V_{QL}	−14	−	−10 V	
Data input capacitance	C_I	−	2	3.5 pF	bias: V_I = 0 V; f_ϕ = 1 MHz
Clock input capacitance	C_ϕ	−	6	10 pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
Leakage currents					
Data input currents	$-I_{IL}$	−	−	1 μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	−	−	100 μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance					
HIGH	R_{QH}	−	250	500 Ω	
LOW	R_{QL}	−	250	500 Ω	V_{P_2} = −5 V
Drive capability (see note 1)	V_{QL}	−	−4.8	−4.6 V	V_{P_2} = −5 V; R_L = 4 kΩ to reference P_0
Power supply current drain (see note 2)	$-I_{P_2}$	−	1.0	1.5 mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	−	5.0	8.0 mA	V_{P_1} = −27 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:					
fall time	t_{THL}	−	100	− ns	
rise time	t_{TLH}	−	100	− ns	
Delay times: fall time	t_{DHL}	−	300	− ns	
rise time	t_{DLH}	−	300	− ns	
D.C. noise margin	M_L	1	−	− V	
	M_H	1.5	−	− V	

Note 1

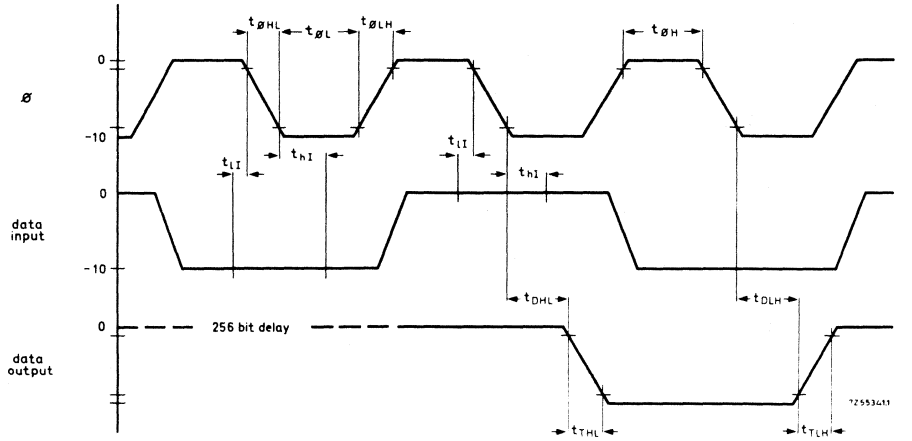
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 5 and 6 for further information on output drive capability.

Note 2

The output buffer power supply current I_{P_2} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

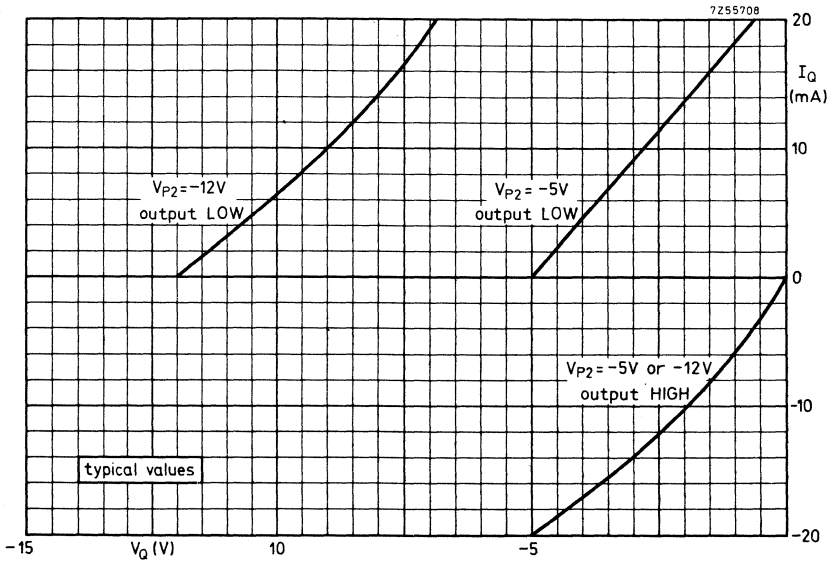
GLOSSERY OF TERMS

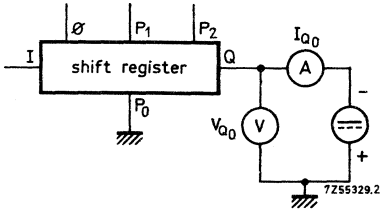
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -9$ V.
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock pulse space: $t_{\phi H}$
   The least allowable time between the end of a clock pulse (ϕ) and the start of the next.
5. Data lead time: $t_{\ell I}$
   The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Data hold time: t_{hI}
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable in order to ensure that the data will be entered in the register.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
10. Rise delay time: t_{DLH}
    The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN156. They show V_Q versus I_Q for the bias V_{P_1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain output curves for other values of V_{P_2}.

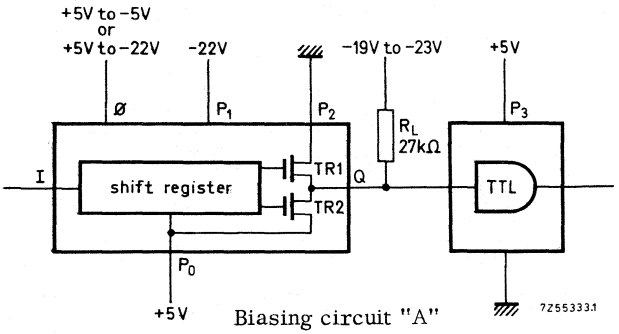
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





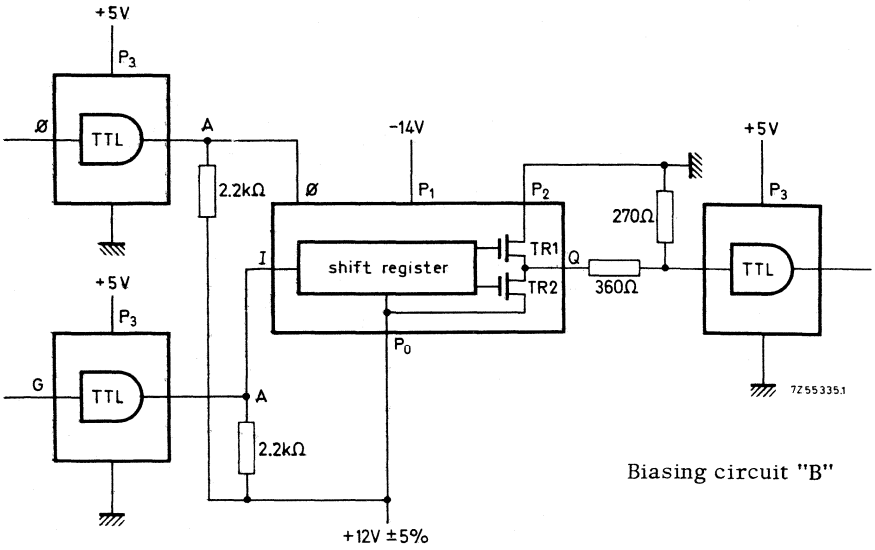
OUTPUT BUFFER DESCRIPTION

2. Biasing circuit "A" may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0}. TR1 and TR2 are the push-pull output driver transistor of the FDN156.



Biasing circuit "A"

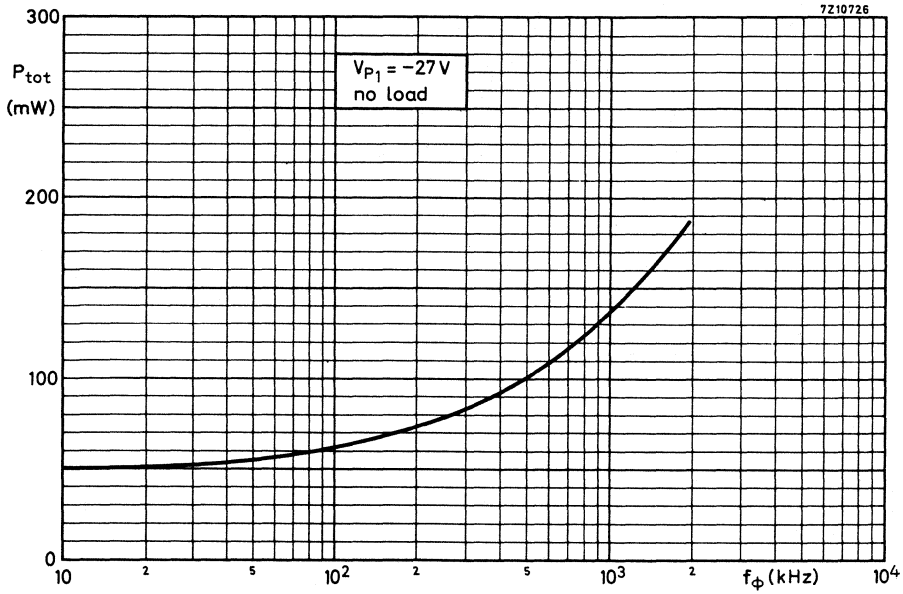
3. Biasing circuit "B" allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A), most non-R_C type gates of our FC series and most FJ gates satisfy this requirement. Special open collector FJ gates (FJH301; 311; 321) have a minimum output breakdown voltage guarantee of 15 V.

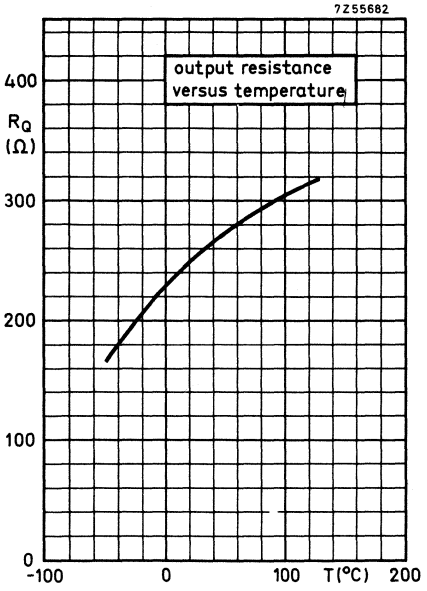


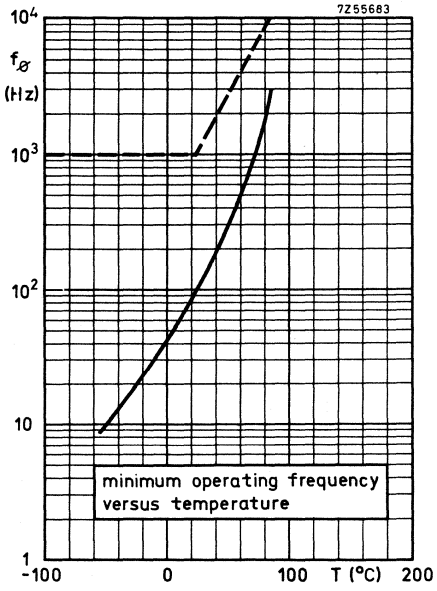
Biasing circuit "B"

4. To drive MOS loads direct, the bias V_{P1} should be between −12 and −14 V to P_0.

TYPICAL PERFORMANCE

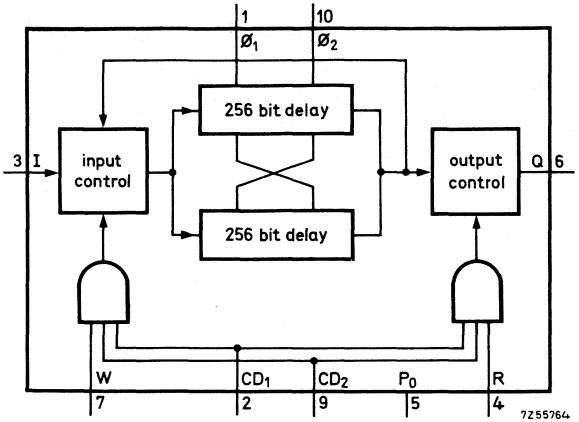


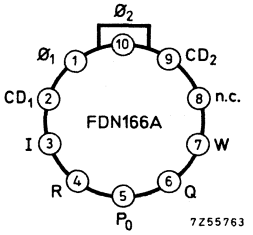




The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

512-BIT RECIRCULATING DYNAMIC SERIAL MEMORY





P_0 connected to the metal case

QUICK REFERENCE DATA			
Clock rate	f_ϕ	0.005 to 5	MHz
Data rate	f_D	0.01 to 5	MHz
Power consumption per bit			
at 1 MHz data rate	P_{av}	0.07	mW
at 5 MHz data rate	P_{av}	0.35	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE : TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN166A consists of two 256-bit 2-phase dynamic shift registers, with internal multiplexing and recirculation circuitry. [1])
Data is written into and read from the device at both ϕ_1 and ϕ_2, so that the data rate is twice the clock rate. The chip disable (CD) inputs allow selection of one-out-of--many circuits in larger memories. Both CD inputs have to be in the HIGH state to activate the device. Data will be written in when W, CD_1, and CD_2 are in the HIGH state; at all other times the device is in the recirculation mode. The output is active only when R, CD_1 and CD_2 are in the HIGH state; so that the outputs of more devices can be wired-OR.
With the FDN166A large serial memories with a drum-like organisation can be made.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation	P_{tot}	max.	625	mW
Junction temperature up to T_{amb} = 25 °C	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	200	°C/W

Note
All terminals are protected against over-voltage due to static charges.

[1]) External behaviour: 512-bit shift register.

DRIVE REQUIREMENTS at T_{amb} = −55 to +85 °C; P_0 is grounded

	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.05	–	1.5 MHz	$V_{\phi L}$ = −23 V
		0.05	–	2.5 MHz	$V_{\phi L}$ = −26 V
Clock pulse width	$t_{\phi L}$	0.28	–	10 µs	$V_{\phi L}$ = −23 V
		0.16	–	10 µs	$V_{\phi L}$ = −26 V
Clock pulse rise time	$t_{\phi LH}$	–	–	100 ns	
Clock pulse fall time	$t_{\phi HL}$	–	–	100 ns	
Clock delay	$t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$	0	–	100 µs	
Clock pulse voltage levels					
HIGH	$V_{\phi H}$	−2	–	+0.3 V	
LOW	$V_{\phi L}$	−28	–	−23 V	
Data input logic levels					
HIGH	V_{IH}, V_{CDH}, V_{RH}, V_{WH}	−1	–	+0.3 V	
LOW	V_{IL}, V_{CDL}, V_{RL}, V_{WL}	−28	–	−9 V	
Data lead time for I, W, R and CD inputs	t_ℓ	50	–	– ns	

CHARACTERISTICS at T_{amb} = −55 to +85 °C; P_0 grounded

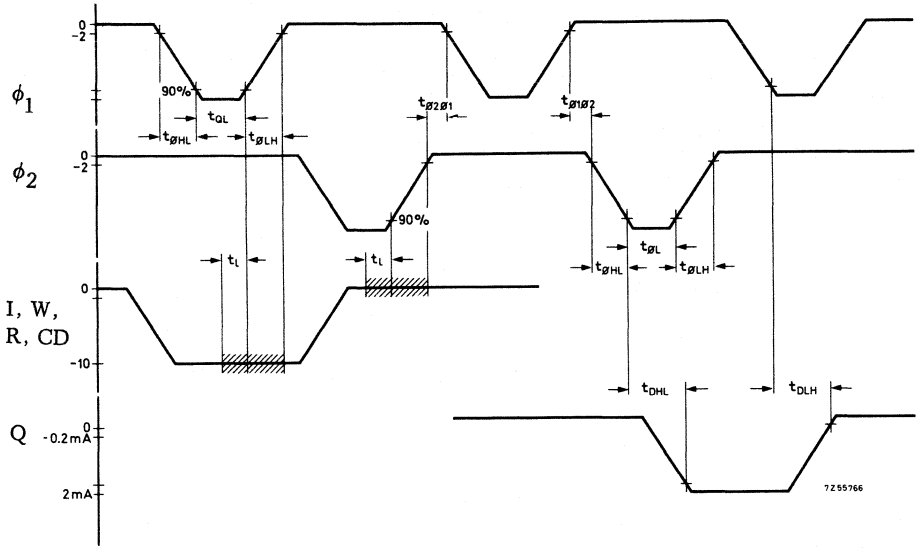
	Symbol	min.	typ.	max.	Conditions and references
Data rate	f_D	0.01	–	3 MHz	$V_{\phi L}$ = −23 V
	f_D	0.01	–	5 MHz	$V_{\phi L}$ = −26 V
Output current					
HIGH	$-I_{QH}$	2	–	– mA	V_Q = −5 V; see note
LOW	$-I_{QL}$	–	–	10 µA	V_Q = −15 V
Capacitances					
I, R, W and CD inputs	C_I	–	2.3	3.5 pF	V_I = 0 V; f = 1 MHz
Clock input capacitance	C_ϕ	–	95	110 pF	V_ϕ = 0 V; f = 1 MHz
Output capacitance	C_Q	–	2.0	2.5 pF	V_Q = 0 V; f = 1 MHz
Leakage currents					
I, R, W and CD inputs	$-I_I$	–	–	1 µA	V_I = −15 V; T_{amb} = 25 °C all other terminals at V_{P0}
Clock inputs	$-I_\phi$	–	–	100 µA	V_ϕ = −28 V; T_{amb} = 25 °C all other terminals at V_{P0}
Output resistance					
HIGH	R_{QH}	–	–	1 kΩ	V_Q = −5 V; See note
Delay times					
Clock input to data output	t_{DHL}, t_{DLH}	–	–	110 ns	

Note

The specified output current is measured immediately after the delay time t_{DLH}. In a steady HIGH state the output resistance decreases to less then 1 kΩ.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

Data inputs (I, W, R, CD_1 and CD_2) must remain valid for the shaded interval to ensure proper entry.
When CD_1, CD_2 and R are HIGH during this time, the output circuit will be active during the succeeding clock pulse.

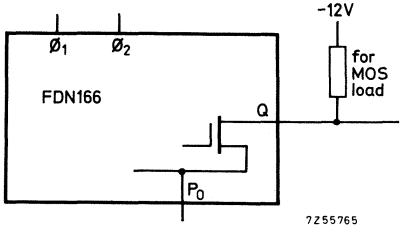
CHARACTERISTICS

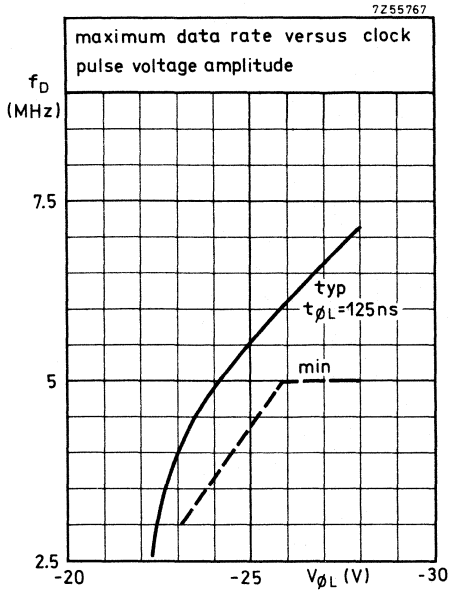
GLOSSARY OF TERMS

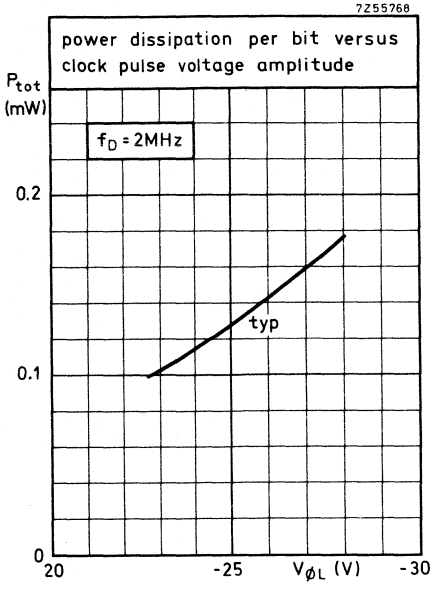
1. Clock pulse width: $t_{\phi}L$
   The time for which the clock pulse is LOW.
2. Clock pulse fall time: $t_{\phi}HL$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi}LH$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
   The time for which the clock pulses are simultaneously HIGH.
5. Data lead time: t_{ℓ}
   The time before the indicated point on the clock pulse for which I, R, W, CD_1 and CD_2 must be present at the inputs to ensure correct entry into the memory.
6. Delay time: t_D
   The delay between the clock pulse reaching LOW and the output beginning to change from LOW to HIGH.

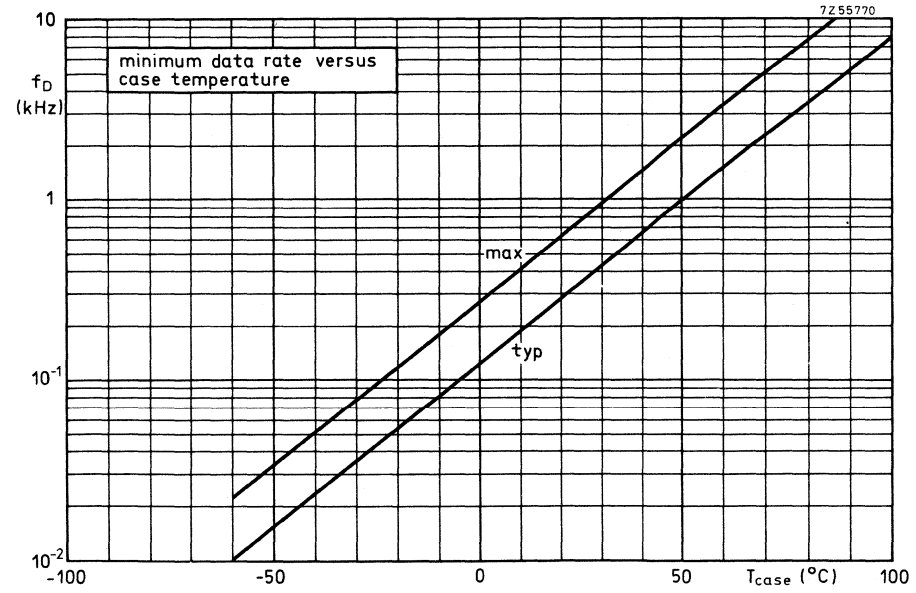
OUTPUT BUFFER DESCRIPTION

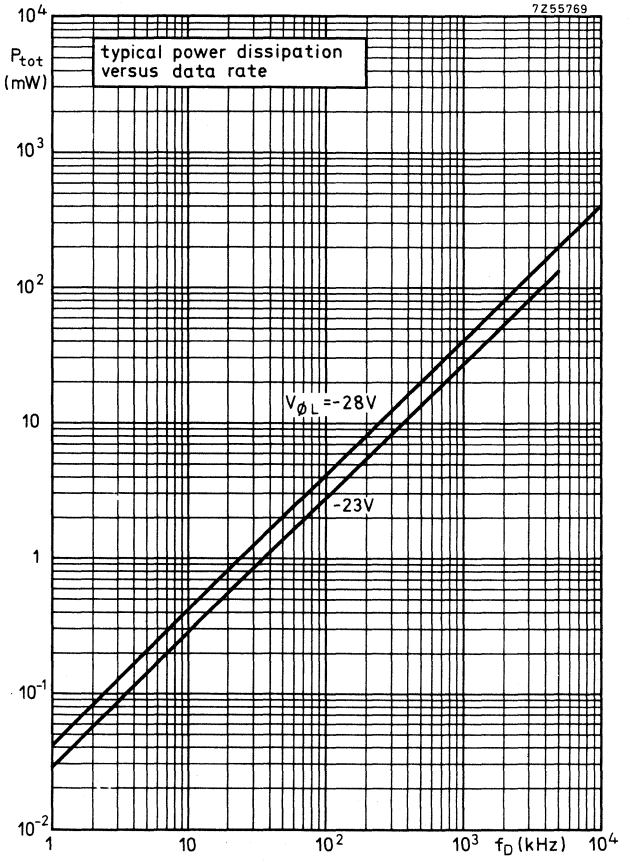
The output buffer of the FDN166A consists of an open drain MOS transistor. The source is connected to P_0, the drain to the output terminal Q. The use of this type of output allows wired-OR-ing of the outputs in expanded memories. The buffer can simply be interfaced with TTL or with other MOS circuits. In the latter case only one resistor is required; which value depends on the load capacitance and the speed desired.




7Z55767
maximum data rate versus clock pulse voltage amplitude
f_D (MHz)
7.5
5
2.5
typ
$t_{\phi L}$=125ns
min
-20
-25
$V_{\phi L}$ (V)
-30

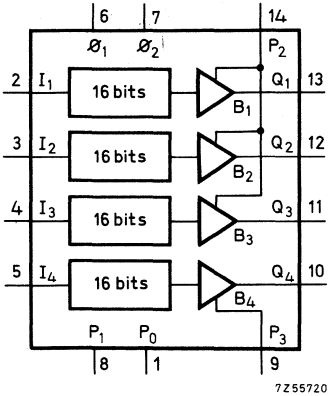

7Z55768
power dissipation per bit versus clock pulse voltage amplitude
P_{tot} (mW)
f_D = 2MHz
0.2
0.1
0
typ
20
-25
$V_{\phi L}$ (V)
-30

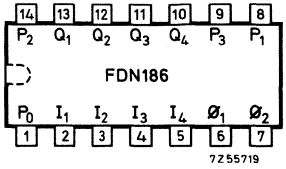

7Z55770
minimum data rate versus case temperature
f_D (kHz)
10
1
10^{-1}
10^{-2}
max
typ
-100
-50
0
50
T_{case} (°C)
100


7Z55769
typical power dissipation
versus data rate
P_{tot} (mW)
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
$V_{\phi L}$=-28V
-23V
1
10
10^2
10^3
f_D (kHz)
10^4

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

QUADRUPLE 16-BIT DYNAMIC SHIFT REGISTER





P0 and metal package bottom are connected.

QUICK REFERENCE DATA			
Supply voltage	V_{P_1}	−24 to −28	V
D.C. noise margin	$M_L; M_H$	> 1	V
Clock rate	f_ϕ	0.01 to 3	MHz
Power consumption per bit at 1 MHz	P_{av}	typ. 1.2	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE : 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN186 package comprises 4 separate 16-bit shift registers that can be used independently or can be externally connected to make registers up to 64-bits long. Clock and power lines are common to all four registers. The output buffers are bi-directional, low impedance NRZ [1]), that by suitable biasing will directly drive MOS, DTL or TTL loads or, because they have separate output voltages (V_{P2}; V_{P3}), a combination of MOS and bipolar. V_{P2} and V_{P3} are output buffer voltages only, and the output signal is independent of the width and amplitude of the clock pulse.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminals P_2 and P_3	$-I_{p2}, -I_{p3}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	156	°C/W

Note

The device is protected against over-voltage caused by static charges.

[1]) Non return to zero.

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	3	MHz	
Clock pulse width	$t_{\phi 1L}$	0.125	–	1	µs	see timing diagram for parameter def.
	$t_{\phi 2L}$	0.125	–	1	µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10	µs	see note 1
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10	µs	see note 1
Clock delay times	$t_{\phi 1\phi 2}$	0	–	49	µs	
	$t_{\phi 2\phi 1}$	0	–	49	µs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Data input logic level						
HIGH	V_{IH}	−1.5	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	10	–	–	ns	

1) Above f_ϕ = 1.54 MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −24 V to −28 V; $V_{P_2} = V_{P_3}$ = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 20 kΩ to P_0

	Symbol	min.	typ.	max.		Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	bias: V_I = 0 V; f = 1 MHz
Clock input capacitance	$C_{\phi 1}, C_{\phi 2}$	–	19	25	pF	bias: V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}, C_{\phi 2}$	–	14	18	pF	bias: V_ϕ = −26 V; f = 1 MHz
Leakage currents:						
Data input currents	$-I_{IL}$	–	–	1	μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	300	600	Ω	
LOW	R_{QL}	–	250	500	Ω	$V_{P_2} = V_{P_3}$ = −5 V
Drive capability (see note 1 on page 5)	V_{QL}	–	−10	−8	V	R_L = 4 kΩ reference to P_0
	V_{QL}	–	−4.7	−4.4	V	$V_{P_2} = V_{P_3}$ = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2 on page 5)	$-I_{P_1}$	–	2.0	3.0	mA	V_{P_1} = −26 V; f = 1 MHz; T_{amb} = 25 °C
	$-I_{P_2}, -I_{P_3}$	–	2.4	3.0	mA	$V_{P_2} = V_{P_3}$ = −13 V; f = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: fall time	t_{DHL}	–	80	–	ns	
rise time	t_{DLH}	–	80	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

CHARACTERISTICS (continued)

Note 1 (see page 4)

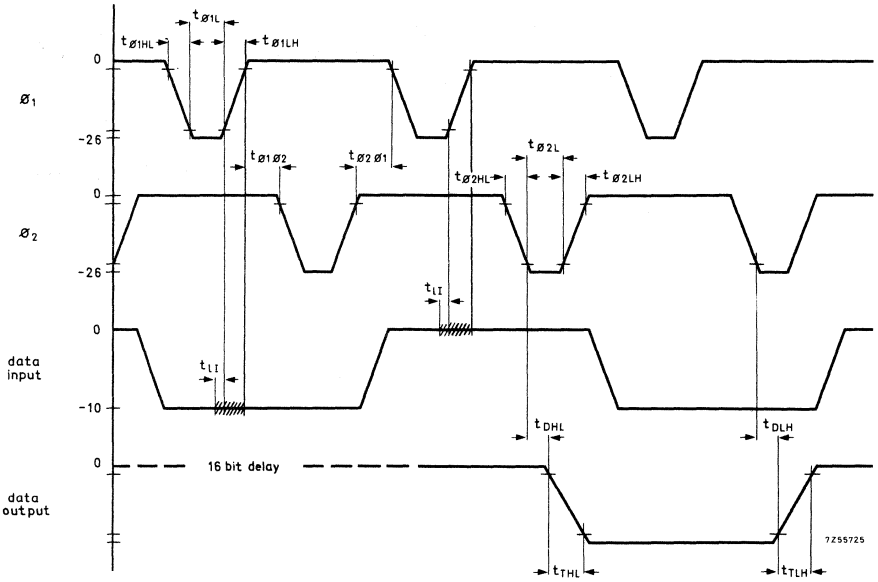
The maximum capacitive load that can be driven depends only on the speed deisred and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

Note 2 (see page 4)

The output buffer power supply currents (I_{P_2}, I_{P_3}) are almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Timing diagram note:

Input data must remain valid for the shaded interval to ensure proper entry into the register.

Note

The indicated points on the vertical axes are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

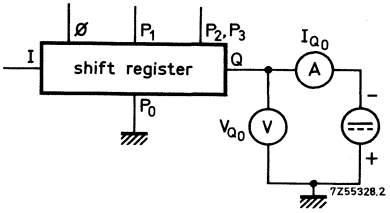
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
   The time between the end of the $\phi 1$ (or $\phi 2$) clock pulse and the start of the $\phi 2$ (or $\phi 1$) clock pulse, defined at -2 V.
5. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse $\phi 1$ for which the voltage at the input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
7. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
8. Fall delay time: t_{DHL}
   The delay between the clock pulse $\phi 2$ reaching LOW and the output beginning to change from HIGH to LOW.
9. Rise delay time: t_{DLH}
   The delay between the clock pulse $\phi 2$ reaching LOW and the output beginning to change from LOW to HIGH.

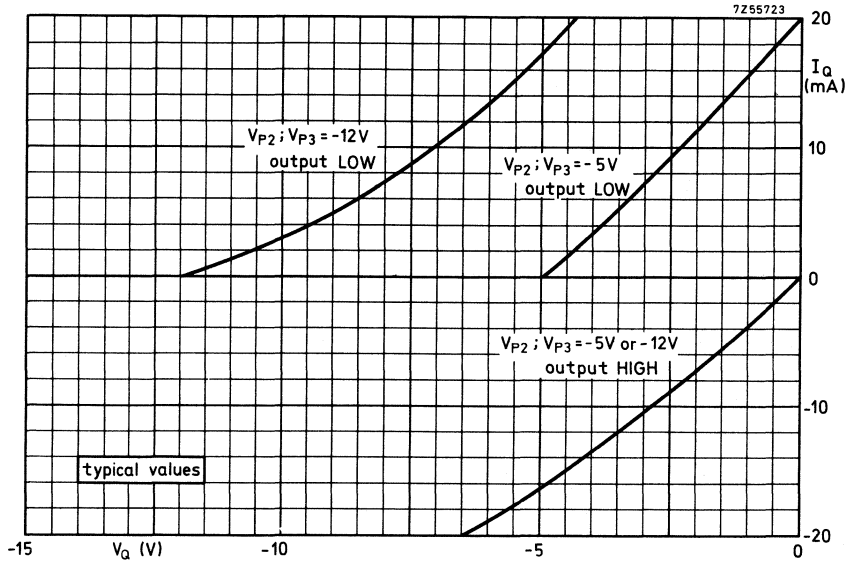
OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN186. They show V_Q versus I_Q for the V_{P2} and V_{P3} at −5 V and −12 V, for both HIGH and LOW output.

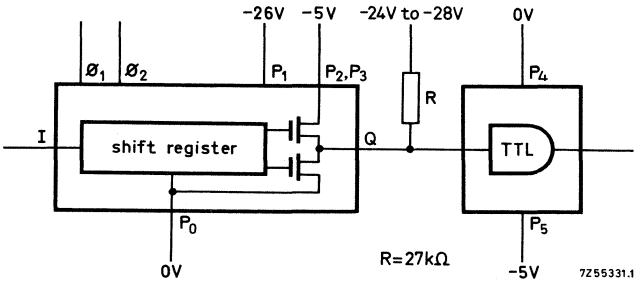
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.

The circuit shown may be used to obtain output curves for other values of V_{P2} and V_{P3}.

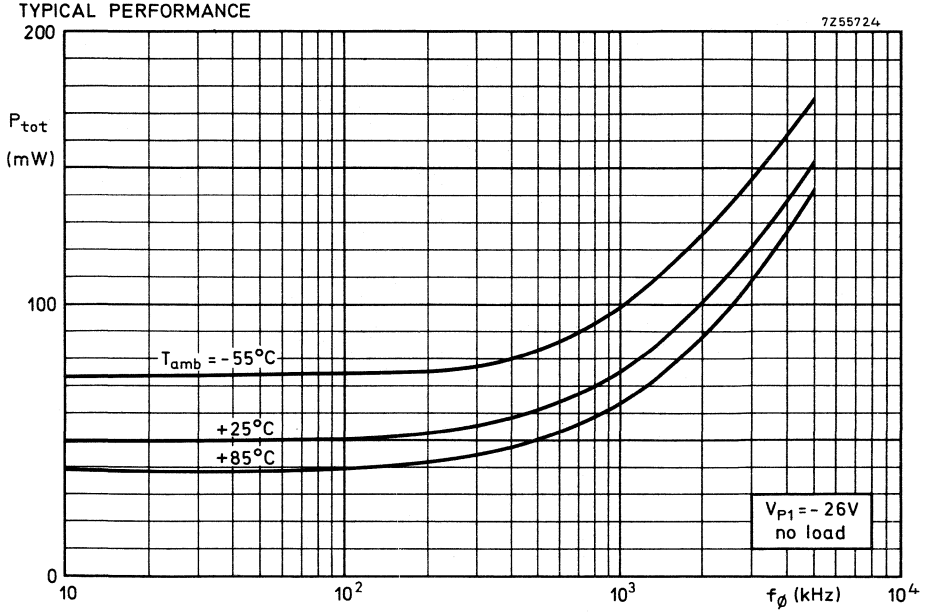


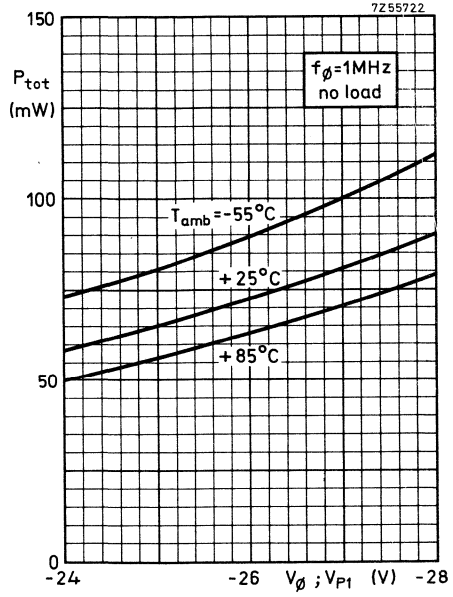


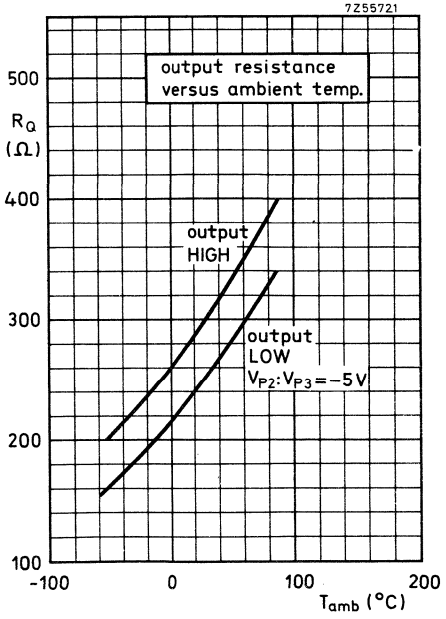
2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.



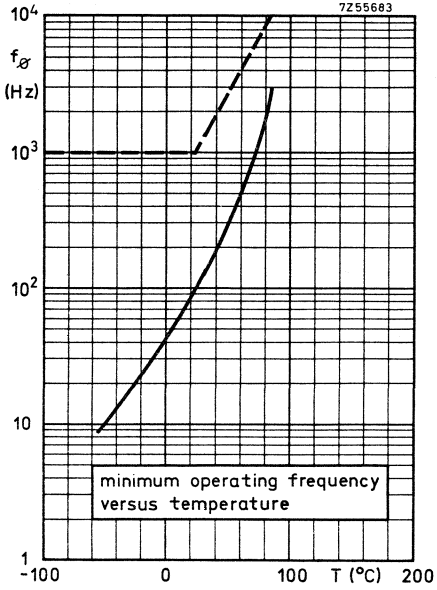
TYPICAL PERFORMANCE





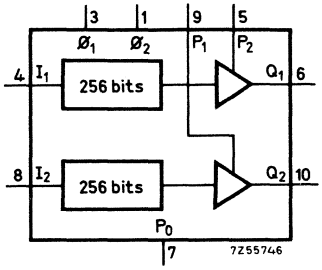


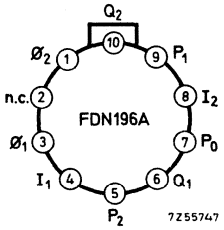
TYPICAL PERFORMANCE (continued)



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

DUAL 256-BIT DYNAMIC SHIFT REGISTER





P_0 connected to metal case

QUICK REFERENCE DATA			
Clock rate	f_ϕ	0.01 to 3	MHz
Power consumption per bit at f_ϕ = 3 MHz	P_{av}	typ. 0.36	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C
D.C. noise margin	M_H; M_L	> 1	V

PACKAGE OUTLINE: TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN196A consists of two 256-bit 2-phase dynamic shift registers, with common clock lines.
The device has two low impedance push-pull output buffers, with separate supply voltages. Thus the two outputs may be independently biased to drive a bipolar load or other MOS circuits.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminals P_1, P_2	$-I_{P_1}$, $-I_{P_2}$	max.	20	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	200	°C/W

Note
All terminals are protected against over-voltage due to static charges.

DRIVE REQUIREMENTS at T_{amb} = −55 to +85 °C; P_0 is grounded

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	3	MHz	
Clock pulse width	$t_{\phi 1L}$	0.125	–	5.0	μs	
	$t_{\phi 2L}$	0.125		5.0	μs	
Clock pulse rise time	$t_{\phi LH}$	–	–	0.5	μs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.5	μs	
Clock delay	$t_{\phi 1\phi 2}, t_{\phi 2\phi 1}$	0	–	45	μs	
Clock pulse voltage levels						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Data input logic levels						
HIGH	V_{IH}	−2	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	10	–	–	ns	
Buffer supply voltages	$-V_{P_1}, -V_{P_2}$	0	–	14	V	

CHARACTERISTICS

Test conditions: $V_{P_1} = V_{P_2} = -12$ to -14 V; $T_{amb} = -55$ to $+85\,^{o}C$; P_0 = grounded standard load: 50 pF in parallel with 20 kΩ to P_0.

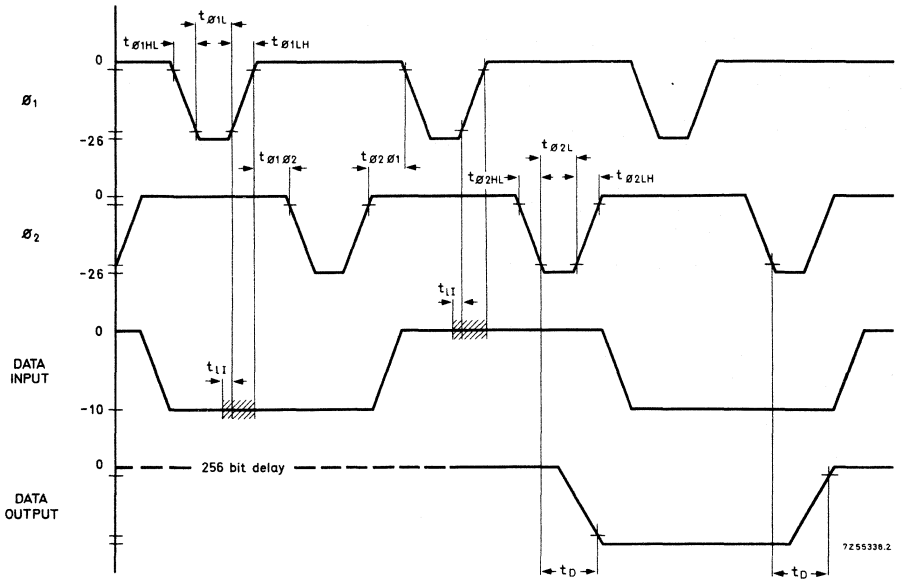
ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	V_I = 0 V; f = 1 MHz
Clock input capacitances	$C_{\phi 1}, C_{\phi 2}$	–	90	110	pF	V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}, C_{\phi 2}$	–	60	80	pF	V_ϕ = −26 V; f = 1 MHz
Leakage currents						
Data input current	$-I_{IL}$	–	–	1	μA	V_I = −15 V; all other terminals at P_0; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at P_0; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	250	500	Ω	
LOW	R_{QL}	–	150	300	Ω	V_{P1}, V_{P2} = −5 V
Supply currents	$-I_{P_1}, -I_{P_2}$	–	−0.68	−1.0	mA	V_{P_1}, V_{P_2} = −13 V; f = 1 MHz; T_{amb} = 25 °C; See note
Delay time						
Clock to output	t_D	–	135	275	ns	

Note

The output buffer power supply current is almost entirely dependent on the external load. The value shown is for a load of 50 pF is parallel with 1 MΩ to P_0.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.
2. With the FDN196A the data inputs must also remain valid for the $t_{\phi LH}$.
3. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

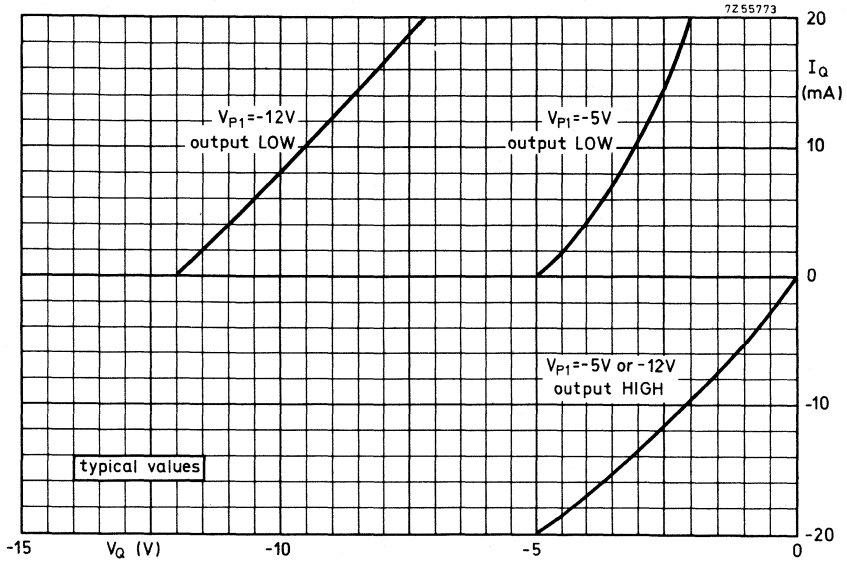
GLOSSARY OF TERMS

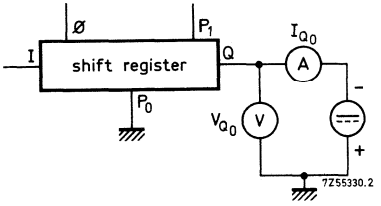
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -26$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
   The last allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Delay time: t_D
   The delay between the clock pulse ϕ_2 reaching LOW and the output reaching its logic level.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN196A. They show V_Q versus I_Q for the bias V_{P1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain LOW output curves for other values of V_{P1}.

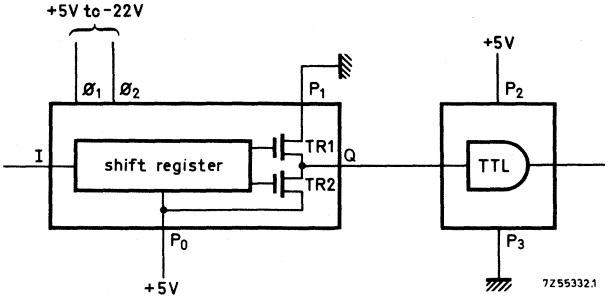
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





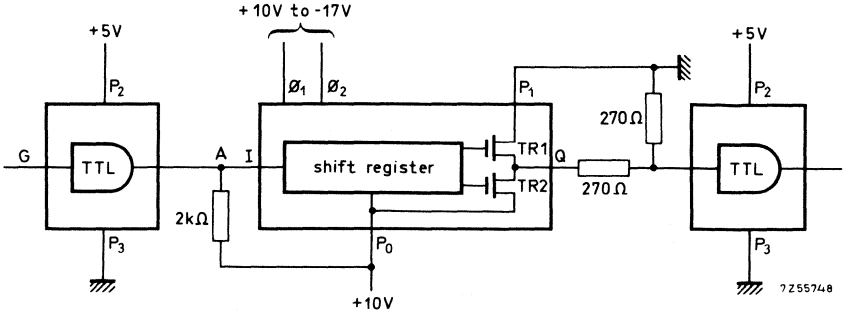
OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0}. TR1 and TR2 are the push-pull output driver transistors of the FDN146.



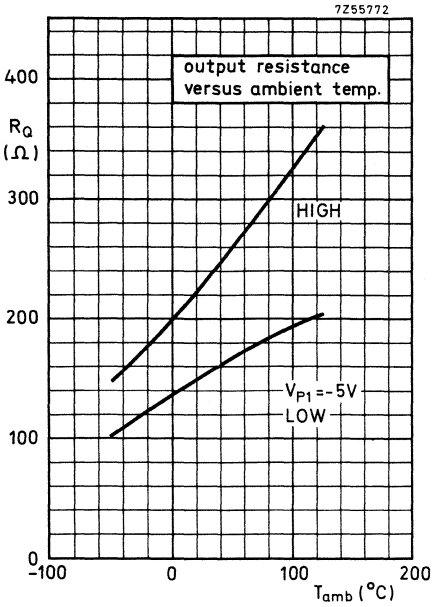
Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at and output using only passive interface components.
Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A), most circuits of our FC series and most FJ gates satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V.



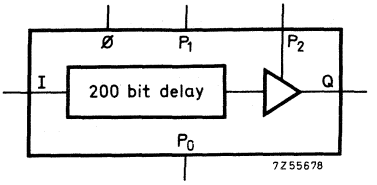
Biasing circuit B

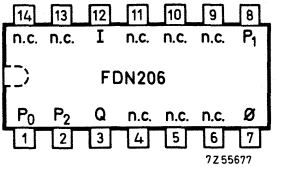
4. To drive MOS loads direct, the bias V_{P1} should be between −12 and −14 V to P_0.

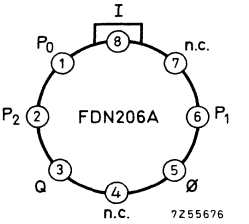

7Z55772
output resistance
versus ambient temp.
400
R_Q
(Ω)
300
200
100
0
HIGH
V_{P1} = -5V
LOW
-100
0
100
200
T_{amb} (°C)

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

200-BIT DYNAMIC SHIFT REGISTER







FDN206 : P_0 connected to the metal bottom
FDN206A: P_0 connected to the metal case

QUICK REFERENCE DATA			
Supply voltage	V_{P1}	−26 to −28	V
D.C. noise margin	M_L; M_H	> 1	V
Clock rate	f_ϕ	0.01 to 1	MHz
Power consumption per bit at $f\phi$ = 10 kHz	P_{av}	< 0.2	mW
$f\phi$ = 1 MHz	P_{av}	< 0.6	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINES: FDN206 ; 14 lead dual in-line (See General Section)
FDN206A; TO-99 (See General Section)

GENERAL DESCRIPTION

The FDN206 contains one 200-bit shift register with one serial input and one serial output. It dissipates little power and uses a one-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads.
The buffer supply terminal P_2 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse.
With the FDN206, the FDN116 (a quadruple 32-bit shift register) and FDN136 (a variable length 1 to 64-bit shift register) shift registers of any required length can be built from off-the-shelf parts.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0				+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	FDN206 :	P_{tot}	max.	800	mW
	FDN206A:	P_{tot}	max.	625	mW
Junction temperature		T_j	max.	150	°C
Storage temperature		T_{stg}		−65 to +150	°C
Total current through terminal P_2		$-I_{P_2}$	max.	40	mA
Output current (per output)		$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	FDN206 :	$R_{th\ j\text{-}a}$	=	156	°C/W
	FDN206A:	$R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	1	MHz	
Clock pulse width	$t_{\phi L}$	0.45	–	50	µs	See timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10	µs	See note
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10	µs	
Clock pulse space	$t_{\phi H}$	0.45	–	50	µs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−12	−9	V	
Data input logic levels						
HIGH	V_{IH}	−2	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	20	–	–	ns	
Data hold time	t_{hI}	75	–	–	ns	
Supply voltages	V_{P1}	−28	−26	−24	V	$f_\phi \leq$ 750 kHz
	V_{P1}	−28	−27	−26	V	$f_\phi \geq$ 750 kHz
	V_{P2}	−28	–	+0.3	V	

Note

The fall time specified for the FDN206 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers are operating in series from a common clock. If a register does not drive other registers the clock fall time may be longer.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −26 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load; 50 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.	max.		Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	bias: V_I = 0 V; f_ϕ = 1 MHz
Clock input capacitance	C_ϕ	–	6	10	pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
Leakage currents						
Data input currents	$-I_{IL}$	–	–	1	μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance:						
HIGH	R_{QH}	–	250	500	Ω	
LOW	R_{QL}	–	250	500	Ω	V_{P_2} = −5 V
Drive capability (see note 1)	V_{QL}	–	−4.8	−4.6	V	V_{P_2} = −5 V; R_L = 4 kΩ to reference P_0
Supply current (see note 2)	$-I_{P_2}$	–	1.0	1.5	mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	–	5.0	8.0	mA	V_{P_1} = −27 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: fall time	t_{DHL}	–	300	–	ns	
rise time	t_{DLH}	–	300	–	ns	
D.C. noise margin	M_L	1	–	–	V	
	M_H	1.5	–	–	V	

Note 1

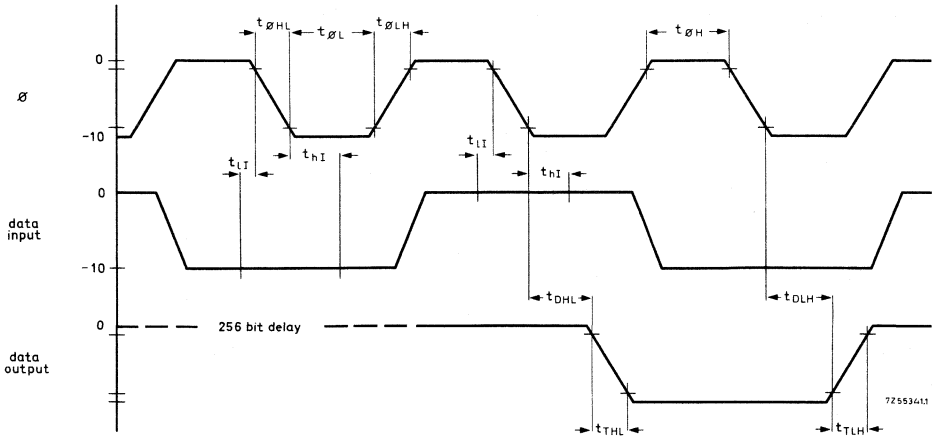
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 7 and 8 for further information on output drive capability.

Note 2

The output buffer supply current I_{P_2} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -9$ V.

2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.

3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.

4. Clock pulse space: $t_{\phi H}$
   The least allowable time between the end of one clock pulse (ϕ) and the start of the next.

5. Data lead time: $t_{\ell I}$
   The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.

6. Data hold time: t_{hI}
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered in the register.

7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

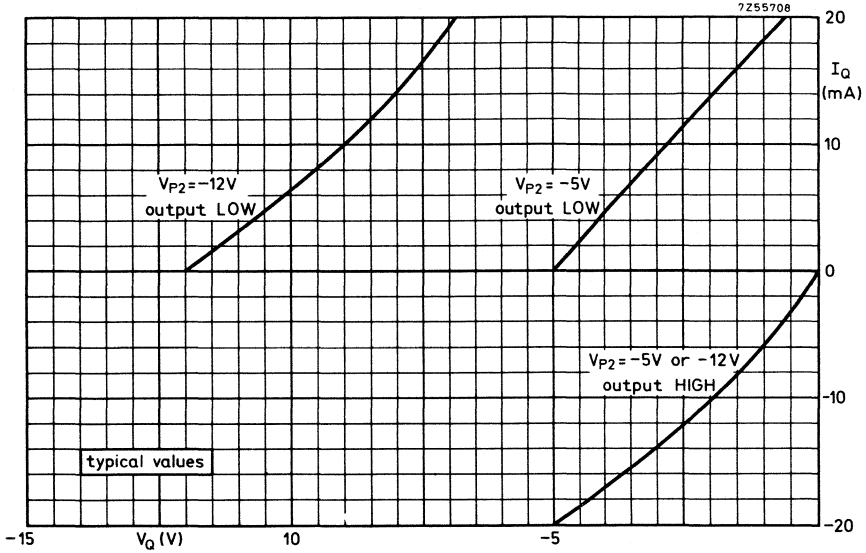
9. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.

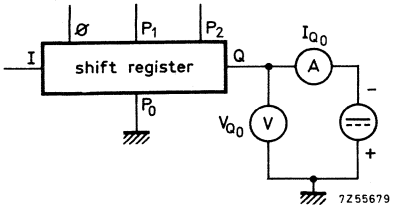
10. Rise delay time: t_{DLH}
    The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN206. They show V_Q versus I_Q for the bias V_{P1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain LOW output curves for other values of V_{P2}.

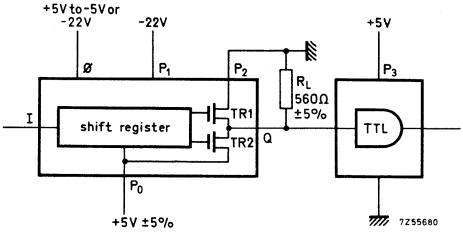
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





OUTPUT BUFFER DESCRIPTION (continued)

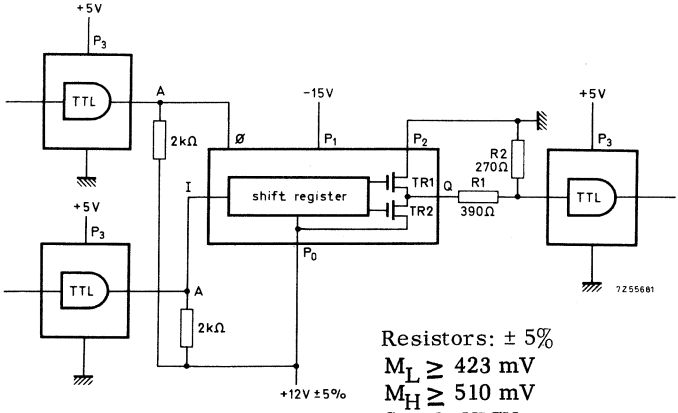
2 Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0}. TR1 and TR2 are the push-pull output driver transistors of the FDN206.



$M_L \geq 368$ mV
$M_H \geq 458$ mV
Steady HIGH state dissipation ≤ 13 mW

Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A); most non-R_C type circuits of our FC series and most FJ gates satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V (FJH301; FJH311; FJH321).

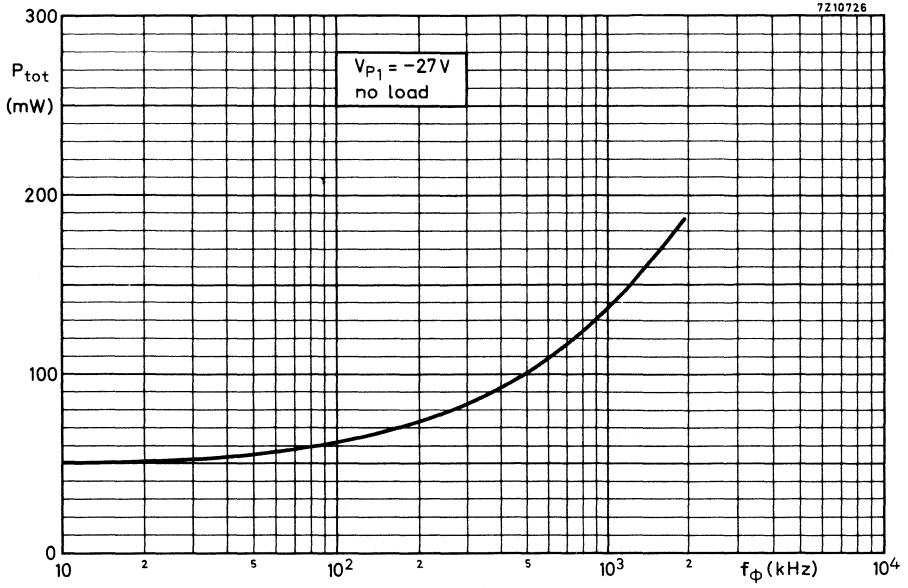


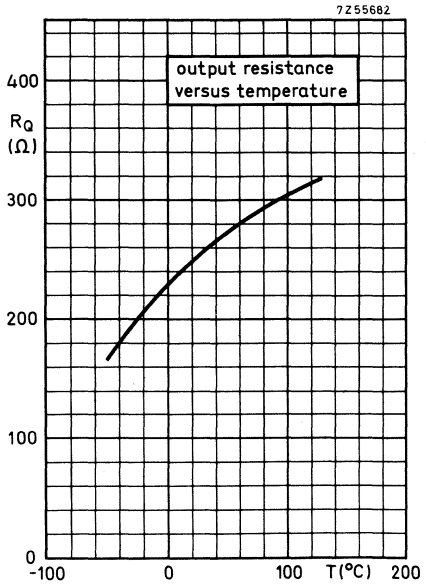
Resistors: ± 5%
$M_L \geq 423$ mV
$M_H \geq 510$ mV
Steady HIGH state dissipation ≤ 55 mW

Biasing circuit B

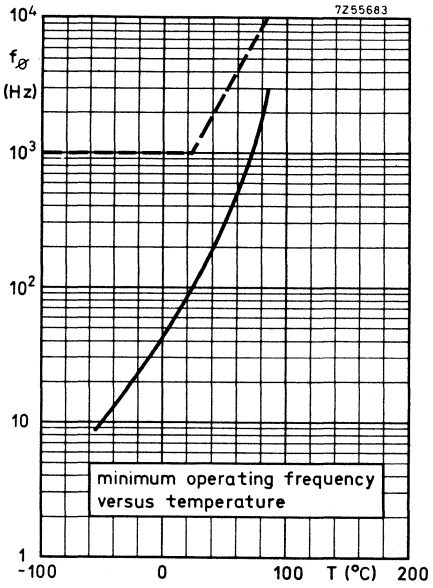
4. To drive MOS loads direct, the bias V_{P0} should be between −12 and −14 V to P_0.

TYPICAL PERFORMANCE



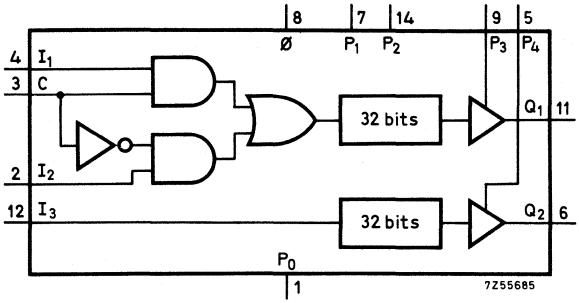


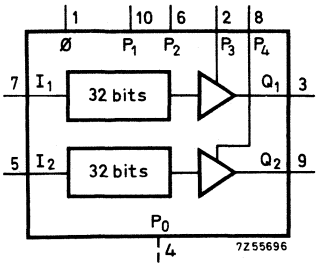
TYPICAL PERFORMANCE (continued)

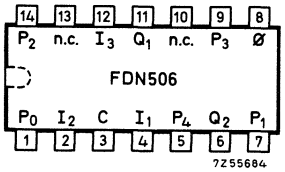


The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

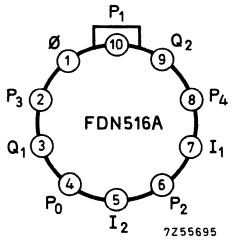
DUAL 32-BIT STATIC REGISTER







P_0 connected to the metal bottom



P_0 connected to the metal case

QUICK REFERENCE DATA				
Supply voltages	V_{P1}	−24 to −28		V
	V_{P2}	−12 to −14		V
Clock frequency	f_ϕ	0 to 1.5		MHz
Power consumption per bit at f_ϕ = 1.5 MHz	P_{av}	typ.	2	mW
Operating ambient temperature	T_{amb}	−55 to +85		°C
D.C. noise margin	M_H, M_L	>	1	V

PACKAGE OUTLINE: FND506; 14 lead ceramic dual in-line (See General Section)
FDN516A; TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN506 and FDN516A are dual 32-bit static shift registers. They require a single phase, low voltage, external clock signal, and may be operated down to d.c. without loss of stored information. Both devices utilize common power and clock lines; the output buffer supplies are separated to facilitate independent biasing for MOS or TTL load drive.

The FDN506 contains the gating, external SELECT command and data inputs for selection of two independent data streams.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0				+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	FDN506	P_{tot}	max.	800	mW
	FDN516A	P_{tot}	max.	625	mW
Junction temperature		T_j	max.	150	°C
Storage temperature		T_{stg}		−65 to +150	°C
Total current through terminals P_3, P_4		$-I_{P3}$,$-I_{P4}$	max.	40	mA
Output current (per output)		$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	FDN506	$R_{th\ j\text{-}a}$	=	156	°C/W
	FDN516A	$R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0	–	1.5 MHz	
Clock pulse width	$t_{\phi H}$	0.24	–	50 µs	See timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 µs	See note
Clock pulse rise time	$t_{\phi LH}$	–	–	1.0 µs	
Clock pulse space	$t_{\phi L}$	0.36	–	– µs	
Clock pulse voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−12	−9 V	
Data/select input logic levels					
HIGH	V_{IH}, V_{CH}	−2	0	+0.3 V	
LOW	V_{IL}, V_{CL}	−28	−12	−9 V	
Data/select lead time	$t_{\ell I}, t_{\ell C}$	50	–	–	
Data/select hold time	t_{hI}, t_{hC}	100	–	–	

Note:

The fall time specified for the FDN506 and FDN516A is to ensure that output data will meet the input hold time requirements of other registers, when more shift registers are operating in series from a common clock. If a register does not drive other registers the clock fall times may be longer.

CHARACTERISTICS (continued)

Test conditions: $V_{P_1} = -24$ V to -28 V; $V_{P_2} = V_{P_3} = V_{P_4} = -12$ V to -14 V; $T_{amb} = -55$ to $+85$ °C; P_0 = grounded; standard load : 50 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.	max.		Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data/select input capacitance	C_I, C_C	–	2	3.5	pF	bias: $V_I = V_C = 0$ V; f = 1 MHz
Clock input capacitance	C_ϕ	–	6	8	pF	bias: $V_\phi = 0$ V; f = 1 MHz
Leakage currents						
Data/select input currents	$-I_{IL}$, $-I_{CL}$	–	–	1	μA	$V_I = V_C = -15$ V; all other terminals at V_{P0}; $T_{amb} = 25$ °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	$V_\phi = -28$ V; all other terminals at V_{P0}; $T_{amb} = 25$ °C
Output resistance						
HIGH	R_{QH}	–	360	600	Ω	$T_{amb} = 25$ °C
LOW	R_{QL}	–	220	500	Ω	$V_{P3} = V_{P4} = -5$ V; $T_{amb} = 25$ °C
	R_{QL}	–	330	–	Ω	$V_{P3} = V_{P4} = -10$ V; $T_{amb} = 25$ °C
Drive capability (See note 1)	V_{QL}	–	−10	−8	V	R_L = 4 kΩ to reference P_0
	V_{QL}	–	−4.7	−4.4	V	$V_{P3} = V_{P4} = -5$ V; R_L = 4 kΩ to reference P_0
Supply current (See note 2)	$-I_{P2}$	–	4.0	6.0	mA	$V_{P2} = -13$ V; f = 1.5 MHz; $T_{amb} = 25$ °C
	$-I_{P1}$	–	3.0	4.5	mA	$V_{P1} = -26$ V; f = 1.5 MHz; $T_{amb} = 25$ °C
Output transition times:						
fall time	t_{THL}	–	80	–	ns	
rise time	t_{TLH}	–	80	–	ns	
Delaytimes: fall time	t_{DHL}	–	260	–	ns	
rise time	t_{DLH}	–	260	–	ns	
D.C. noise margin	M_L	1.0	–	–	V	
	M_H	1.5	–	–	V	

Note 1

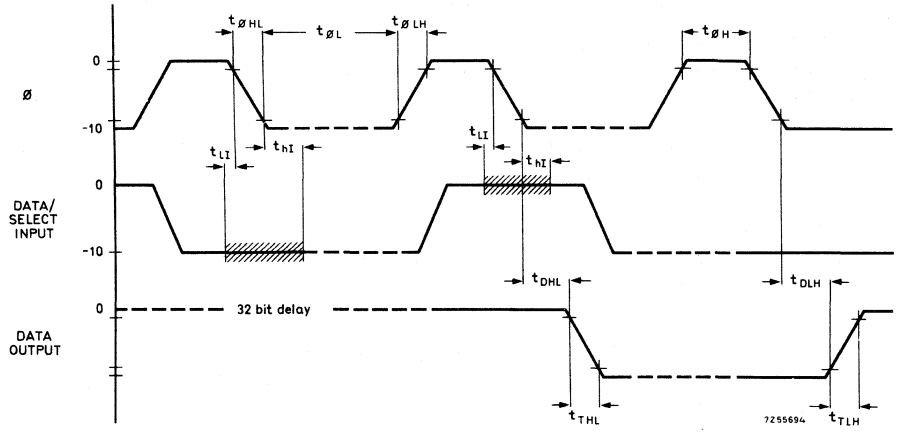
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 5 and 6 for further information on output drive capability.

Note 2

The output buffer power supply current is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes:

1. Clock pulse ϕ is normally kept LOW.
2. The data and select inputs must remain valid for the shaded interval to ensure proper selection and entry of input data.
3. Data is kept in the register for arbitrarity long periods by keeping the clock LOW.

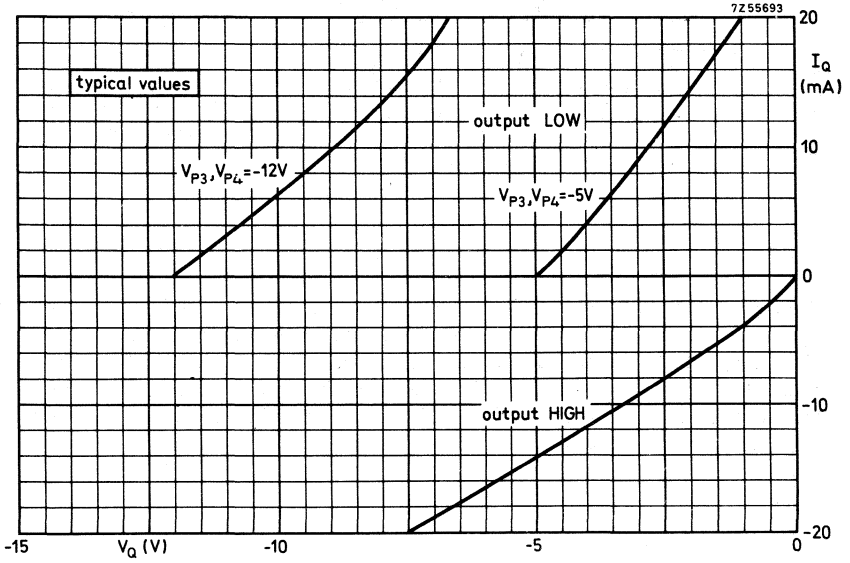
CHARACTERISTICS (continued)

GLOSSERY OF TERMS

1. Clock pulse width: $t_{\phi H}$
   The time for which the clock pulse is HIGH: $V_{\phi H} \geq -2$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock pulse space: $t_{\phi L}$
   The least allowable time between the end of one clock pulse (ϕ) and the start of the next, measured at -9 V.
5. Data lead time: $t_{\ell L}$
   The time before the -2 V point on the clock pulse for which the voltage at the data/select input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Data hold time: t_{hl}
   The time after the clock pulse ϕ reaches LOW(-9 V) for which the data/select inputs must remain stable in order to ensure that the data will be entered in the register.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
10. Rise delay time: t_{DLH}
    The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN506 and FDN516A.
   The output buffer supply voltages may be varied between 0 and −14 V according to the output voltage swing required. It does not affect the operating speed of the register.

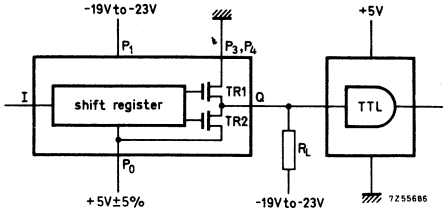


Note

When operating with high output current levels, the maximum power rating must not be exceeded.

OUTPUT BUFFER DESCRIPTION (continued)

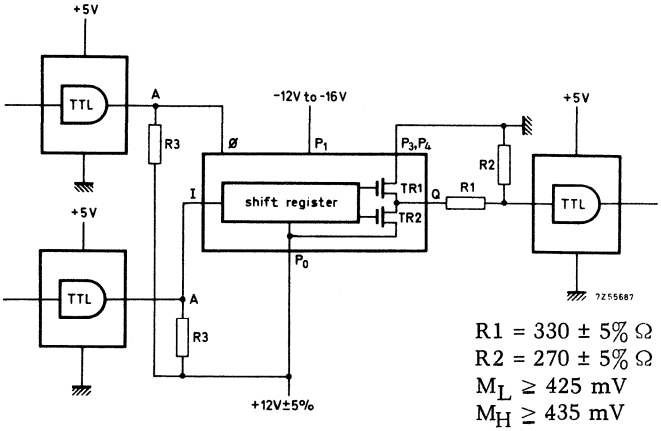
2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0}. TR1 and TR2 are the push-pull output driver transistors of the FDN506 and FDN516A.



R_L = 22 ± 5% kΩ
$M_L \geq$ 450 mV
$M_H \geq$ 1.5 V
Steady HIGH state dissipation < 1 mW

Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead (point A), most circuits of our FC series (non-R_C types) satisfy this requirement. The open collector FJ gates FJH301, FJH311 and FJH321 have a minimum output breakdown voltage guarantee of 15 V.



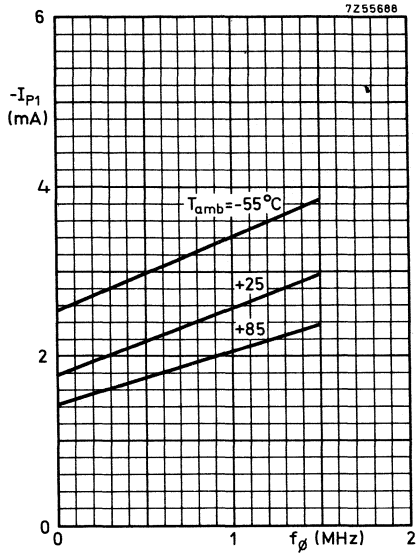
R1 = 330 ± 5% Ω
R2 = 270 ± 5% Ω
$M_L \geq$ 425 mV
$M_H \geq$ 435 mV
Steady HIGH state dissipation ≤ 63 mW

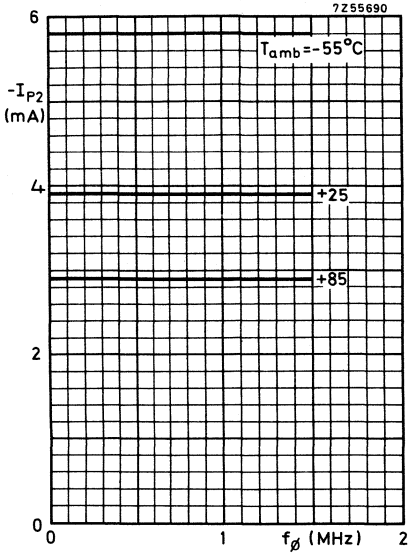
Biasing circuit B

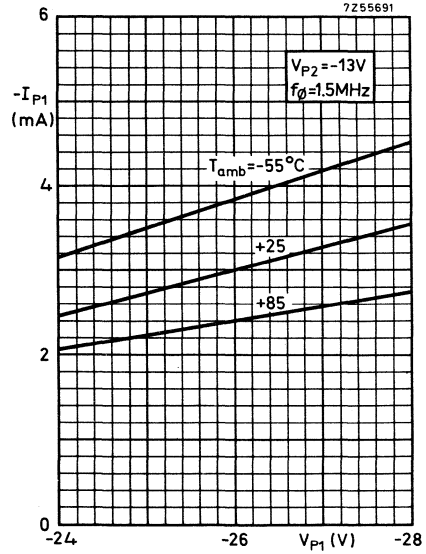
4. To drive MOS loads direct, the bias V_{P3} and V_{P4} should be between −12 and −14 V to P_0.

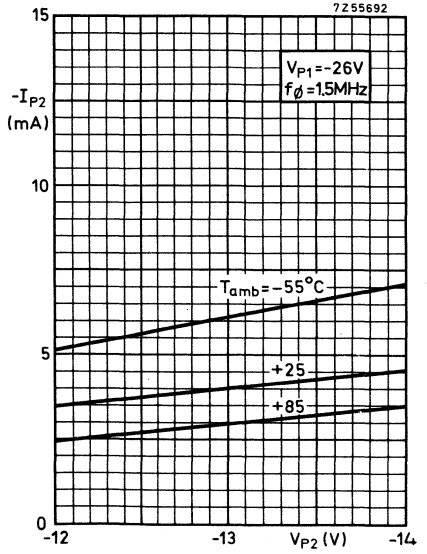
TYPICAL PERFORMANCE at P_0 = grounded; standard load : 50 pF in parallel with 20 kΩ to P_0.

Test condition: $V_{P1} = -26$ V; $V_{P2} = -13$ V



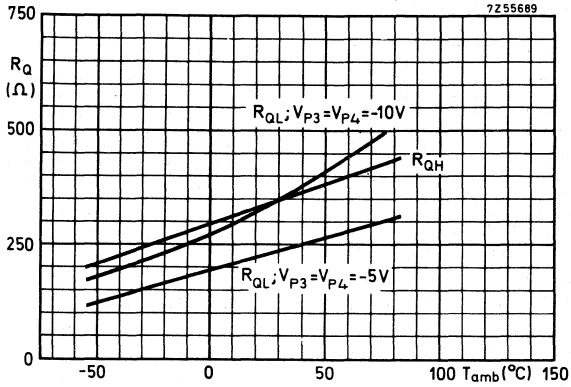






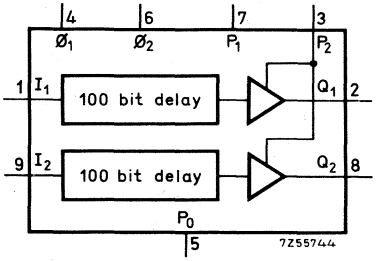
TYPICAL PERFORMANCE (continued)

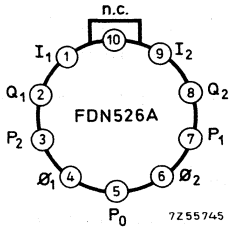
Test conditions: P_0 = grounded; $V_{P_1} = -26$ V; $V_{P_2} = -13$ V



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 100-BIT STATIC SHIFT REGISTER





P_0 connected to metal case

QUICK REFERENCE DATA			
Clock rate	f_ϕ	0 to 3	MHz
Supply voltage	V_{P_1}	−24 to −28	V
Power consumption per bit at f_ϕ = 3 MHz	P_{av}	typ. 2	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C
D.C. noise margin	M_H, M_L	> 1	V

PACKAGE OUTLINE: TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN526A is a monolithic dual 100-bit shift register. The two shift registers have each one serial input and output. They operate from common clocks and supply lines. The device has low impedance push-pull output buffers, which, when appropriately biased, are capable of interfacing direct with MOS, TTL, DTL and other loads.
The buffer supply terminal P_2 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of supply voltage V_{P_1}, the amplitude and width of the clock pulses.
All inputs, outputs, supply terminals and clock inputs are protected against static voltages.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	^oC
Storage temperature	T_{stg}		−65 to +150	^oC
Total current through terminal P_2	$-I_{P_2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	200	$^oC/W$

DRIVE REQUIREMENTS at T_{amb} = −55 to +85 °C; P_0 = grounded

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0	–	2	MHz	$V_{P_1}, V_{\phi L}$=−24 V
		0	–	3	MHz	$V_{P_1}, V_{\phi L}$=−26 V
Clock pulse width [1])	$t_{\phi 1L}$	0.2	–	10	µs	$V_{P_1}, V_{\phi L}$=−24 V
		0.1	–	10	µs	$V_{P_1}, V_{\phi L}$=−26 V
	$t_{\phi 2L}$	0.2	–	–	µs	$V_{P_1}, V_{\phi L}$=−24 V
		0.15	–	–	µs	$V_{P_1}, V_{\phi L}$=−26 V
Clock pulse rise time	$t_{\phi LH}$	–	–	0.5	µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.5	µs	
Clock delay	$t_{\phi 1\phi 2}, t_{\phi 2\phi 1}$	0	–	–	µs	
Clock pulse voltage levels						
HIGH	$V_{\phi H}$	−2	–	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Data input logic levels						
HIGH	V_{IH}	−2.0	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	20	–	–	ns	

[1]) See timing diagram on page 5.

CHARACTERISTICS

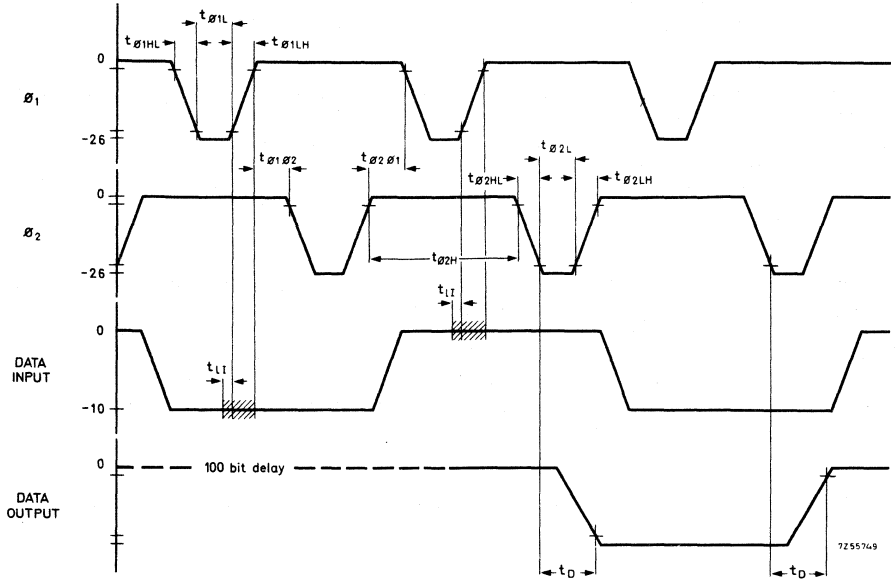
Test conditions: V_{P_1} = −24 to −28 V; V_{P_2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 25 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.[1])	max.		Conditions and references
Output levels						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	V_I = 0 V; f = 1 MHz
Clock input capacitances	$C_{\phi 1}, C_{\phi 2}$	–	17	25	pF	V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}, C_{\phi 2}$	–	15	22	pF	V_ϕ = −26 V; f = 1 MHz
Leakage currents						
Data input current	$-I_{IL}$	–	–	1	μA	V_I = −15 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	400	750	Ω	V_Q = −1 V
Drive capability	V_{QL}	–	−11.3	−8	V	R_L = 4 kΩ to P_0; V_{P_2} = −5 V
Supply currents	$-I_{P_1}$	–	1.1	1.8	mA	V_{P_1} = −26 V; f = 1 MHz; T_{amb} = 25 °C; R_L = 1 MHz
	$-I_{P_2}$	–	9.3	18	mA	V_{P_2} = −13 V; f = 1.5 MHz; T_{amb} = 25 °C; R_L = 1 MHz
Delay times						
Clock to output	t_D	–	150	275	ns	
D.C. noise margin	M_H, M_L	1	–	–	V	

[1]) Typical values measured at: V_{P_1} = −26 V; V_{P_2} = −13 V; $V_{\phi L}$ = −26 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.
2. For d.c. operation $\phi 2$ should be kept LOW.

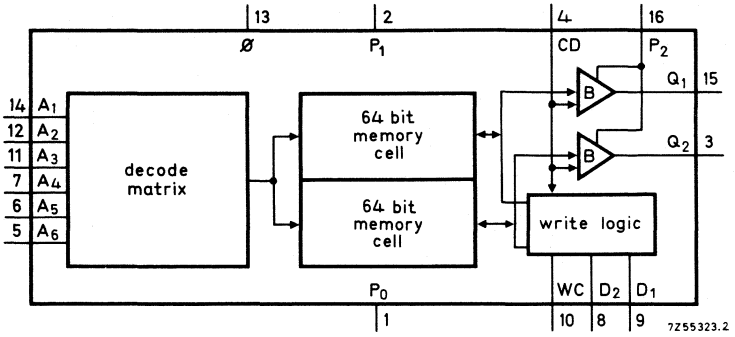
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

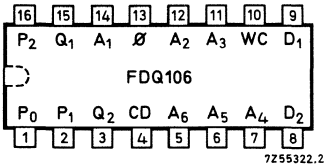
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} = -26$ V
2. Clock pulse space: $t_{\phi 2H}$
   The time for which the clock pulse $\phi 2$ is HIGH ($V_{\phi} > -2$ V).
3. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
4. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
5. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or $\phi 2$) clock pulse and the start of the $\phi 2$ (or ϕ_1) clock pulse, defined at -2 V.
6. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Delay time: t_D
   The delay between the clock pulse reaching LOW and the output reaching its logic level.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ/WRITE RANDOM ACCESS MEMORY, 128-BIT, 64 WORD, 2 BITS PER WORD



WC = write control; CD = chip disable



P0 and metal package bottom are connected

QUICK REFERENCE DATA				
Supply voltage	V_{P_1}	−26 to −28		V
Standby power per bit (required clock power)		typ.	3	μW
Total power consumption at 1 MHz read-rate	P_{tot}	typ.	135	mW
Read access time	t_{AR}	<	1	μs
D.C. noise margin	M_L, M_H	>	1	V
Data read rate	f_{DR}	<	1	MHz
Data write rate	f_{DW}	<	1	MHz
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE: 16 lead metal-ceramic dual in-line (See general section)

GENERAL DESCRIPTION

The FDQ106 is a monolithic, 128 bit random access read/write memory. It is organized as two 64 bit memories with 6 common single-rail address inputs and two separate outputs; it is used as a 64 word, 2-bits per word memory. It requires a single-phase clock strobe pulse to refresh the data stored in all the memory cells simultaneously and to change the data stored in a cell in the write mode.
It also incorporates a chip disable that inhibits both data inputs and output buffers for expanded memory applications. The memory is activated in the write mode by applying a write control pulse; at all other times it is in the read mode.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to −30		V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to +150		°C
Total current through terminal P_2	$-I_{P_2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	156	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.	Conditions and references
Data read rate	f_{DR}	–	–	1 MHz	
Data write rate	f_{DW}	–	–	1 MHz	
Strobe rate	f_{ϕ}	0.01	–	1 MHz	
Strobe pulse width	$t_{\phi H}$	0.08	–	5 µs	see timing diagram for parameter definitions
Write control pulse width	t_{WL}	0.5	–	10 µs	
Write control and strobe pulse rise time:	t_{WLH}	–	–	0.1 µs	
	$t_{\phi LH}$	–	–	0.1 µs	
fall time:	t_{WHL}	–	–	0.1 µs	
	$t_{\phi HL}$	–	–	0.1 µs	
Write control and strobe pulse voltage levels:					
HIGH	V_{WH}; $V_{\phi H}$	−2	0	+0.3 V	
LOW	V_{WH}; $V_{\phi L}$	−28	−27	−26 V	
Address, data, and chip disable input logic levels:					
HIGH	V_{AH}, V_{DH}, V_{CDH}	−2	0	+0.3 V	
LOW	V_{AL}, V_{DL}, V_{CDL}	−28	−12	−9 V	
Write address lead time	$t_{\ell WA}$	0.35	–	– µs	
Strobe address lead time	$t_{\ell \phi A}$	0.76	–	– µs	
Strobe write lead time	$t_{\ell W \phi HL}$	0.40	–	– µs	

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −26 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 50 kΩ to P_0.

	Symbol	min.	typ.	max.	Conditions and references
ELECTRICAL DATA					
Read access time	t_{AR}		0.2	0.5 1.0 μs	
Data output logic levels					
HIGH	V_{QH}	−1.0	−	0 V	
LOW	V_{QL}	−14	−	−10 V	
Address and data input capacitance	C_A, C_D	−	4.5	6.0 pF	bias: V_A; V_D = 0 V; f_ϕ = 1 MHz
Chip disable input capacitance	C_{CD}	−	7.0	9.0 pF	bias: V_{CD} = 0 V; f_ϕ = 1 MHz
Strobe input capacitance	C_ϕ	−	56	68 pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
	C_ϕ	−	28	35 pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Write control input capacitance	C_W	−	7.9	9.2 pF	bias: V_{WC} = 0 V; f_ϕ = 1 MHz
	C_W	−	5.8	7.0 pF	bias: V_{WC} = −26 V; f_ϕ = 1 MHz
Data output capacitance	C_Q	−	3.5	4.5 pF	bias: V_Q = 0 V; f_ϕ = 1 MHz
Leakage currents:					
Address, data, chip disable input currents	$-I_{AL}$, $-I_{DL}$, $-I_{CDL}$	−	−	1 μA	bias: V_A; V_D; V_{CD} = −15 V; see note 2
Strobe and write control input currents	$-I_{\phi L}$, $-I_{WL}$	−	−	100 μA	bias: V_ϕ; V_{WC} = −28 V; all see note 2
Output leakage current	$-I_Q$	−	−	10 μA	V_Q = 10 V; CD = LOW; T_{amb} = 25 °C
Output resistances:					
HIGH	R_{QH}	−	250	600 Ω	
LOW	R_{QL}	−	250	600 Ω	V_{P_2} = −5 V
Power supply current drain: at V_{P_1}	$-I_{P_1}$	−	4.5	7.5 mA	V_{P_1} = −28 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
at V_{P_2} (see note 1)	$-I_{P_2}$	−	0.8	1.0 mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:					
fall time	t_{THL}	−	100	− ns	
rise time	t_{TLH}	−	100	− ns	
D.C. noise margin	M_L, H_M	1	−	− V	

Notes

1. I_{P_2} is almost entirely dependent on the external load.
2. T_{amb} = 25 °C; all other terminals at V_{P0}

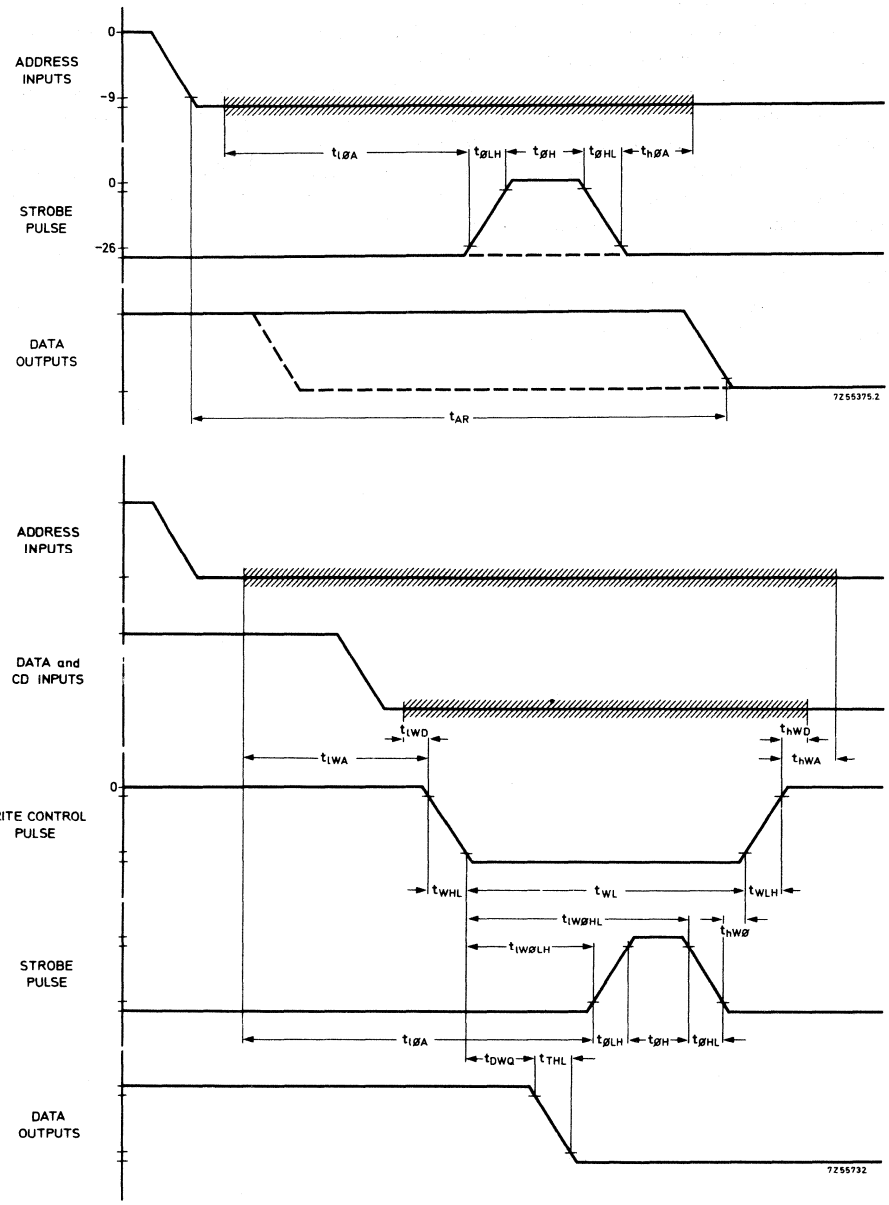
CHARACTERISTICS (continued)

STAND-BY POWER CONSIDERATIONS

If the FDQ106 is to be kept in stand-by condition with all d.c. power to it shut off, the stored data can be preserved by maintaining a 10 kHz strobe clock rate.
Since essentially all d.c. power dissipation is in the address input inverters, decode circuits and output buffers, the power required to preserve the stored data is limited to reactive strobe power and whatever leakage current occurs at the strobe input lead. Since the reactive strobe power is frequency dependent, the lowest allowable frequency should be used for stand-by operation. A strobe frequency of less than 10 kHz may be used if the ambient temperature is less than +85 ^{o}C.
D.C. power may be switched on and off only at those moments when a change of address is also allowable.
After re-application of d.c. power, a series of about 10 strobe pulses is required before the circuit is fully operational.

CHARACTERISTICS (continued)

TIMING DIAGRAM



CHARACTERISTICS (continued)

Timing diagram notes

1. To avoid destroying data in non-addressed memory cells, the address inputs must not be made to change state during the shaded intervals in the timing diagrams.
2. When the CD input is LOW, the WRITE logic is inoperative and the output is floating. The CD input affects the output directly, with a propagation delay of about 100 ns. It may change state an any time except during the shaded interval in the timing diagram.
3. No strobe pulse is required during a READ cycle; however, a minimum strobe frequency of 10 kHz is required and strobe pulses may occur during READ cycles if the requirement of note 1 is observed.
4. To write into the device, a WRITE control pulse and a strobe pulse are required, and the CD input must be HIGH.
   During a WRITE cycle the memory outputs are active and the new data will appear at the outputs after t_{DWQ} ($\leq$ 200 ns).
   However, data is actually written into the memory cell by the trailing edge of the strobe pulse.
5. Wheter they are in READ or WRITE cycles, all memory cells are simultaneously refreshed during a strobe pulse. No cycling through addresses is required.
6. If the address inputs remain unchanged, the data outputs appear as d.c. levels, no return to zero.

GLOSSARY OF TERMS

1. Strobe pulse width: $t_{\phi H}$
   The time for which the strobe pulse is in the HIGH state (ϕ is nominally LOW)
2. Write control pulse width: t_{WL}
   The time for which the WRITE control pulse is LOW ($V_{WL} \leq -26$ V)
3. Pulse fall time: t_{WHL} and $t_{\phi HL}$
   The time between the 10 % and 90 % voltage points as the pulse goes from HIGH to LOW.
4. Pulse rise time: t_{WLH} and $t_{\phi LH}$
   The time between the 90 % and 10 % voltage points as the pulse goes from LOW to HIGH.
5. Strobe address lead time: $t_{\ell \phi A}$
   The time before the 10 % strobe pulse voltage point for which the address must be present.
6. Write address lead time: $t_{\ell WA}$
   The time before the 10 % write control pulse voltage point for which the address must be present.
7. Write data lead time: $t_{\ell WD}$
   The time before the 10 % write control pulse voltage point for which the data must be present at the data inputs ($t_{\ell WD} \geq 0$)
8. Read access time: t_{AR}
   After the address inputs reach the correct level, the time that elapses before the outputs start to change state.

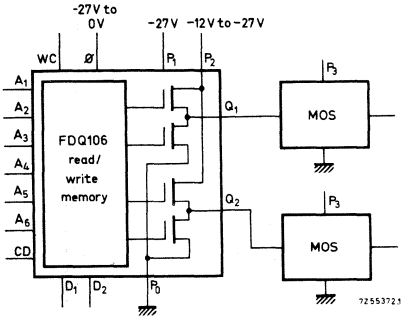
CHARACTERISTICS (continued)

9. Write-pulse-to-output propagation time: t_{DWQ}
   After the write control pulse reaches the LOW state, the time that elapses before the outputs start to change state.
10. Output fall transition time: t_{THL}
    The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
11. Output rise transition time: t_{TLH}
    The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
12. Write address and write data hold times: t_{hWA} and t_{hWD}
    The time for which the write control pulse must be in the HIGH state before the address or inputs may change state ($t_{hWA} \geq 0$ and $t_{hWD} \geq 0$).
13. Strobe address hold time: $t_{h\phi A}$
    The time for which the strobe pulse must be LOW before the address may change state ($t_{h\phi A} \geq 0$)
14. Write control-strobe pulse lead times: $t_{\ell W\phi LH}$ and $t_{\ell W\phi HL}$
    The time before the 10% voltage point on the strobe pulse leading edge, or the 90% voltage point on the strobe pulse trailing edge, for which the write control pulse must be in the LOW state ($t_{\ell W\phi LH} \geq 0$; $t_{\ell W\phi HL} \geq 400$ ns).
15. Write control-strobe pulse hold time: $t_{hW\phi}$
    The time after the strobe pulse has returned to LOW for which the write control pulse remain LOW ($t_{hW\phi} \geq 0$).

OUTPUT BUFFER DESCRIPTION

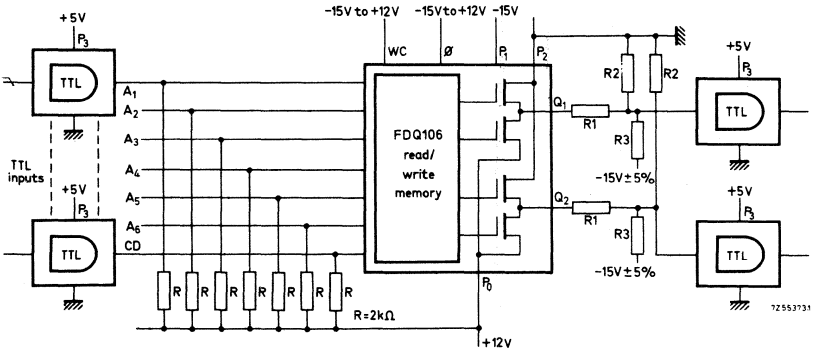
The output buffers used on the FDQ106 are identical to these used on the FDN106, FDN116, FDN126 and FDN136 dynamic shift registers. The V_Q versus I_Q characteristics shown in the data sheets for these shift registers also apply, therefore, to the FDQ106. The Vp supply voltage may be varied between 0 and −28 V according to the load requirements.

1. Biasing circuit A may be used to drive MOS loads.
   Normal MOS input signals must drive the address and other input signals in accordance with the specified electrical characteristics.



Biasing circuit A

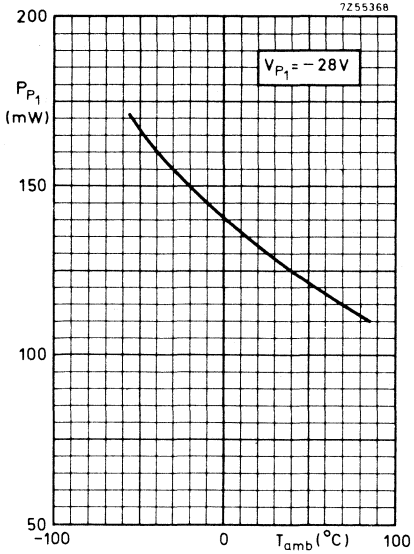
2. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both data inputs and data outputs. Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead, most of our FC gates [1]) and FJ gates [1]) satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V. ([1]) non-RC types)

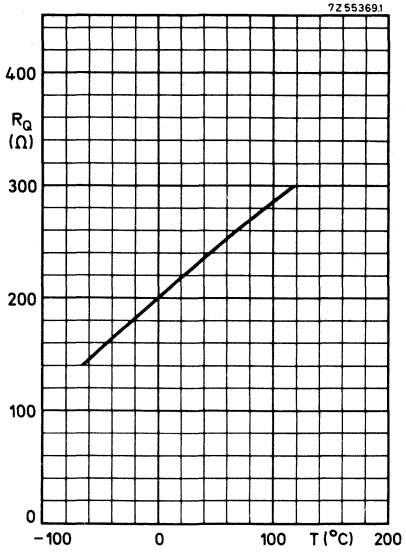


Fan-out = 1		Fan-out = 2	
R1 = 1.2 kΩ	M_H = 600 mV	R1 = 560 Ω	M_H = 450 mV
R2 = 1 kΩ	M_L = 750 mV	R2 = 1 kΩ	M_L = 500 mV
R3 = 10 kΩ	P_{HIGH} = 13 mW	R3 = 4.7 kΩ	P_{HIGH} = 41 mV

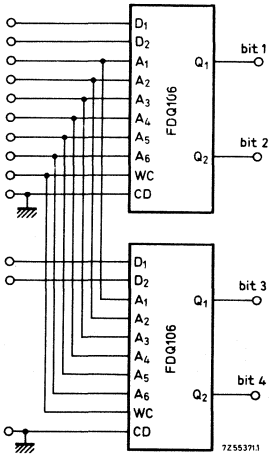
Biasing circuit B

TYPICAL PERFORMANCE

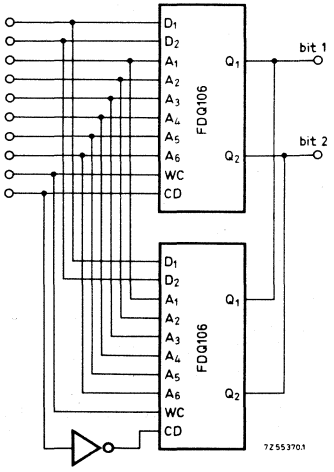




EXPANDED MEMORIES



64 word, 4 bits per wor



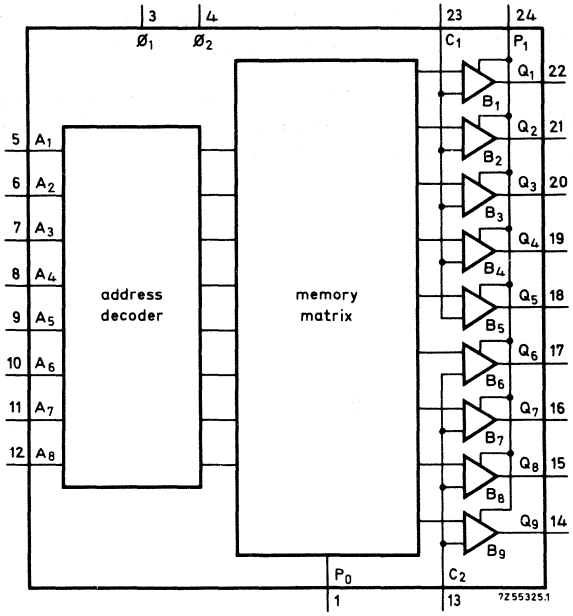
128 word, 2 bits per word

A LOW state at the chip **disable** input will cause both push-pull output buffers to turn off. In the off state, the output impedance of the output transistors becomes very high (approximately 5 MΩ) making it possible to use wired-or configurations with other FDQ106 outputs.

Chip disable also inhibits write, which allows common bussing of data input lines.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ ONLY MEMORY, 256 WORD, 9 BITS PER WORD



QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	1	μs
Clock rate	f_ϕ	max.	1	MHz
Power dissipation at f_ϕ = 1 MHz	P_ϕ	typ.	90	mw
D.C. noise margin	M_L, M_H	>	1	V
Operating ambient temperature	T_{amb}	-55 to +85		°C

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See General Section)

GENERAL DESCRIPTION

The FDR106Z is a monolithic 2304 bit read only memory. When ordering an FDR106Z the customer must send a bit pattern matrix (see example on pages 10 to 15) with the desired content. For performance evaluation, we can supply specimens of FDR106Z1, which is identical to the FDR106Z but contains a bit pattern of our own. The FDR106Z requires a two phase clock, but the outputs remain steady as long as the address remains unchanged. The normal configuration is as a 256 word, 9 bits per word, parallel output ROM. However, by means of two output inhibit controls it can be set up for 512 4-bit words.

The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134) ←

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to	−30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_1	$-I_{P1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE ←

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.01	–	1.0 MHz	
Clock pulse width	$t_{\phi 1L}$ $t_{\phi 2L}$	0.50 0.35	– –	5.0 μs 5.0 μs	see timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 μs	see note
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 μs	see note
Clock delay time	$t_{\phi 1\phi 2}$	0	–	45 μs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	45 μs	
Clock input voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−26	−24 V	
Adress input and output inhibit input logic levels:					
HIGH	V_{AH}, V_{CH}	−2	0	+0.3 V	
LOW	V_{AL}, V_{CL}	−28	−12	−9 V	

→ Note

At frequencies higher than 800 kHz, $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ will be determined by $t_{\phi LHmax}$ and $t_{\phi HLmax}$.

CHARACTERISTICS

Test conditions: V_{P1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 30 pF in parallel with 150 kΩ to P_0.

ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Output levels:						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Address input capacitance	C_A	–	3.2	4.0	pF	bias: V_A = 0 V; f_ϕ = 1 MHz
Output inhibit input capacitance	C_C	–	5.0	6.0	pF	bias: V_ϕ; V_C = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	–	15	17	pF	bias: V_ϕ; V_C = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	18	21	pF	bias: V_ϕ; V_C = 0 V; f_ϕ = 1 MHz
	$C_{\phi 1}$	–	8.1	10.5	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	11.2	14.5	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Output capacitance	C_Q	–	4.0	5.0	pF	bias: V_Q = 0 V; f_ϕ = 1 MHz
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	–	–	1	µA	$V_A = V_C$ = −15 V [1]
Clock input current	$-I_{\phi L}$	–	–	100	µA	V_ϕ = −28 V [1]
Output current	$-I_Q$	–	–	10	µA	V_Q = −10 V; $V_{C1} = V_{C2}$ = LOW; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	700	–	Ω	
LOW	R_{QL}	–	300	–	Ω	V_{P1} = −5 V
Clock power dissipation (see note 1)	$P_{\phi 1}$, $P_{\phi 2}$	–	36	–	mW	f_ϕ = 1 MHz
Input current (See note 2)	$-I_{P1}$	–	4.8	–	mA	V_{P1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	350	–	ns	
Delay times: fall time	t_{DHL}	–	20	–	ns	
rise time	t_{DLH}	–	20	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

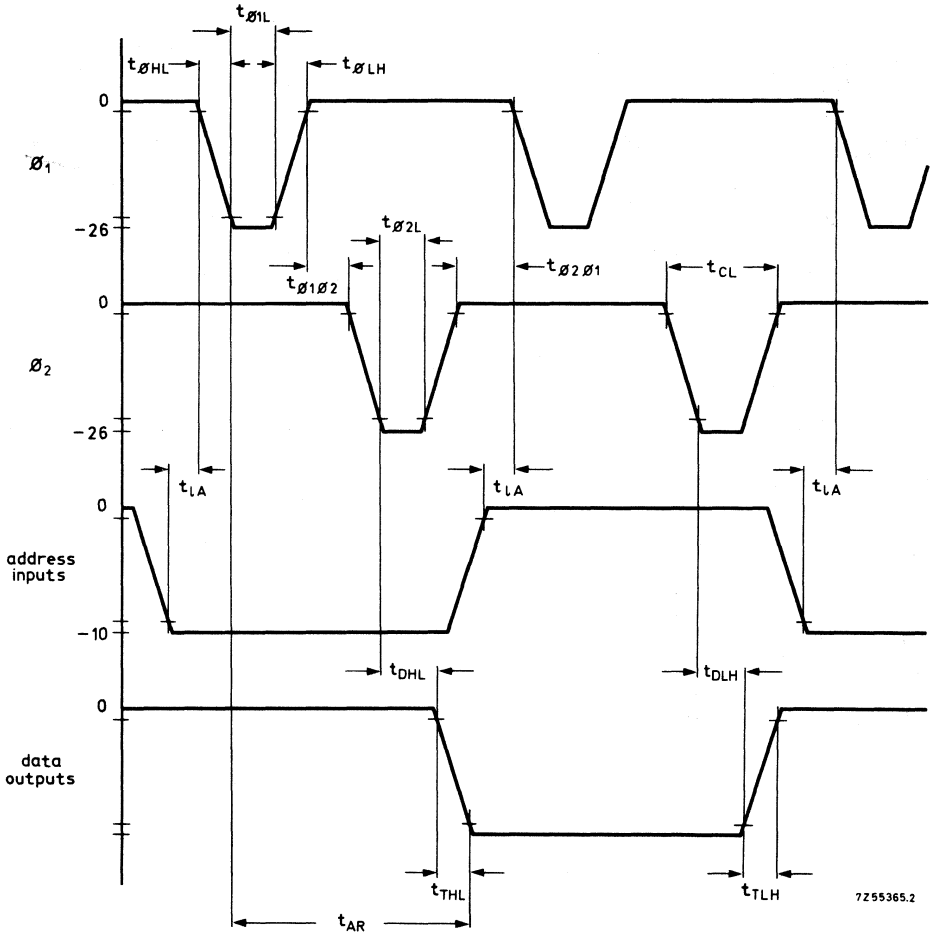
Note 1: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 2: I_{P1} is almost entirely dependent on the external load.

[1]) T_{amb} = 25 °C; all other terminals at V_{P0}.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit timing requirements:

1. Address input signals are clocked into the memory during ϕ_1, and must remain present throughout ϕ_1. Address lead time (t_{lA}) must be ≥ 0.
2. Output inhibit signals act without delay. If output signals are to be read during phase 1, output inhibit signals must be delayed with respect to their associated address until phase 2 (t_{CL}).
3. The output signals remain steady for as many clock cycles as the address and output inhibit signals remain unchanged.

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

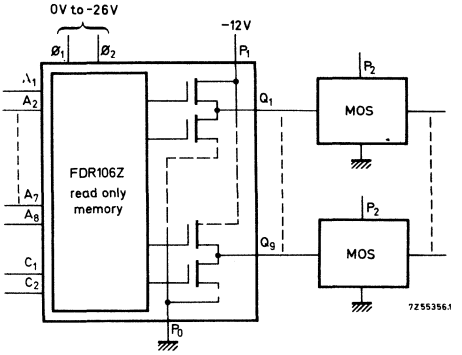
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_\phi \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Output inhibit time: t_{CL}
   The minimum time that the output inhibit signal must be present during ϕ_2 in order to inhibit the output, defined at -2 V.
10. Read access time: t_{AR}
    The time between the 90% point on the negative going edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

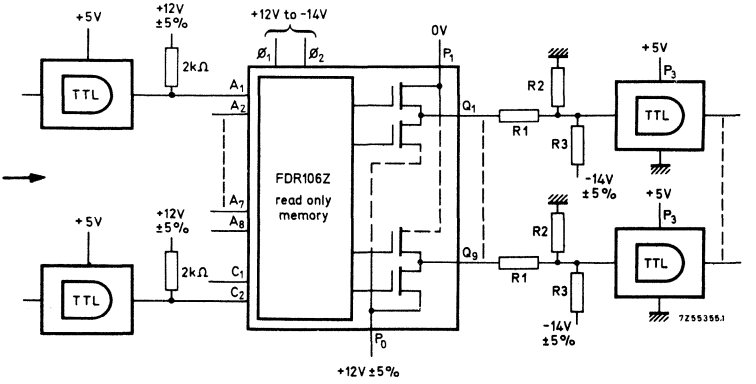
The only d.c. supply required is V_{P_1}, the push-pull output buffer supply. V_{P_1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

2. Biasing circuit B is used when driving TTL or DTL loads direct from each output buffer.
   Note the neither active nor passive interface components are required. The circuit assumes MOS input excursions from +5 V (V_{P0}) to ≤ 4 V.



R_1 = 910 Ω
R_2 = 1.8 kΩ
R_3 = 8.2 kΩ
all resistors: ± 5%
M_L = 600 mV
M_H = 460 mV
$P_{totHIGH}$ < 200 mW per output

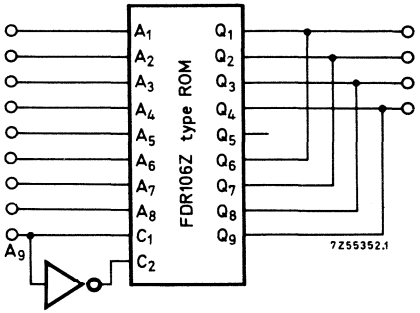
Biasing circuit B.

Note: The negative voltage is 26 V ± 5% below V_{P0}.

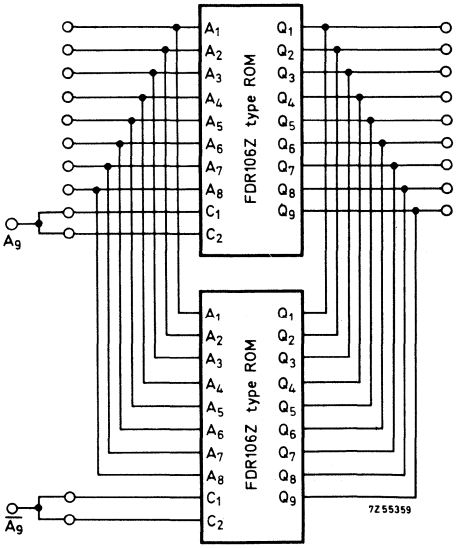
WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the **low impedance mode** [1]). C_1 controls output buffers 1 to 5, and C_2 controls output buffers 6 to 9. This output inhibit wired-or capability makes it possible to use the FDR106Z type ROM in many different applications, such as those shown here.
Note that the terminals A9 and $\overline{A9}$ although shown as address inputs, must actually be output inhibit signals synchronous with the addressed data word rather than the address.

ROM
512 word
4 bits



ROM
512 word
9 bits



[1]) Except for the effect of leakage current and capacitive load.

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Four forms are needed for 256 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customers's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS .
   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least sifnificant bit; the left-hand bit is bit 9, it is the most sinificant .The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.
   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
   c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1])
   Memories of 256 words need 4 pages, of specifications.
   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, as with 256 word memories, column 9 is unused and is, therefore, left blank.

[1]) See example on page 12.

2. CONTENTS (DATA OUTPUTS)

a) Each column has provision for words of 9 bits numbered 1 to 9, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.

b) The requisite bit pattern should be inserted under headings 1 to 9 using only ones (1 = LOW) and zeros (0 = HIGH).

3. AUTHORIZED SIGNATURE

Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern

FDR 106 Z...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

Note: 1 = LOW; 0 = HIGH

ADDRESS INPUTS 9 8 7 6 5 4 3 2 1	00 OUTPUTS 9 8 7 6 5 4 3 2 1	01 OUTPUTS 9 8 7 6 5 4 3 2 1	CONTENTS 10 OUTPUTS 9 8 7 6 5 4 3 2 1	11 OUTPUTS 9 8 7 6 5 4 3 2 1
	8 9 10 11 12 13 14 15 16	17 18 19 20 21 22 23 24 25	26 27 28 29 30 31 32 33 34	35 36 37 38 39 40 41 42 43
1 2 3 - - 4 5 6 7				
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

APPLICATIONS

The bit patterns stored in the FDR106Z1 allow this ROM to perform the following functions:

1. STARBURST ALPHA-NUMERIC CHARACTER GENERATION

Generation of activating signals for 64 17-segment starburst pattern character using an ASCII input code (128 words).

2. STARBURST PATTERN GENERATION

Generation of x and y deflection signal to produce a 22 stroke starburst pattern on a CRT (22 words).

3. SEVEN SEGMENT DECODE NUMERIC BLANKING CHARACTER GENERATOR (16 WORDS)

4. SELECTRIC TO ASCII CODE CONVERSION

Conversion of IBM selectric input/output writer keyboard code to ASCII code with even or odd parity (88 words).

PATTERN 1

STARBURST CHARACTER GENERATION

For a starburst character, 17 activating signals are used for the 17 segments of the pattern. Since only 9 output lines are available in the FDR106Z1, the complete bit pattern for each character must be stored in two 9-bit words; thus a total of 128 words are used for 64 characters. Fig. 1 shows the segments controlled by the output bits of the first (S) and second (T) word for each character. The S word contains 9 segment signals and the T word 8. The nineth bit of ROM T(T6) is not used. A logic 1 output signal (nominally −12 V) represents an activated (ON) segment signal. The starburst character generation function is selected by setting address bit A_8 to 0 V (V_{P_0} or HIGH signals). S words are selected by setting address bit A_5 to 0 V (HIGH) and T words by setting address bit A_5 to −10 V (LOW).
Address bits A_1, A_2, A_3, A_4, A_6 and A_7 are used to select any one of the characters. The input character code is a subset of the standard ASCII 7 bit code derived by using ASCII bits b_1, b_2, b_3, b_4, b_5 and b_7 according to the following table:

FDR106Z1 address input	ASCII bit
A_1	b_4
A_2	b_3
A_3	b_2
A_4	b_1
A_6	b_5
A_7	b_7

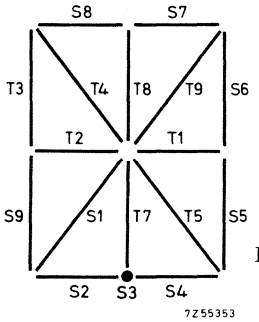


Fig. 1 Starburst pattern segments

PATTERN 1 (continued)

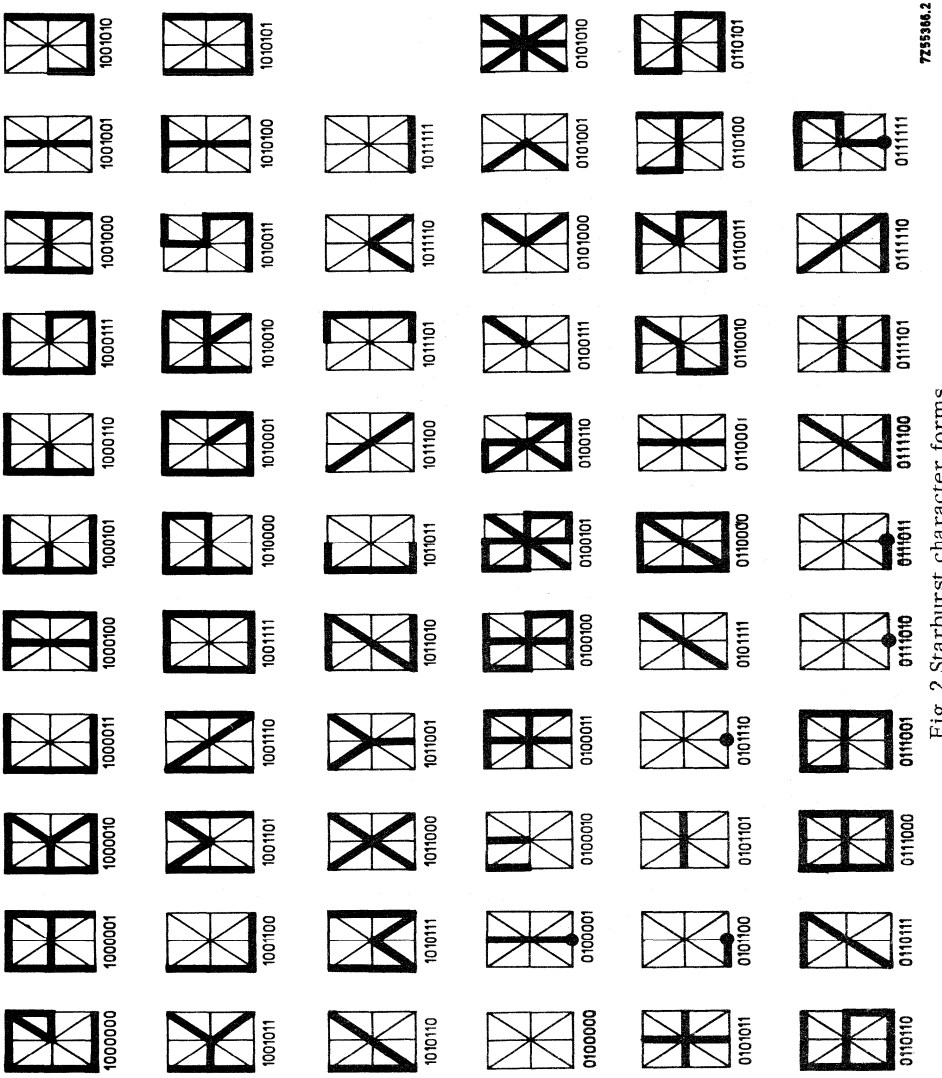


Fig. 2 Starburst character forms

→ **PATTERN** 1 (continued)

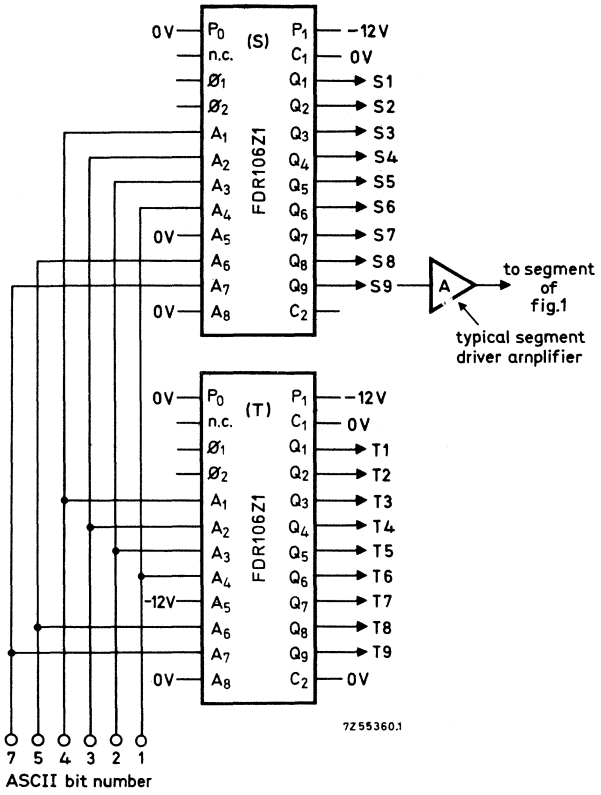


Fig. 3. Wiring diagram for segment activation of a 17 segment illuminated display

PATTERN 2

2.1 STARBURST STROKE PATTERNS GENERATION

In this configuration, the ROM is used to produce x and y deflection signals to generate the pattern of Fig. 4 on a CRT. For this purpose the FDR106Z1 is connected as shown in Fig. 5, with certain of the ROM outputs connected back to the address input lines [1]). Each word in this sequence contains (in addition to the x and y steering signal outputs for a CRT) the address of the next word of the group used for this function. One clock power is applied, the memory steps in turn to a next word of the group each clock period and will thus continuously cycle through the group, as shown in Fig. 6 where the address and contents (outputs) of each word are sequentially listed. The +x, −x, +y and −y signals are rate signals and must be integrated as shown in Figs. 7a, b and c to produce the x and y deflection signals for a CRT.

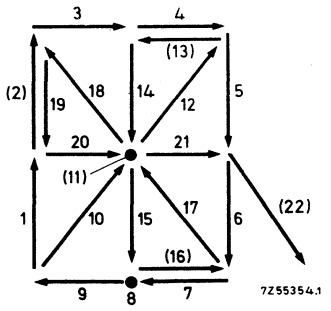


Fig. 4 Starburst stroke pattern

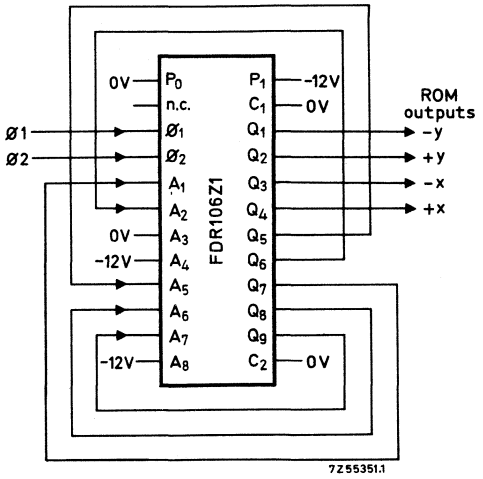


Fig. 5 Wiring diagram for starburst stroke pattern generator

[1]) In doing so, the ROM runs at the ϕ_1, ϕ_2 clock-rate through a sequence of 22 addresses.

PATTERN 2 (continued)

Address bits								Segment of Fig. 4	ROM contents								
														+x	−x	+y	−y
A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1		Q_9	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
1	1	1	1	1	0	1	1	1	0	0	1	1	1	0	0	1	0
1	0	0	1	1	0	1	1	2	0	1	0	1	1	0	0	1	0
1	0	1	1	1	0	1	0	3	0	0	0	1	1	1	0	0	0
1	0	0	1	1	0	1	0	4	0	1	1	0	1	1	0	0	0
1	0	1	1	1	0	0	1	5	0	0	1	0	1	0	0	0	1
1	0	0	1	1	0	0	1	6	0	1	0	0	1	0	0	0	1
1	0	1	1	1	0	0	0	7	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	0	8	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	9	0	0	1	0	0	0	1	0	0
1	0	0	0	1	0	0	1	10	0	1	1	0	0	1	0	1	0
1	0	1	0	1	0	0	1	11	0	1	1	1	1	0	0	0	0
1	0	1	1	1	0	1	1	12	1	0	1	1	1	1	0	1	0
1	1	0	1	1	0	1	1	13	1	1	0	1	1	0	1	0	0
1	1	1	1	1	0	1	0	14	1	0	0	1	1	0	0	0	1
1	1	0	1	1	0	1	0	15	1	1	1	0	1	0	0	0	1
1	1	1	1	1	0	0	1	16	1	0	1	0	1	1	0	0	0
1	1	0	1	1	0	0	1	17	1	1	0	0	1	0	1	1	0
1	1	1	1	1	0	0	0	18	1	0	0	0	1	0	1	1	0
1	1	0	1	1	0	0	0	19	1	0	0	0	0	0	0	0	1
1	1	0	0	1	0	0	0	20	1	0	1	0	0	1	0	0	0
1	1	0	0	1	0	0	1	21	1	1	1	0	0	1	0	0	0
1	1	1	0	1	0	0	1	22	1	1	1	1	1	1	0	0	1
1	1	1	1	1	0	1	1	1	0	0	1	1	1	0	0	1	0

Fig. 6 Starburst pattern sequence

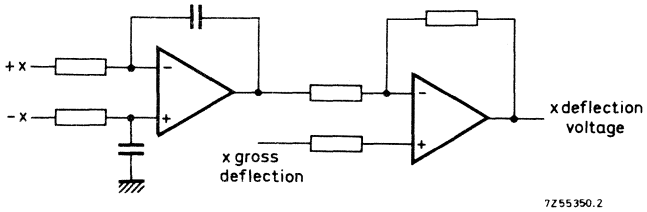


Fig. 7a x integrator circuit: identical circuit for y

Note: 1 = LOW; 0 = HIGH

PATTERN 2 (continued)

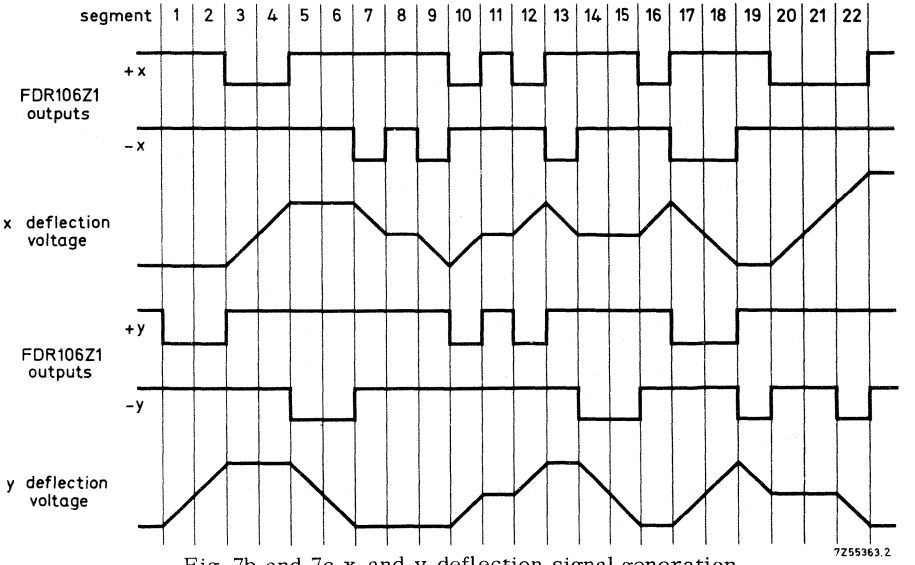


Fig. 7b and 7c x and y deflection signal generation

2.2 Generation of blanking signal

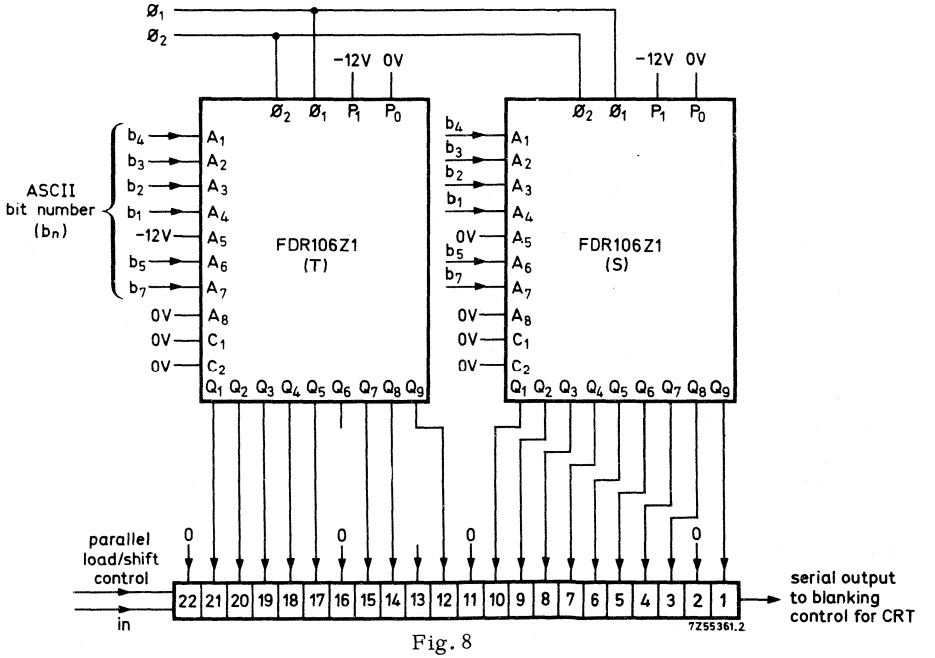


Fig. 8

→ **PATTERN** 3

SEVEN SEGMENT DECODE

This portion of the FDR106Z1 generates seven driver signals, a zero indicator signal, and an "over-nine" indicator signal for a seven segment display device. The input code is BCD augmented by special characters. The segment activation patterns are shown, together with the BCD code at the ROM inputs, in Fig.9.
Fig.10 is the connection diagram for seven segment function configuration.

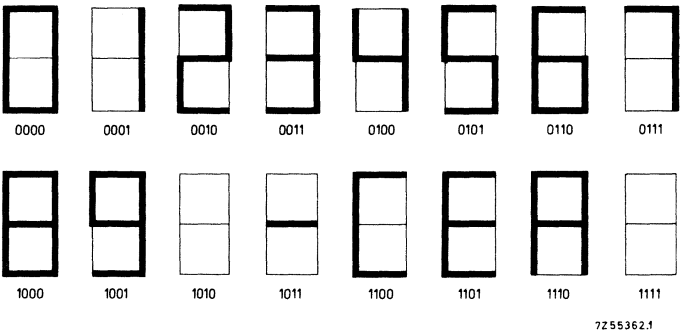


Fig. 9 Seven segment character forms and their binary input code (8421)

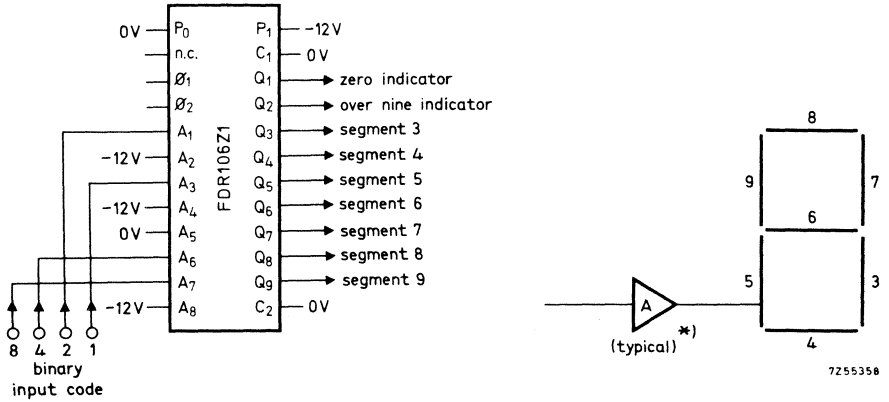


Fig. 10 Wiring diagram for a seven segment decode

*) Typical segment driver amplifier

PATTERN 4

SELECTRIC TO ASCII CODE CONVERTER

When used in the selectric to ASCII code converter configuration, the FDR106Z1 translates seven input line signals from a selectric input/output writer (correspondence model) to ASCII code with even or odd parity. Fig.11 shows the wiring connections for this function. The conncetion of selectric contacts is shown for a machine with standard wiring. Selectric keyboards provide six signal lines (R_1, R_2, R_{2A}, R_5, T_1 and T_2) and a parity line which is not used in this application. The keyboard shift contact provides the seventh input line (A_7) to the FDR106Z1 (upper case is LOW, lower case is HIGH). Fig.12 shows the selectric contact signals and FDR106Z1 address bits for which the code converter is patterned. The ASCII code for > is generated when the selectric ¢ key is depressed, and the code for < when the selectric ° (degrees) key is depressed.

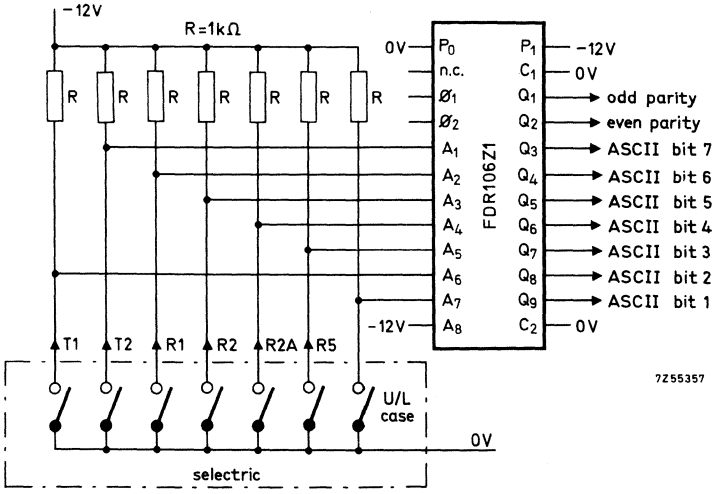


Fig. 11 Wiring diagram for selectric to ASCII code converter

SELECTRIC CODE

FDR106Z1 address bit selectric contact	A_7	A_6	A_1	A_2	A_3	A_4	A_5	FDR106Z1 address bit selectric contact	A_7	A_6	A_1	A_2	A_3	A_4	A_5
character	case							character	case						
A	U	0	1	1	1	0	0	W	U	0	1	1	1	1	1
a	L	0	1	1	1	0	0	w	L	0	1	1	1	1	1
B	U	1	0	1	1	1	1	X	U	1	0	0	0	0	0
b	L	1	0	1	1	1	1	x	L	1	0	0	0	0	0
C	U	1	0	1	1	0	0	Y	U	1	1	0	1	1	1
c	L	1	0	1	1	0	0	y	L	1	1	0	1	1	1
D	U	1	0	0	1	0	0	Z	U	0	0	0	0	0	1
d	L	1	0	0	1	0	0	z	L	0	0	0	0	0	1
E	U	1	0	0	1	0	1	(	U	0	0	0	0	0	0
e	L	1	0	0	1	0	1	)	L	0	0	0	0	0	0
F	U	1	1	1	0	0	0	@	U	0	0	1	0	0	1
f	L	1	1	1	0	0	0	2	L	0	0	1	0	0	1
G	U	1	1	0	0	0	0	#	U	0	0	1	0	0	0
g	L	1	1	0	0	0	0	3	L	0	0	1	0	0	0
H	U	1	0	0	1	1	1	$	U	0	0	0	1	1	0
h	L	1	0	0	1	1	1	4	L	0	0	0	1	1	0
I	U	0	1	1	1	0	1	%	U	0	0	0	1	0	1
i	L	0	1	1	1	0	1	5	L	0	0	0	1	0	1
J	U	1	1	0	0	0	1	¢	U	0	0	1	1	0	1
j	L	1	1	0	0	0	1	6	L	0	0	1	1	0	1
K	U	1	0	1	1	0	1	&	U	0	0	0	1	0	0
k	L	1	0	1	1	0	1	7	L	0	0	0	1	0	0
L	U	1	0	0	1	1	0	*	U	0	0	1	1	0	0
l	L	1	0	0	1	1	0	8	L	0	0	1	1	0	0
M	U	0	1	0	0	0	0	(	U	0	0	1	1	1	1
m	L	0	1	0	0	0	0	9	L	0	0	1	1	1	1
N	U	1	0	1	0	0	1	)	U	0	0	0	1	1	1
n	L	1	0	1	0	0	1	0	L	0	0	0	1	1	1
O	U	0	1	0	1	1	0	–	U	1	1	1	1	1	1
o	L	0	1	0	1	1	0	-	L	1	1	1	1	1	1
P	U	1	1	0	1	0	1	+	U	1	1	1	0	0	1
p	L	1	1	0	1	0	1	=	L	1	1	1	0	0	1
Q	U	1	1	1	1	0	1	°	U	0	1	0	0	0	1
q	L	1	1	1	1	0	1	!	L	0	1	0	0	0	1
R	U	0	1	0	1	0	0	:	U	1	1	0	1	0	0
r	L	0	1	0	1	0	0	;	L	1	1	0	1	0	0
S	U	0	1	0	1	1	1	"	U	0	1	0	1	0	1
s	L	0	1	0	1	1	1	,	L	0	1	0	1	0	1
T	U	1	0	0	0	0	1	'	U	1	1	1	1	0	0
t	L	1	0	0	0	0	1	'	L	1	1	1	1	0	0
U	U	1	0	1	0	0	0		U	0	1	1	0	0	1
u	L	1	0	1	0	0	0		L	0	1	1	0	0	1
V	U	0	1	1	0	0	0	?	U	1	1	0	1	1	0
v	L	0	1	1	0	0	0	/	L	1	1	0	1	1	0

Note: 1 = LOW; 0 = HIGH

COMPLETE FDR106Z1 BIT PATTERN

ADDRESS INPUTS		ROM CONTENTS			
		00	01	10	11
		outputs	outputs	outputs	outputs
	8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1
1	0 0 X X 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 0 1 1	1 0 0 0 0 0 1 0 0
2	0 0 X X 0 0 0 1	0 0 0 0 0 0 0 0 0	1 0 0 0 1 0 0 0 0	1 1 1 1 1 1 0 1 0	0 0 0 0 0 0 1 1 1
3	0 0 X X 0 0 1 0	0 1 1 0 1 1 0 1 0	0 1 1 0 0 0 1 1 1	0 0 0 1 1 0 0 0 0	0 0 0 0 0 0 1 1 1
4	0 0 X X 0 0 1 1	0 0 0 0 0 0 1 1 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 1 1	1 0 0 0 0 0 0 0 0
5	0 0 X X 0 1 0 0	0 0 0 1 0 0 0 0 0	0 1 0 0 0 0 0 0 0	1 1 1 0 0 1 0 1 0	1 0 0 0 0 0 0 1 0
6	0 0 X X 0 1 0 1	0 0 0 0 0 0 0 0 1	1 1 1 0 1 1 0 1 1	0 0 0 0 0 0 1 0 0	0 0 0 0 0 0 0 0 0
7	0 0 X X 0 1 1 0	0 1 0 0 1 1 0 1 1	0 1 0 0 1 1 0 0 0	1 1 1 0 1 1 0 1 0	0 0 0 0 0 0 1 1 1
8	0 0 X X 0 1 1 1	0 0 0 0 0 0 1 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 1 0	0 0 0 0 1 1 0 0 0
9	0 0 X X 1 0 0 0	0 0 0 0 0 0 1 0 0	0 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0
10	0 0 X X 1 0 0 1	0 0 0 0 0 0 0 0 1	0 0 0 0 0 1 0 0 0	0 1 1 1 1 1 0 1 0	0 0 0 0 0 0 1 1 1
11	0 0 X X 1 0 1 0	0 1 0 0 1 1 0 0 1	1 1 1 0 0 0 1 1 1	0 1 1 0 1 1 0 1 0	0 0 0 0 0 0 1 1 1
12	0 0 X X 1 0 1 1	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 1	0 0 0 0 0 1 0 1 0	0 0 0 0 0 0 0 1 1
13	0 0 X X 1 1 0 0	0 1 1 1 1 0 0 0 0	0 1 1 0 0 0 0 1 1	0 1 1 0 1 1 0 1 0	1 0 0 0 0 0 0 0 1
14	0 0 X X 1 1 0 1	0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 1 1	0 0 0 0 0 0 1 1 0	0 0 0 0 0 0 0 0 0
15	0 0 X X 1 1 1 0	0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0
16	0 0 X X 1 1 1 1	0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0	0 1 1 1 0 0 1 0 0	0 0 1 0 0 0 0 0 1

Note: 1 = LOW; 0 = HIGH

COMPLETE FDR106Z1 BIT PATTERN

ADDRESS INPUTS		ROM CONTENTS			
	8 7 6 5 4 3 2 1 (6 5 = 00)	00 outputs 9 8 7 6 5 4 3 2 1	01 outputs 9 8 7 6 5 4 3 2 1	10 outputs 9 8 7 6 5 4 3 2 1	11 outputs 9 8 7 6 5 4 3 2 1
17	0 1 X X 0 0 0 0	1 1 1 1 0 1 0 1 0	1 0 0 0 0 0 1 0 1	1 1 1 1 0 0 0 0 0	0 0 0 0 0 0 1 1 1
18	0 1 X X 0 0 0 1	1 0 0 1 1 0 0 0 0	0 0 0 0 0 0 1 1 1	0 0 0 0 0 0 0 0 1	1 0 0 0 1 1 0 0 0
19	0 1 X X 0 0 1 0	0 1 1 1 1 1 0 1 0	0 1 1 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0
20	0 1 X X 0 0 1 1	1 0 0 0 0 1 0 1 0	0 0 0 0 0 0 1 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 1 1 0 0 0
21	0 1 X X 0 1 0 0	1 1 1 0 0 1 0 1 0	1 0 0 0 1 0 1 1 0	1 1 1 1 0 0 0 0 0	0 0 0 0 1 0 1 1 1
22	0 1 X X 0 1 0 1	1 0 0 1 1 1 0 1 0	0 0 0 0 0 0 0 0 0	0 1 1 0 0 1 0 1 1	1 0 0 0 0 0 0 0 0
23	0 1 X X 0 1 1 0	1 1 1 0 0 0 0 0 0	0 0 0 0 0 0 1 1 0	1 0 0 0 0 0 0 0 1	1 0 0 0 0 0 1 0 0
24	0 1 X X 0 1 1 1	1 0 0 1 1 0 0 0 0	0 0 0 0 1 1 1 0 0	0 0 0 0 0 0 0 0 1	0 0 0 0 1 0 0 0 0
25	0 1 X X 1 0 0 0	1 1 1 1 1 0 0 0 0	0 0 0 0 0 0 1 1 1	1 1 1 1 1 1 0 1 0	0 0 0 0 1 0 1 0 0
26	0 1 X X 1 0 0 1	0 0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	1 0 1 0 0 1 0 0 0
27	0 1 X X 1 0 1 0	1 1 1 0 0 1 0 1 0	0 0 0 0 0 0 1 1 0	1 0 0 1 1 1 0 1 0	0 0 0 0 0 0 1 0 0
28	0 1 X X 1 0 1 1	1 0 0 1 1 0 0 0 0	1 0 0 0 0 1 1 0 0	0 1 0 0 0 0 0 1 0	0 1 1 0 0 0 0 0 0
29	0 1 X X 1 1 0 0	1 1 1 0 0 1 0 1 0	0 0 0 0 0 0 1 0 0	0 0 1 0 1 1 0 1 0	0 1 0 0 0 0 0 0 1
30	0 1 X X 1 1 0 1	1 0 0 0 0 0 0 0 0	1 0 0 0 1 0 1 1 0	0 0 1 0 0 1 0 0 0	0 1 1 0 0 0 0 0 0
31	0 1 X X 1 1 1 0	1 1 1 0 1 1 0 1 0	0 0 0 0 0 0 1 0 1	1 0 0 1 1 0 0 0 1	0 0 0 0 1 0 1 0 0
32	0 1 X X 1 1 1 1	1 1 1 1 1 1 0 1 0	0 0 0 0 0 0 1 0 0	0 0 0 0 0 1 0 1 0	0 0 0 0 0 0 0 0 0

Note: 1 = LOW; 0 = HIGH

COMPLETE FDR106Z1 BIT PATTERN (continued)

ADDRESS INPUTS		ROM CONTENTS			
		00 outputs	01 outputs	10 outputs	11 outputs
	8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1
33	1 0 X X 0 0 0 0	1 0 1 1 1 0 1 1 0	0 1 0 1 1 1 1 1 0	0 0 0 1 1 1 1 0 1	0 0 1 0 1 1 1 0 1
34	1 0 X X 0 0 0 1	1 0 1 1 0 1 1 1 0	1 0 0 0 0 1 0 0 1	1 1 1 0 0 1 1 1 0	0 1 0 1 0 1 1 0 1
35	1 0 X X 0 0 1 0	1 1 0 0 1 1 0 0 1	0 1 0 0 1 1 0 1 0	1 0 1 0 1 1 1 1 0	0 1 1 1 0 1 1 1 0
36	1 0 X X 0 0 1 1	0 1 1 0 1 1 1 1 0	0 1 1 1 0 1 0 0 1	0 1 1 0 0 1 1 0 1	1 0 1 1 1 1 0 1 0
37	1 0 X X 0 1 0 0	1 1 1 0 1 1 0 1 0	1 0 1 0 1 1 0 0 1	0 0 1 0 0 1 1 1 0	1 0 1 0 0 1 1 0 1
38	1 0 X X 0 1 0 1	0 1 0 0 1 1 1 0 1	1 1 1 0 0 1 0 0 1	1 1 0 1 1 1 0 1 0	0 0 0 0 1 1 1 1 0
39	1 0 X X 0 1 1 0	0 0 0 1 1 1 0 1 0	0 1 1 0 1 1 0 0 1	1 1 0 0 0 1 1 0 1	1 1 0 1 0 1 1 1 0
40	1 0 X X 0 1 1 1	1 0 0 0 0 1 1 1 0	1 0 0 1 0 1 1 0 1	0 0 1 1 0 1 0 1 0	1 0 0 0 1 1 1 0 1
41	1 0 X X 1 0 0 0	0 0 1 0 0 0 1 0 0	0 0 0 0 0 0 0 0 0	1 0 1 1 0 0 0 1 0	0 0 0 0 1 0 1 0 0
42	1 0 X X 1 0 0 1	0 1 1 0 0 1 0 1 0	0 1 0 0 1 0 0 0 1	0 1 1 1 1 0 0 0 0	0 0 1 0 1 0 0 0 1
43	1 0 X X 1 0 1 0	1 1 1 0 1 1 1 0 1	0 1 1 0 1 1 0 0 0	1 0 1 1 0 0 1 0 0	0 0 0 1 1 1 0 0 0
44	1 0 X X 1 0 1 1	0 1 1 1 1 1 0 0 0	0 1 0 1 1 0 0 1 0	1 1 0 1 1 1 1 0 0	1 0 1 1 1 1 0 1 0
45	1 0 X X 1 1 0 0	0 0 1 0 1 1 0 1 0	0 0 0 0 1 1 0 0 1	0 0 1 1 0 1 1 0 1	0 0 0 1 0 1 1 1 0
46	1 0 X X 1 1 0 1	1 1 1 1 0 1 1 0 1	1 1 0 0 1 1 1 1 0	1 1 1 1 0 1 0 1 0	1 0 0 1 1 1 1 1 0
47	1 0 X X 1 1 1 0	0 0 1 0 0 0 1 0 0	1 0 0 1 1 1 0 0 1	1 1 0 1 0 1 1 0 0	0 1 0 0 0 1 1 1 0
48	1 0 X X 1 1 1 1	0 1 1 1 0 1 1 0 0	1 1 1 0 1 1 1 0 1	0 1 1 0 0 0 1 0 0	1 0 1 1 0 1 0 0 1

Note: 1 = LOW; 0 = HIGH

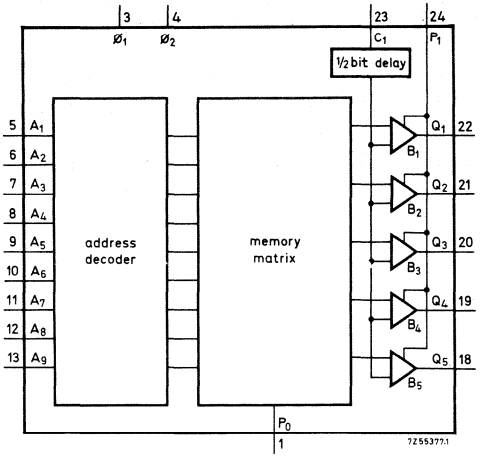
COMPLETE FDR106Z1 BIT PATTERN (continued)

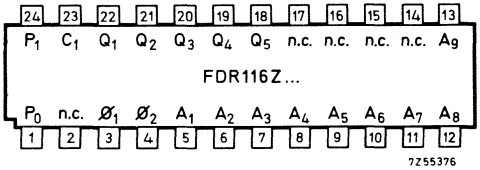
ADDRESS INPUTS		ROM CONTENTS			
		00 outputs	01 outputs	10 outputs	11 outputs
	8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1	9 8 7 6 5 4 3 2 1
49	1 1 X X 0 0 0 0	1 1 0 1 1 0 1 1 0	0 1 0 1 1 0 1 0 1	0 0 0 1 1 0 1 1 0	0 0 1 0 1 0 1 1 0
50	1 1 X X 0 0 0 1	1 0 1 1 0 0 1 0 1	0 0 1 1 1 1 0 0 1	1 1 1 0 0 0 1 0 1	0 1 0 1 0 0 1 1 0
51	1 1 X X 0 0 1 0	1 1 0 0 0 1 0 1 0	0 0 0 0 0 0 1 1 0	1 0 1 0 1 0 1 0 1	0 1 1 1 0 0 1 0 1
52	1 1 X X 0 0 1 1	0 1 1 0 1 0 1 0 1	0 1 1 1 0 1 0 0 1	0 1 1 0 0 0 1 1 0	1 1 0 1 0 1 0 0 1
53	1 1 X X 0 1 0 0	0 1 1 0 0 1 0 1 0	1 0 1 0 0 1 0 1 0	0 0 1 0 0 0 1 0 1	1 0 1 0 0 0 1 1 0
54	1 1 X X 0 1 0 1	0 1 0 0 1 0 1 1 0	0 1 0 0 0 1 0 0 1	0 1 0 1 1 1 0 0 1	0 0 0 0 1 0 1 0 1
55	1 1 X X 0 1 1 0	0 1 0 1 0 1 0 1 0	0 1 1 1 1 1 0 1 0	1 1 0 0 0 0 1 1 0	1 1 0 1 0 0 1 0 1
56	1 1 X X 0 1 1 1	1 0 0 0 0 0 0 1 0 1	1 0 0 1 0 0 1 1 0	0 0 1 1 0 1 0 1 0	1 0 0 0 1 0 1 1 0
57	1 1 X X 1 0 0 0	1 0 1 0 0 1 0 0 0	1 0 0 0 0 0 0 0 1	1 0 1 1 0 0 0 1 0	1 0 0 0 1 0 1 1 0
58	1 1 X X 1 0 0 1	1 1 1 0 0 1 0 0 0	1 1 0 0 1 0 1 1 0	1 1 1 1 1 1 0 0 1	1 0 1 0 1 1 0 0 0
59	1 1 X X 1 0 1 0	1 1 1 1 1 1 1 0 0	1 1 1 0 1 0 0 0 1	1 1 0 0 1 1 0 1 0	1 0 0 1 1 0 0 0 1
60	1 1 X X 1 0 1 1	0 0 0 0 0 0 0 1 1	1 1 0 1 1 0 1 0 0	1 1 1 1 1 0 1 1 0	0 0 1 1 1 0 0 1 0
61	1 1 X X 1 1 0 0	0 0 1 0 0 1 0 0 1	1 0 0 1 0 1 0 1 0	0 0 1 1 0 0 1 1 0	0 0 0 1 0 0 1 0 1
62	1 1 X X 1 1 0 1	1 1 1 1 0 0 1 1 0	1 1 0 0 1 0 1 0 1	1 1 1 1 1 1 0 0 1	1 0 0 1 1 0 1 0 1
63	1 1 X X 1 1 1 0	1 1 1 1 0 1 1 0 0	0 0 0 1 0 1 0 0 1	1 1 0 1 1 1 0 1 0	0 1 0 0 0 0 1 0 1
64	1 1 X X 1 1 1 1	0 0 0 1 0 0 0 1 0	1 1 1 0 1 0 1 1 0	0 0 0 0 0 0 0 1 0	1 1 1 1 1 0 1 0 1

Note: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ-ONLY MEMORY, 512 WORD, 5 BITS PER WORD





QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	850	ns
Clock rate	f_ϕ	max.	1.2	MHz
Power dissipation at f_ϕ = 1 MHz	P_ϕ	typ.	90	mw
D.C. noise margin	M_L, M_H	>	1	V
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR116Z is a monolithic 2560 bit read only memory. When ordering an FDR116Z the customer must send a bit pattern matrix with the desired content. For performance evaluation, we can supply specimens of FDR116Z1, which is identical to the FDR116Z but contains a bit pattern of our own. The FDR116Z requires a two phase clock, but the outputs remain steady as long as the address remains unchanged. The normal configuration is as a 512,word, 5 bits per word, parallel output ROM. An output inhibit control allows the use of multiple FDR116Z in a wired-OR configuration.

The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.

The patterns permanently stored in the memory matrix of the FDR116Z1 are described in the following data sheets.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134) ←

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to	−30	V
Power dissipation up to $T_{amb} = 25\,^{o}C$	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	^{o}C
Storage temperature	T_{stg}	−65 to	+150	^{o}C
Total current through terminal P_2	$-I_{P_2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	$^{o}C/W$

CHARACTERISTICS at T_{amb} = −55 to +85 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.1	–	1.2 MHz	see note
Clock pulse width	$t_{\phi 1L}$ $t_{\phi 2L}$	0.50 0.25	– –	1.0 μs 1.0 μs	see timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 μs	see note
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 μs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	4.5 μs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	4.5 μs	
Clock input voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−26	−24 V	
Address input and output inhibit input logic levels:					
HIGH	V_{AH}, V_{CH}	−2	0	+0.3 V	
LOW	V_{AL}, V_{CL}	−14	−12	−9 V	

→ Note

At frequencies higher than 870 kHz, $t_{\phi 1Lmax}$ and $t_{\phi 2Lmin}$ will be determined by $t_{\phi LHmax}$ and $t_{\phi HLmax}$.

CHARACTERISTICS

Test conditions: V_{P_1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; **standard load: 30 pF in parallel with 150 kΩ to P_0.**

ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	–	750	850	ns	see note 1
Output levels:						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Address input capacitance	C_A	–	3.2	4.0	pF	bias: V_A = 0 V; f_ϕ = 1 MHz
Output inhibit input capacitance	C_C	–	3.2	4.0	pF	bias: V_C; V_ϕ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	–	21	30	pF	bias: V_C; V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	13	18	pF	bias: V_C; V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 1}$	–	13	18	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	7.4	10	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	–	–	1	μA	V_A = V_C = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	300	–	Ω	
LOW	R_{QL}	–	170	–	Ω	V_{P_1} = −5 V
Clock power dissipation (see note 2)	P_ϕ	–	36	–	mW	f_ϕ = 1 MHz
Input current (see note 3)	$-I_{P_1}$	–	4.0	–	mA	V_{P_1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: fall time	t_{DHL}	–	20	–	ns	
rise time	t_{DLH}	–	20	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

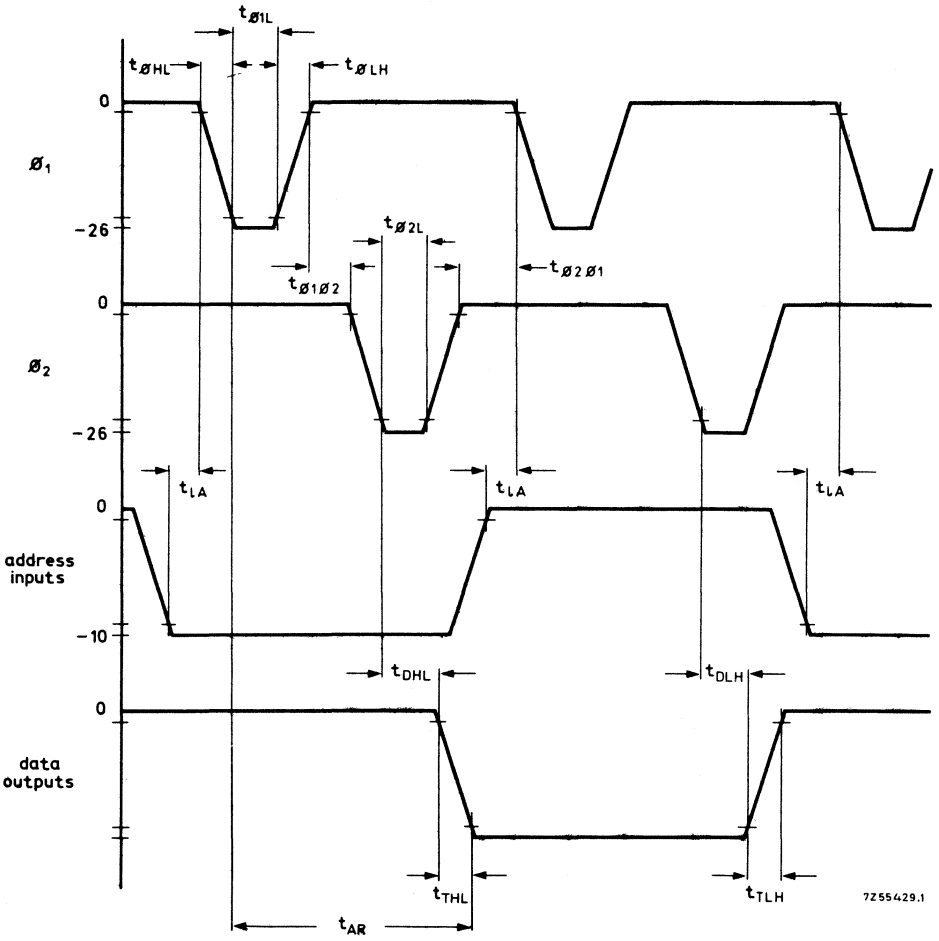
Note 1: The minimum access time assumes the summation of the rise time of ϕ_1 and the fall time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P_1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

The indicated points on the vertical axis are specified in the glossary of terms.

Address and output inhibit timing requirements:

1. Address input (and output inhibit input) signals are clocked into the memory during ϕ_1, and must remain present throughout ϕ_1. Address lead time ($t_{\ell A}$) must be ≥ 0.
2. The output signals remain steady **for as many clock cycles as the address and output** inhibit signals remain unchanged.

CHARACTERISTICS (continued)

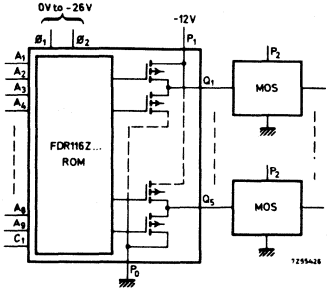
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_\phi \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$; $t_{\phi 2\phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read access time: t_{AR}
   The time between the 90% point on the negative going edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

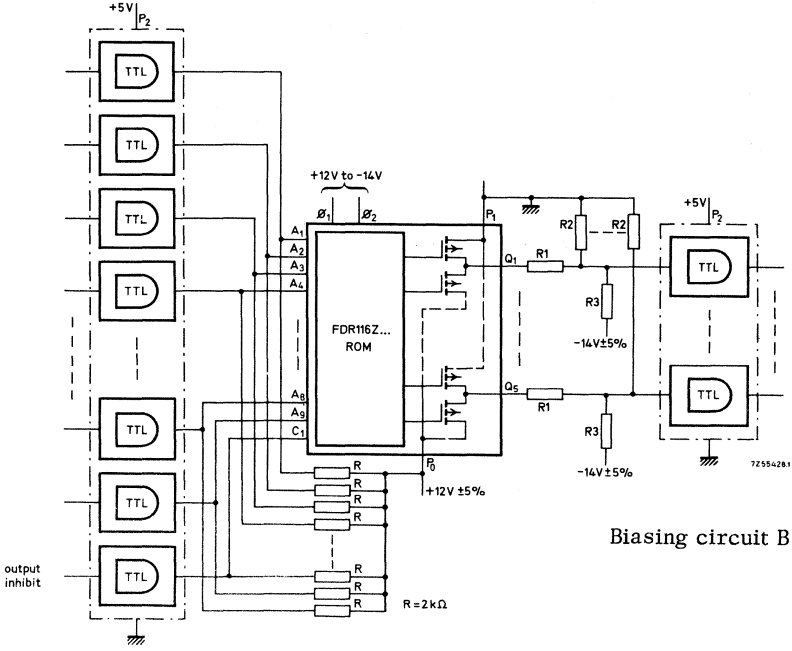
The only d.c. supply required is V_{P_1}, the push-pull output buffer supply. V_{P_1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A.

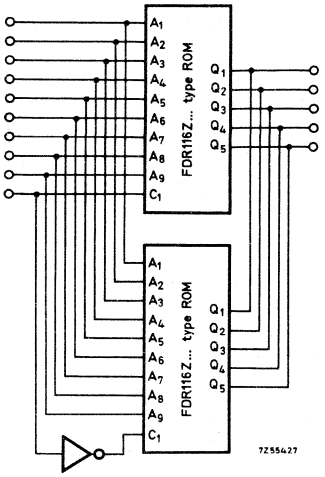
2. Biasing circuit B may be used to interface with TTL, both at the input and the output of the ROM. Note that no active interface devices are required. At the address and C inputs any TTL devices can be used that will sustain a minimum of +12 V at their output terminals.



Biasing circuit B.

WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-OR with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-OR capability makes it possible to use the FDR116Z type ROM in many different applications, such as the one shown here.



1024 words, 5 bits per word ROM

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customers's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS

a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.

b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.

c) Bit 7, 8 and 9 specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1])
Memories of 512 words need 8 pages, of specifications.

d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form.

1) See example on page 12

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN (continued)

2. CONTENTS (DATA OUTPUTS)

   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 5 using only ones (1 = LOW) and zeros (0 = HIGH).

3. AUTHORIZED SIGNATURE

   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

CHARACTER GENERATION

The FDR116Z1 is meant for generating ASCII characters for display in a system in which each character is made up of seven 5-bit rows that are traced one at a time. It is capable of storing 64 different characters, each having its own 6-bit address.

To generate a line of characters for display, word addresses are applied in sequence to the WORD SELECT inputs A_1 to A_3 and character addresses to the CHARACTER SELECT inputs A_4 to A_9. First, the row to be traced is selected by applying its address (3 bits) to inputs A_1 to A_3; then the desired characters are selected by applying their addresses (6 bits each) to inputs A_4 to A_9. When one row in a line of characters has been traced, the next row is generated by applying a new word address (inputs A_1 to A_3) and repeating the same sequence of character addresses as before. After the sequence of character addresses has been repeated in conjunction with the word addresses for all seven rows, the full line of characters has been generated. Of the FDR116Z1, a selection is available, which has a maximum read rating of 1.67 MHz (cycle time 600 ns).

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern

FDR 116 ...

page of

AUTHORIZED SIGNATURE

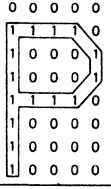
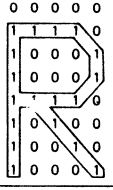
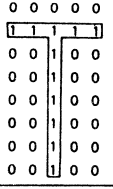
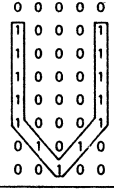
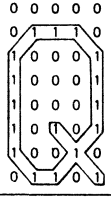
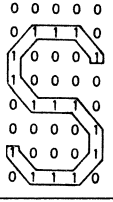
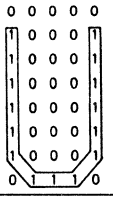
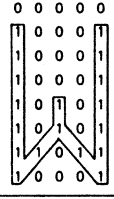
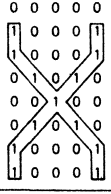
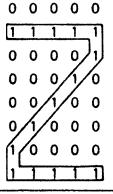
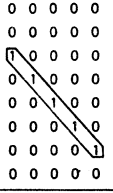
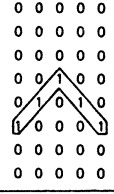
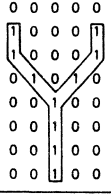
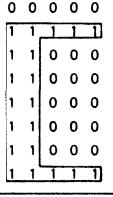
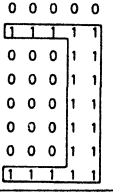
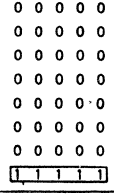
CUSTOMER NAME:

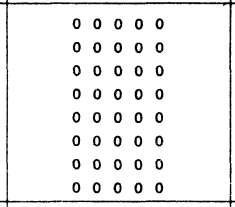
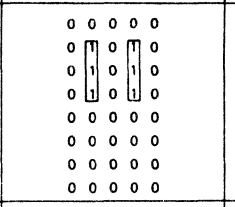
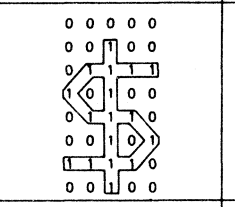
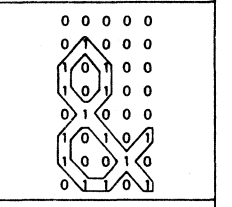
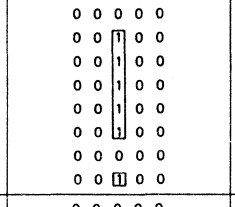
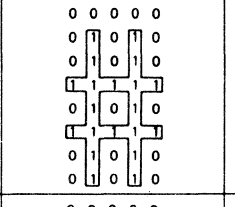
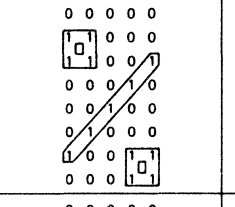
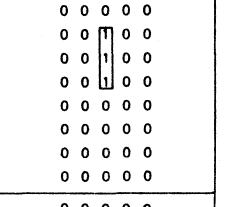
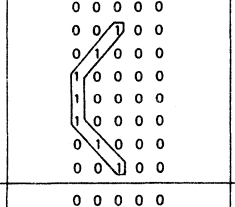
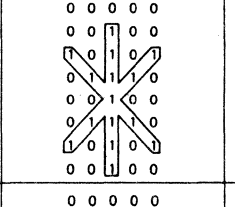
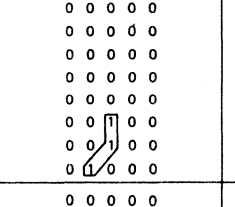
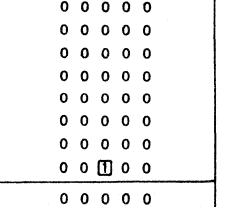
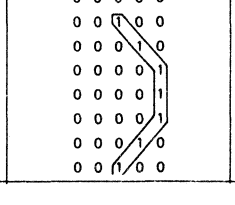
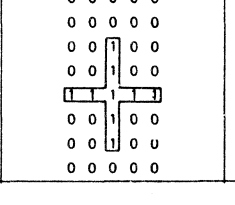
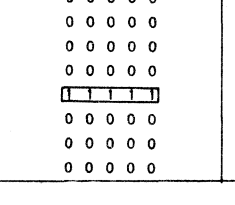
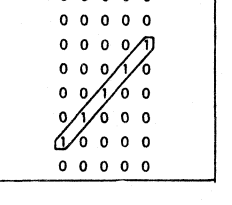
DATE

Note: 1 = LOW; 0 = HIGH

ADDRESS INPUTS 9 8 7 6 5 4 3 2 1	CONTENTS 00 OUTPUTS 10 9 8 7 6 5 4 3 2 1	01 OUTPUTS 10 9 8 7 6 5 4 3 2 1	10 OUTPUTS 10 9 8 7 6 5 4 3 2 1	11 OUTPUTS 10 9 8 7 6 5 4 3 2 1
	1 2 3 - - 4 5 6 7	8 9 10 11 12 13 14 15 16 17	18 19 20 21 22 23 24 25 26 27	28 29 30 31 32 33 34 35 36 37	38 39 40 41 42 43 44 45 46 47
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A9 A8 A7 A6 A5 A4	A3 A2 A1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
	↓	00	01	10	11
0 0 0 X X 0	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				
0 0 0 X X 1	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				
0 0 1 X X 0	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				
0 0 1 X X 1	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				

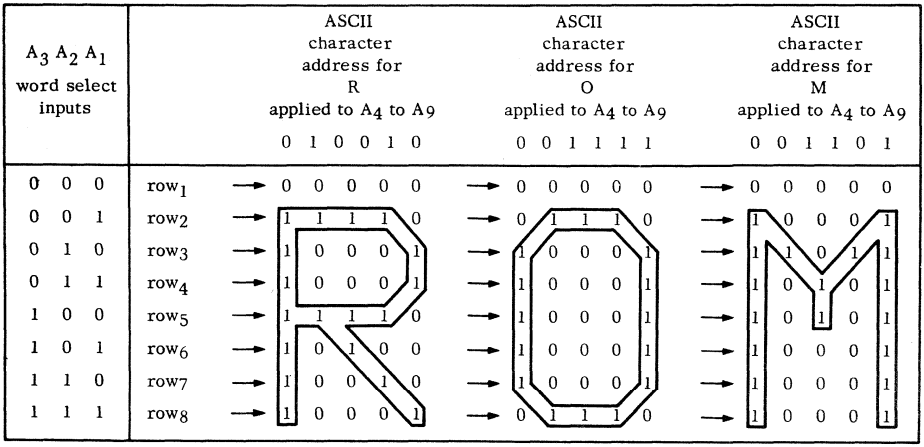
ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A9 A8 A7 A6 A5 A4	A3 A2 A1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
X X		00	01	10	11
0 1 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
$A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$
X X		00	01	10	11
1 0 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A9 A8 A7 A6 A5 A4	A3 A2 A1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
		00	01	10	11
1 1 0 X X 0	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				
1 1 0 X X 1	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				
1 1 1 X X 0	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				
1 1 1 X X 1	0 0 0				
	0 0 1				
	0 1 0				
	0 1 1				
	1 0 0				
	1 0 1				
	1 1 0				
	1 1 1				

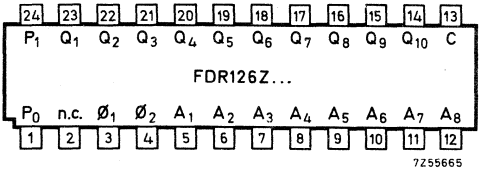
ROM ORGANISATION

In this example, with the word select input address fixed, the ASCII character addresses are sequentially altered to produce one line of three different characters, left to right. After 8 sequential binary word select iterations using the same character address sequence, the complete line of characters is formed, including a SPACE line.



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

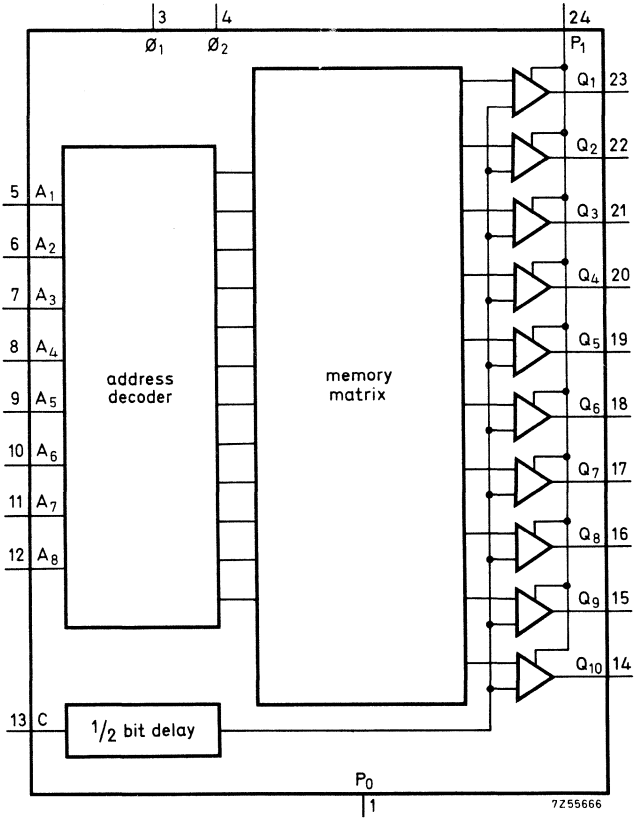
READ ONLY MEMORY, 256 WORD, 10 BITS PER WORD



P_0 and metal package bottom are connected.

QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	1	µs
Clock rate	f_ϕ	0.1 to	1	MHz
Power dissipation at f_ϕ = 1 MHz	P_{av}	typ.	100	mw
D.C. noise margin	M_H, M_L	>	1.0	V
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See General Section)


3
4
24
Ø1
Ø2
P1
Q1 23
Q2 22
Q3 21
Q4 20
Q5 19
Q6 18
Q7 17
Q8 16
Q9 15
Q10 14
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 A8
address decoder
memory matrix
13 C
1/2 bit delay
P0
1
7Z55666

GENERAL DESCRIPTION

The FDR126Z is a monolithic 2560 bit read only memory. When ordering an FDR126Z the customer must send a bit pattern matrix (see example on pages 12, 14 to 17) with the desired content. For performance evaluation, we can supply specimens of FDR126Z1, which is identical to the FDR126Z but contains a bit pattern of our own. The FDR126Z requires a two phase clock; the outputs remain steady as long as the address remains unchanged.
The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.
The FDR126Z1 is a pre-programmed version of the FDR126Z READ-ONLY memory. It is intended to convert from ASCII to SELECTRIC line code and vice versa.
When 7-bit address of either code is applied to the inputs of the ROM, the corresponding 7-bits of the other code will appear at the outputs.
The three remaining outputs are used for parity and control code indications.
The electrical characteristics of the FDR126Z1 are equal to those of the FDR126Z.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to	−30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_1	$-I_{P_1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	°C/W

Note
All terminals are protected against over-voltage caused by static charges.

CHARACTERISTICS at T_{amb} = −55 to +85 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	1.0	MHz	
Clock pulse width	$t_{\phi 1L}$ $t_{\phi 2L}$	0.60 0.25	– –	5.0 5.0	µs µs	see timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10	µs	
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10	µs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	45	µs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	45	µs	
Clock input voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Address input and output inhibit input logic levels:						
HIGH	V_{AH}, V_{CH}	−2	0	+0.3	V	
LOW	V_{AL}, V_{CL}	−28	−12	−9	V	

CHARACTERISTICS (continued)

Test conditions: V_{P1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 30 pF in parallel with 150 kΩ to P_0.

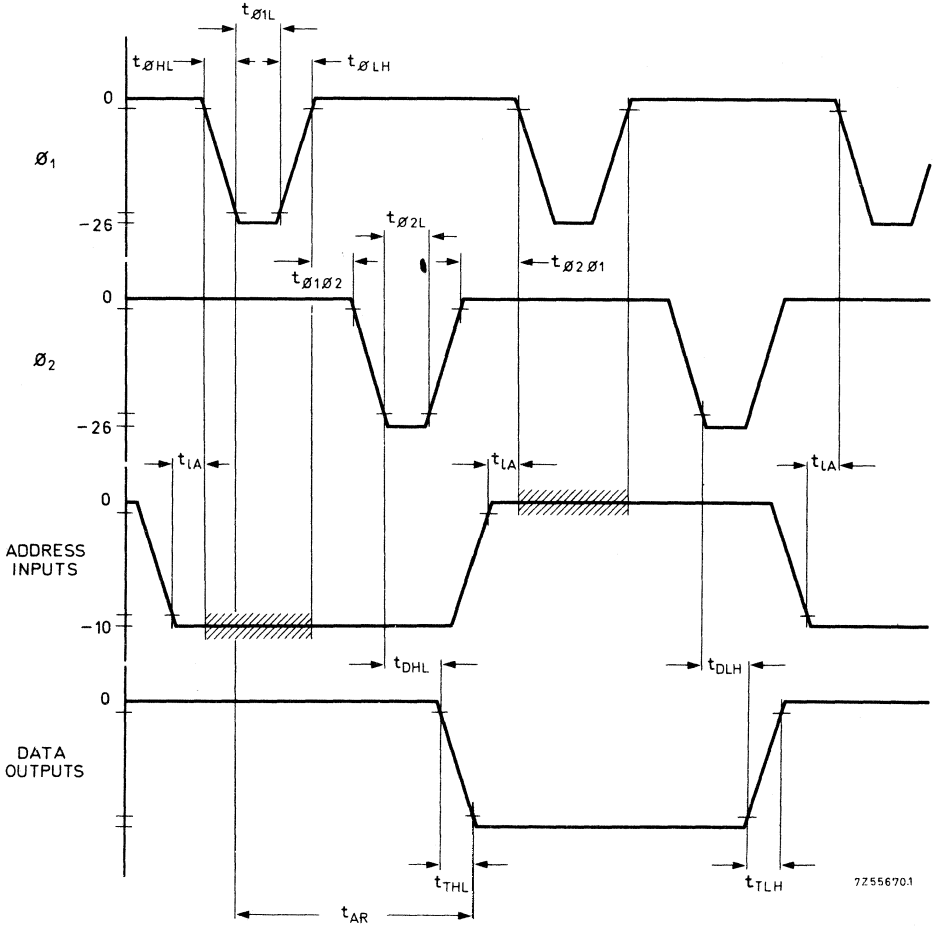
ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	–	0.75	1	µs	
Output levels:						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Address input capacitance	C_A	–	3.6	5.0	pF	bias: V_A = 0 V; f_ϕ = 1 MHz
Output inhibit input capacitance	C_C	–	3.2	4.0	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	–	19	30	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	20	30	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 1}$	–	11	20	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	12	20	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	–	–	1	µA	$V_A = V_C$ = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	µA	V_ϕ = −28 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	400	–	Ω	
LOW	R_{QL}	–	300	–	Ω	V_{P1} = −5 V
Clock power dissipation (see note 1) ($\phi_1+\phi_2$)	P_ϕ	–	36	–	mW	f_ϕ = 1 MHz
Supply current (see note 2)	$-I_{P1}$	–	5.0	–	mA	V_{P1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: fall time	t_{DHL}	–	20	–	ns	
rise time	t_{DLH}	–	20	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

Note 1: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 2: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit timing requirements:

1. Address and output inhibit signals are clocked into the memory during ϕ_1, and must remain present throughout ϕ_1. Address and output inhibit lead time ($t_{\ell A}$) must be ≥ 0, during the shaded interval.
2. The output signals remain steady for as many clock cycles as the address and output inhibit signals remain unchanged.

Note:
The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

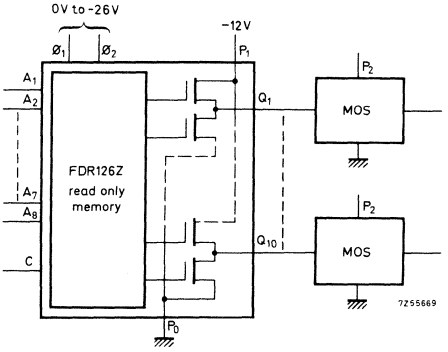
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V.
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Output inhibit time: t_{CL}
   The minimum time that the output inhibit signal must be present during ϕ_2 in order to inhibit the output, defined at −2 V.
10. Read access time: t_{AR}
    The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present.

OUTPUT BUFFER DESCRIPTION

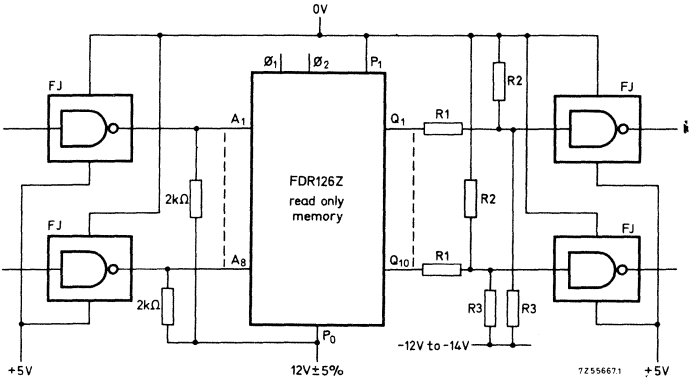
The only d.c. supply required is V_{P1}, the push-pull output buffer supply. V_{P1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

2. Biasing circuit B is used when driving TTL loads direct from each output buffer. This circuit allows also to drive MOS circuits direct from TTL. For this purpose special TTL gates are available (FJH301, FJH311 and FJH321), with a guaranteed minimum output breakdown voltage of 15 V.

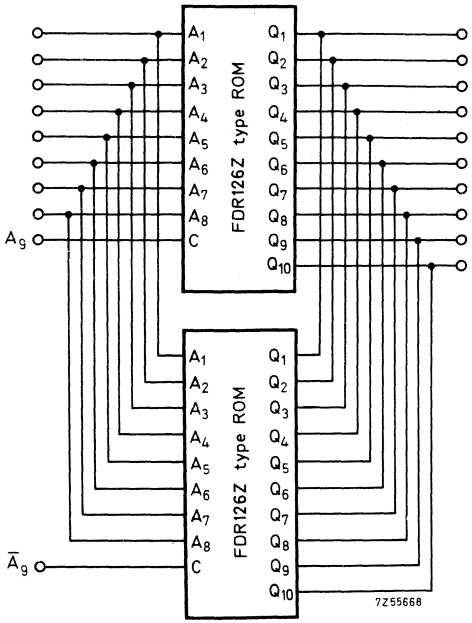


R1 = 820 Ω
R2 = 820 Ω
R3 = 12 kΩ
All resistors: ± 5%

Biasing circuit B

WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-or capability makes it possible to use the FDR126Z type ROM in many different applications, such as those shown here. Note that the terminals A9 and $\overline{A9}$ although shown as address inputs, must actually be output inhibit signals synchronous with the address.



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Four forms are needed for 256 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customers's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS
   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.
   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
   c) Bits 7, 8 and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1])
   Memories of 256 words need 4 pages, of specifications.
   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, as with 256 word memories, column 9 is unused and is, therefore, left blank.

[1]) See example on page 12.

2. CONTENTS (DATA OUTPUTS)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE
   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern FDR 126 ...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

ADDRESS INPUTS 9 8 7 6 5 4 3 2 1	CONTENTS 00 OUTPUTS 10 9 8 7 6 5 4 3 2 1	01 OUTPUTS 10 9 8 7 6 5 4 3 2 1	10 OUTPUTS 10 9 8 7 6 5 4 3 2 1	11 OUTPUTS 10 9 8 7 6 5 4 3 2 1
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

Note: 1 = LOW; 0 = HIGH

GENERAL DESCRIPTION of FDR126Z1

The FDR126Z1 is a version of the FDR126Z pre-programmed to convert from ASCII to SELECTRIC line code and vice versa.
When any 7-bit address of either code is presented to the input the FDR126Z1 will deliver the corresponding word at its output.
The direction of conversion is selected with the eighth address input.
The correspondence between code bits and inputs and outputs is shown in the table below.

address input	ASCII bit	SELECTRIC bit	output
A_1	b_1	1	Q_1
A_2	b_2	2	Q_2
A_3	b_3	4	Q_3
A_4	b_4	8	Q_4
A_5	b_5	A	Q_5
A_6	b_6	B	Q_6
A_7	b_7	S	Q_7

A_8 = LOW: conversion from SELECTRIC line code to ASCII.

A_8 = HIGH: conversion from ASCII to SELECTRIC line code.

Output Q_8 adds an odd parity bit to the 7-bit output code on Q_1 to Q_7 (see note).

Output Q_9 LOW indicates odd parity at the input.

Comparison of the Q_9 output with the parity bit added to the input word indicates whether or not the input code is correct.

If Q_{10} is LOW, the word on outputs Q_1 to Q_7 is a line control code.

Note:
1 = LOW; 0 = HIGH

ASCII CODE

b7 → / b6 → / b5 →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL / IL1	DLE / PRE2	SPACE / SPACE1	0 / 0	@ / @	P / P	\ / |	p / p
0 0 0 1	1	SOH / b	DC1 / RS2	! / !	| / |	A / A	Q / Q	a / a	q / q
0 0 1 0	2	STX / 9	DC2 / PN1	" / "	2 / 2	B / B	R / R	b / b	r / r
0 0 1 1	3	ETX / EOB1	DC3 / RS1	# / #	3 / 3	C / C	S / S	c / c	s / s
0 1 0 0	4	EOT / EOT1	DC4 / PF1	$ / $	4 / 4	D / D	T / T	d / d	t / t
0 1 0 1	5	ENQ / UC2	NAK / !	% / %	5 / 5	E / E	U / U	e / e	u / u
0 1 1 0	6	ACK / -	SYN / IL2	& / &	6 / 6	F / F	V / V	f / f	v / v
0 1 1 1	7	BEL / LC1	ETB / EOB2	/ / |	7 / 7	G / G	W / W	g / g	w / w

Note: 1 = LOW; 0 = HIGH

ASCII CODE (continued)

b7 → b6 → b5 →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
1 0 0 0	8	BS / BS1	CAN	(/ (	8 / 8	H / H	X / X	h / h	x / x
1 0 0 1	9	HT / HT1	EM / RES1	) /)	9 / 9	I / I	Y / Y	i / i	y / y
1 0 1 0	10	LF / LF1	SUB / BY1	* / *	: / :	J / J	Z / Z	j / j	z / z
1 0 1 1	11	VT / ②	ESC / PRE1	+ / +	; / ;	K / K	[/ ±	k / k	[/ ±
1 1 0 0	12	FF / ⑤	FS / BY2	, / ,	< / o	L / L	\ / ±	! / !	: / ±
1 1 0 1	13	CR / NL1	GS / RES2	- / -	= / =	M / M	] / ±	m / m	] / ±
1 1 1 0	14	SO / UC1	RS / RES2	. / .	> / ¢	N / N	‾ / ±	n / n	~ / ±
1 1 1 1	15	SI / LC2	US / BY2	/ / /	? / ?	O / O	- / -	o / o	DEL / DEL1

Note: 1 = LOW; 0 = HIGH

SELECTRIC LINE CODE TO ASCII CODE CORRESPONDENCE

S → B → A →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	SPACE1 / SPACE	t / t	! / !	j / j	SPACE2 / SPACE	T / T	o / <	J / J
0 0 0 1	1	1 / 1	x / x	m / m	g / g	± /]	X / X	M / M	G / G
0 0 1 0	2	2 / 2	n / n	. / .	= / =	@ / @	N / N	. / .	+ / +
0 0 1 1	3	3 / 3	u / u	v / v	f / f	# / #	U / U	V / V	F / F
0 1 0 0	4	5 / 5	e / e	| / /	p / p	% / %	E / E	" / "	P / P
0 1 0 1	5	7 / 7	d / d	r / r	; / ;	& / &	D / D	R / R	: / :
0 1 1 0	6	6 / 6	k / k	i / i	q / q	¢ / >	K / K	I / I	Q / Q
0 1 1 1	7	8 / 8	c / c	a / a	, / ,	* / *	C / C	A / A	, / ,

Note: 1 = LOW; 0 = HIGH

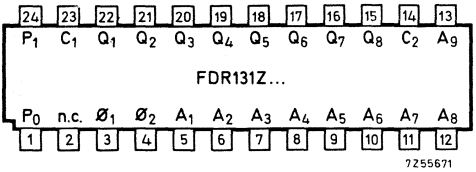
SELECTRIC LINE CODE TO ASCII CODE CORRESPONDENCE (continued)

S → / B → / A →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	row ↓ / column →	0	1	2	3	4	5	6	7
1 0 0 0	8	4 / 4	| / |	o / o	/ / /	$ / $	L / L	O / O	? / ?
1 0 0 1	9	0 / 0	h / h	s / s	y / y	) /)	H / H	S / S	Y / Y
1 0 1 0	10	z / z	① / RS	② / VT	③ / RS	Z / Z	④ / RS	⑤ / FF	⑥ / RS
1 0 1 1	11	9 / 9	b / b	w / w	- / -	(/ (	B / B	W / W	- / -
1 1 0 0	12	PN1 / DC2	BY1 / SUB	RES1 / EM	PF1 / DC4	PN2 / DC2	BY2 / FS	RES2 / GS	PF2 / DC4
1 1 0 1	13	RS1 / DC3	LF1 / LF	NL1 / CR	HT1 / HT	RS2 / DC1	LF2 / LF	NL2 / CR	HT2 / HT
1 1 1 0	14	UC1 / SO	EOB1 / ETX	BS1 / BS	LC1 / BEL	UC2 / ENQ	EOB2 / ETB	BS2 / BS	LC2 / SI
1 1 1 1	15	EOT1 / EOT	PRE1 / ESC	IL1 / NUL	DEL1 / DEL	EOT2 / EOT	PRE2 / DLE	IL2 / NUL	DEL2 / NUL

Note: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

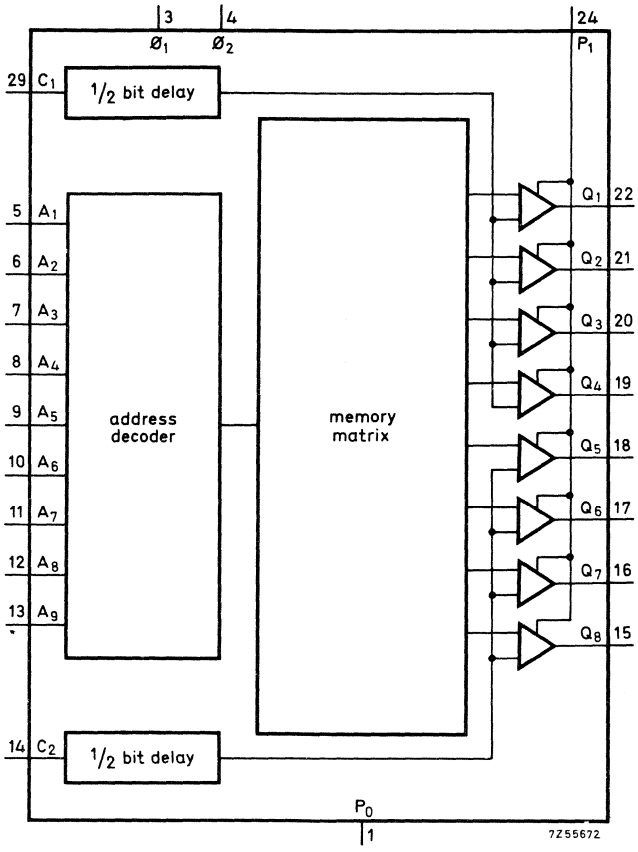
READ ONLY MEMORY, 512 WORD, 8 BITS PER WORD



P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA			
Read access time	t_{AR}	max. 1.5	µs
Clock rate	f_ϕ	max. 0.66	MHz
Power dissipation (MOS load)	P_{tot}	typ. 100	mW
D.C. noise margin	M_H, M_L	> 1.0	V
Operating ambient temperature	T_{amb}	0 to 70	°C

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See page 18)


3
4
24
Ø1
Ø2
P1
29 C1
1/2 bit delay
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 A8
13 A9
address decoder
memory matrix
Q1 22
Q2 21
Q3 20
Q4 19
Q5 18
Q6 17
Q7 16
Q8 15
14 C2
1/2 bit delay
P0
1
7Z55672

GENERAL DESCRIPTION

The FDR131Z is a monolithic 4096-bit READ-only memory (ROM) with a capacity of 512 words, 8 bits per word. With two output-inhibit control lines C_1 and C_2 it can also operate as a 1024-word, 4 bits per word memory. The memory matrix is given the desired content by means of a special mask. When ordering, customers have to complete a set of forms specifying the bit pattern to be associated with each address. The output-inhibit control make it possible to use several FDR131Z memories in wired-OR configuration.

The only d.c. supply is the output buffer supply (P_1), which may be adapted to interface direct with either MOS or bipolar DTL/TTL. All terminals of the FD circuits are effectively protected against over voltage caused by static charge.

A pre-programmed specimen of the FDR131Z is the FDR131Z1 given on page 14.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to −30		V
Power dissipation up to $T_{amb} = 25\,^{o}C$	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	^{o}C
Storage temperature	T_{stg}	−65 to +150		^{o}C
Total current through terminal P_1	$-I_{P_1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	$^{o}C/W$

CHARACTERISTICS at T_{amb} = 0 to +70 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.1	–	0.66	MHz	(see note)
Clock pulse width	$t_{\phi 1L}$	0.90	–	2.0	µs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.35	–	2.0	µs	
Clock pulse rise time (ϕ_1, ϕ_2)	$t_{\phi LH}$	–	–	1.0	µs	See note
Clock pulse fall time	$t_{\phi 1HL}$	0.165	–	1.0	µs	
	$t_{\phi 2HL}$	–	–	1.0	µs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	4.5	µs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	4.5	µs	
Clock input voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Address input and output inhibit input logic levels:						
HIGH	V_{AH}, V_{CH}	−2	0	+0.3	V	
LOW	V_{AL}, V_{CL}	−14	−12	−9	V	

Note:
At frequencies higher than 191 kHz the maximum clock pulse rise and fall times will be determined by the minimum ϕ_1 and ϕ_2 pulse width.

CHARACTERISTICS

Test conditions: V_{P1} = −12 V to −14 V; T_{amb} = 0 to +70 °C; P_0 = grounded; standard load: 30 pF in parallel with 150 kΩ to P_0.

ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	–	1.2	1.5	µs	see note 1
Output levels:						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Address input and output inhibit input capacitances	C_A, C_C	–	3.2	4.0	pF	bias: $V_A = V_C = 0$ V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	–	18	22	pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	16	20	pF	
	$C_{\phi 1}$	–	11	14	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	9.5	12	pF	
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	–	–	1	µA	$V_A = V_C$ = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	µA	V_ϕ = −28 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	500	–	Ω	
LOW	R_{QL}	–	350	–	Ω	V_{P1} = −5 V
Clock power dissipation (see note 2) ($\phi_1 + \phi_2$)	P_ϕ	–	36	–	mW	f_ϕ = 1 MHz
Supply current (see note 3)	$-I_{P1}$	–	4.0	–	mA	V_{P1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	200	–	ns	
rise time	t_{TLH}	–	200	–	ns	
Delay times: fall time	t_{DHL}	–	20	–	ns	
rise time	t_{DLH}	–	20	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

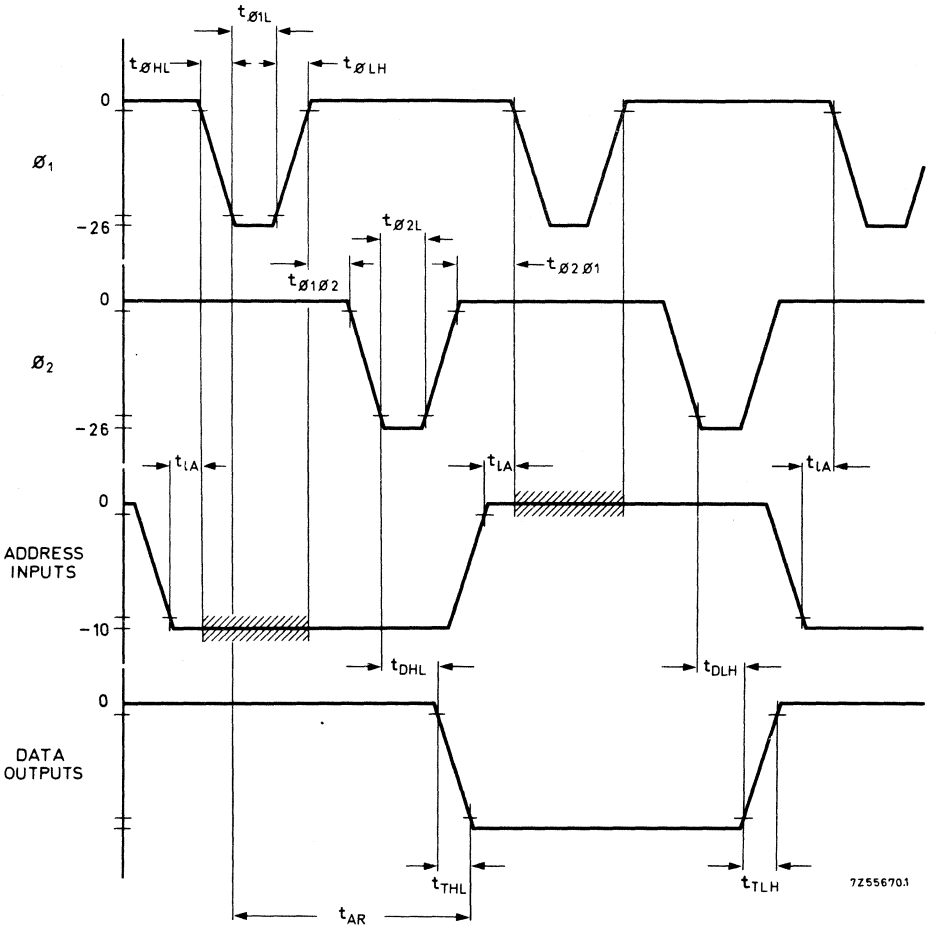
Note 1: Assuming the fall time of ϕ_1 and rise time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit requirements:

1. Address and output inhibit signals are clocked into the memory during $\phi 1$, and must remain present during the shaded interval. Address lead time ($t_{\ell A}$) must be ≥ 0.
2. The output signals remain steady when the address and output inhibit signals remain unchanged.

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

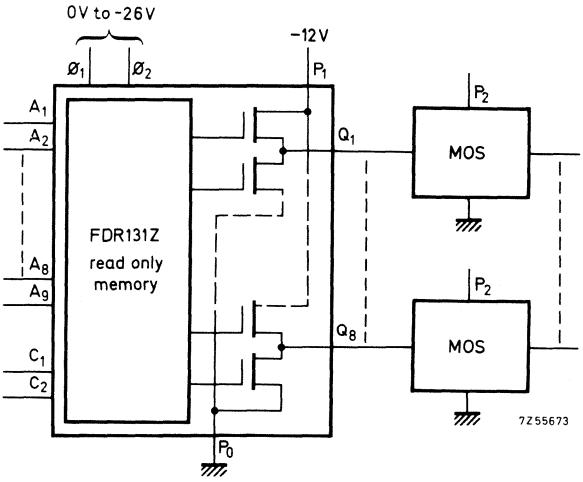
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output start to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read acces time: t_{AR}
   The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

The only d.c. supply required is V_{P1}, the push-pull output buffer supply. V_{P1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

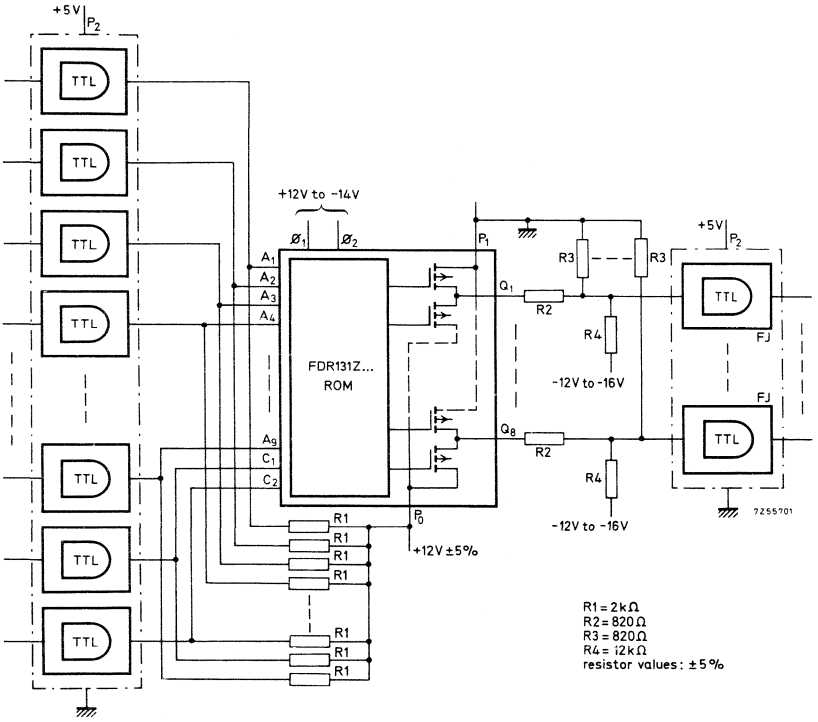
1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit B is used to interface direct with TTL on both the inputs and outputs of the READ-only memory. No active interface components are required. The TTL circuits on the inputs of the ROM must be able to sustain at least +12 V at their outputs.
   The quadruple NAND gate FJH301 and the sextuple inverter FJH321 are especially manufactured with a guaranteed breakdown voltage of 15 V for this purpose.

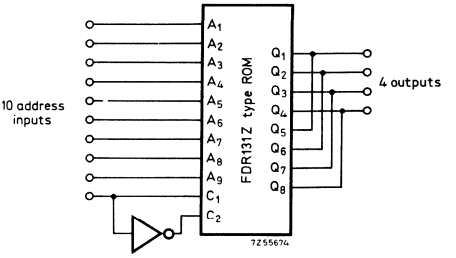


WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. C_1 controls output buffers 1 to 4, and C_2 controls output buffers 5 to 8. This output inhibit wired-or capability makes it possible to use the FDR131Z type ROM in many different applications, such as those shown here.

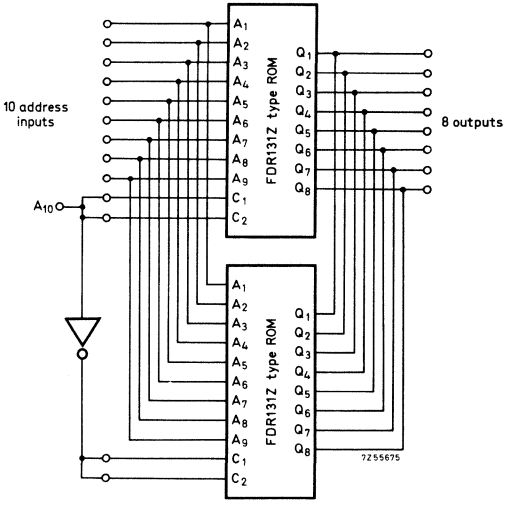
1024 words

4-bits per word



1024 words

8-bits per word



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 13. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched cards are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customer's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid-out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS
   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.
   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
   c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1]
   Memories of 256 words need 4 pages, of specifications.
   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, a column is unused and is, therefore, left blank.

[1]) See example on page 13

2. CONTENTS (DATA OUTPUTS)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE
   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

Note: 1 = LOW; 0 = HIGH

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern FDR 131...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

ADDRESS INPUTS	CONTENTS			
	00	01	10	11
	OUTPUTS	OUTPUTS	OUTPUTS	OUTPUTS
9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

GENERAL DESCRIPTION of FDR131Z 1

The FDR131Z1 is a version of the FDR131Z pre-programmed to convert from ASCII to EBCDIC and vice versa.
When the standard 7-bit ASCII code plus parity is presented to address inputs A_1 to A_8, the FDR131Z1 will deliver the corresponding 8-bit EBCDIC code at its outputs, when the A_9 input is HIGH. Conversely, when the standard 8-bit EBCDIC code is presented to inputs A_1 to A_8, the corresponding ASCII code plus parity will be delivered at the outputs when A_9 is LOW. The code conversion circuits from ASCII to EBCDIC are provided in duplicate to accomodate either odd or even parity. The correspondence between code bits and inputs and outputs is shown in the tables below and on the following pages.

Conversion from ASCII to EBCDIC

ASCII-bits	ROM inputs [1]	ROM outputs	EBCDIC-bits
b_1 (least significant bit)	A_1	Q_1	7 (least significant bit)
b_2	A_2	Q_2	6
b_3	A_3	Q_3	5
b_4	A_4	Q_4	4
b_5	A_5	Q_5	3
b_6	A_6	Q_6	2
b_7 (most significant bit)	A_7	Q_7	1
b_8 (odd or even paratity)	A_8	Q_8	0 (most significant bit)

Correspondence of ASCII(A) to EBCDIC(E) code

To find the 7-bit ASCII code for a particular symbol, (see table on page 15) write down the binary coded decimal number belonging to that symbol; e.g., the number belonging to the letter g is 103, which means that the corresponding binary digits for bits b_7 to b_1 of the ASCII code are 1100111.

[1]) Condition: A_9 is HIGH

Correspondence of ASCII(A) to EBCDIC(E) code (continued)

	0-15		16-31		32-47		48-63		64-79		80-95		96-111		112-127	
	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A	E
0	NUL	NUL	DLE	DLE	SP	SP	0	0	@	@	P	P	\	¦	p	p
1	SOH	SOH	DC1	DC1	!	!	1	1	A	A	Q	Q	a	a	q	q
2	STX	STX	DC2	DC2	"	"	2	2	B	B	R	R	b	b	r	r
3	ETX	ETX	DC3	DC3	#	#	3	3	C	C	S	S	c	c	s	s
4	EOT	EOT	DC4	DC4	$	$	4	4	D	D	T	T	d	d	t	t
5	ENQ	ENQ	NAK	NAK	%	%	5	5	E	E	U	U	e	e	u	u
6	ACK	ACK	SYN	SYN	&	&	6	6	F	F	V	V	f	f	v	v
7	BEL	BEL	ETB	EOB	´	'	7	7	G	G	W	W	g	g	w	w
8	BS	BS	CAN	CAN	(	(	8	8	H	H	X	X	h	h	x	x
9	HT	HT	EM	EM	)	)	9	9	I	I	Y	Y	i	i	y	y
10	LF	LF	SUB	SUB	*	*	:	:	J	J	Z	Z	j	j	z	z
11	VT	VT	ESC	PRE	+	+	;	;	K	K	[	(	k	k	{	(
12	FF	FF	FS	IFS	,	,	<	<	L	L	\	/	l	l	:	¦
13	CR	CR	GS	IGS	-	-	=	=	M	M	]	)	m	m	]	)
14	SO	SO	RS	IRS	.	.	>	>	N	N	^	¬	n	n	~	¢
15	SI	SI	US	IUS	/	/	?	?	O	O	_	_	o	o	DEL	DEL

Explanation of symbols

NUL = null
SOH = start of heading
STX = start of text
ETX = end of text
EOT = end of transmission
ENQ = enquiry
ACK = acknowledge
BEL = bell
BS = backspace
HT = horizontal tab
FF = form-feed
CR = carriage return
SO = shift out
SI = shift in

DLE = data link escape
DC1 to DC4 = device control
NAK = negative acknowledge
SYN = synchronous idle
ETB = end of transmission block
CAN = cancel
EM = end of medium
SUB = substitute
ESC = escape
FS = file separator
GS = group separator
RS = record separator
US = unit separator
DEL = delete (rub out)

The ASCII to EBCDIC characters for which there was no correspondence have been converterd as follows:

128-ASCII	256-EBCDIC
[	(
\	/
]	)
^	¬

128-ASCII	256-EBCDIC
\	¦ 1)
{	(
}	)
~	¢

1) The EBCDIC to ASCII is ' to ´

Conversion from EBCDIC to ASCII

When the standard 8-bit EBCDIC code is presented to inputs A_1 to A_8, the corresponding ASCII code plus parity will be delivered at the outputs when A_9 is LOW.

EBCDIC-bits	ROM-inputs [1]	ROM-outputs	ASCII-bits
7 (least significant bit)	A_1	Q_1	b_1 (least significant bit)
6	A_2	Q_2	b_2
5	A_3	Q_3	b_3
4	A_4	Q_4	b_4
3	A_5	Q_5	b_5
2	A_6	Q_6	b_6
1	A_7	Q_7	b_7 (most significant bit)
0 (most significant bit)	A_8	Q_8	b_8 (even parity)

Correspondence of EBCDIC to ASCII code

	0-15		16-31		32-47		48-63		64-79		80-95		96-111		112-127	
	E	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A
0	NUL	NUL	DLE	DLE	DS	–	–	–	SP	SP	&	&	–	–	–	–
1	SOH	SOH	DC1	DC1	SOS	–	–	–	–	–	–	–	/	/	–	–
2	STX	STX	DC2	DC2	FS	–	SYN	SYN	–	–	–	–	–	–	–	–
3	ETX	ETX	DC3	DC3	–	–	–	–	–	–	–	–	–	–	–	–
4	PF	–	RES	–	BYP	–	PN	–	–	–	–	–	–	–	–	–
5	HT	HT	NL	–	LF	LF	RS	–	–	–	–	–	–	–	–	–
6	LC	–	BS	BS	EOB	ETB	VC	–	–	–	–	–	–	–	–	–
7	DEL	DEL	IL	–	PRE	ESC	EOT	EOT	–	–	–	–	–	–	–	–
8	–	–	CAN	CAN	–	–	–	–	–	–	–	–	–	–	–	–
9	–	–	EM	EM	–	–	–	–	–	–	–	–	–	–	–	–
10	SMM	–	CC	–	SM	–	–	–	¢	–	!	!	–	–	:	:
11	VT	VT	–	–	–	–	–	–	.	.	$	$	,	,	#	#
12	FF	FF	IFS	FS	–	–	DC4	DC4	<	<	*	*	%	%	@	@
13	CR	CR	IGS	GS	ENQ	ENQ	NAK	NAK	(	(	)	)	–	–	,	↗
14	SO	SO	IRS	RS	ACK	ACK	–	–	+	+	;	;	>	>	=	=
15	SI	SI	IUS	US	BEL	BEL	SUB	SUB	|	:	¬	–	?	?	"	"

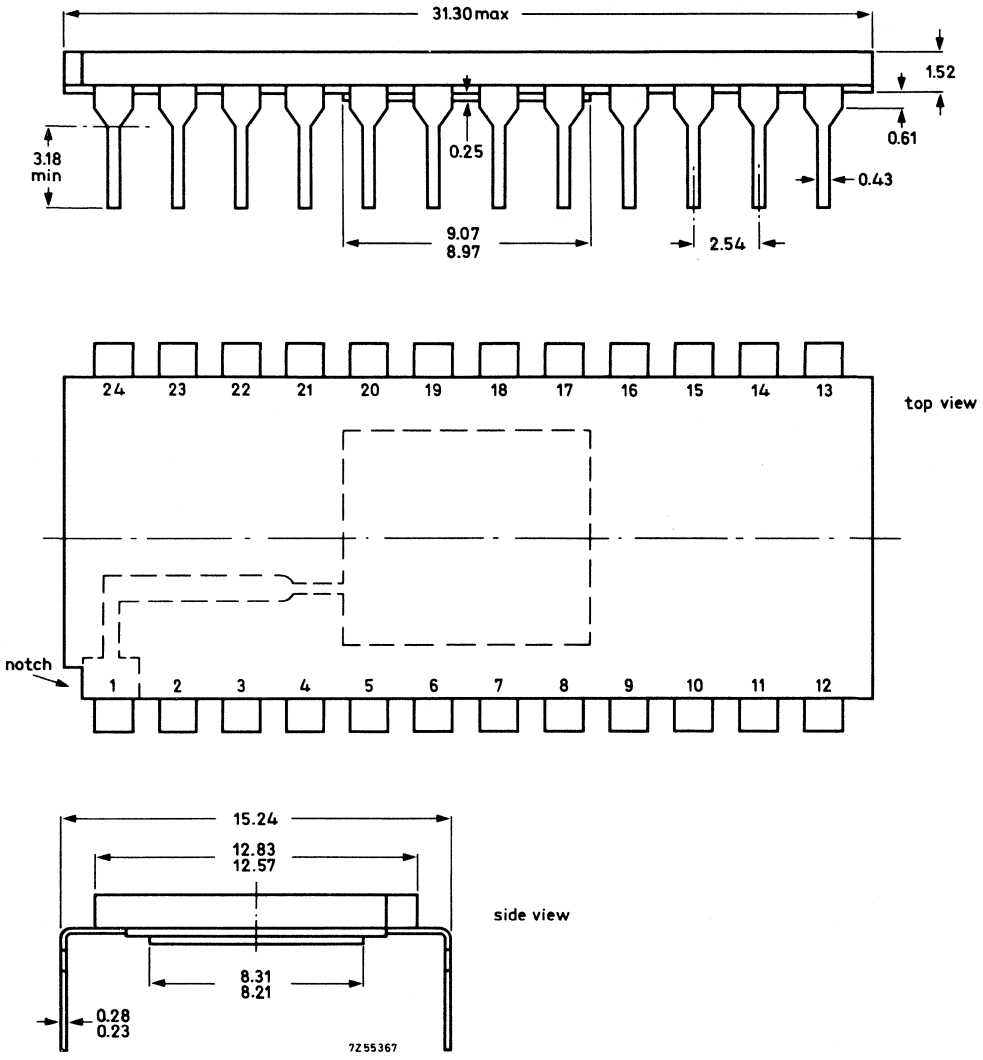
[1]) Condition: A_9 = LOW

Correspondence of EBCDIC to ASCII code (continued)

To find the 8-bit EBCDIC code for a particular symbol (see table below and on page 16), write down the decimal number belonging to that symbol; e.g., the number belonging to the letter g is 135, which means the corresponding number for the bit positions 0 to 7 of the EBCDIC code is 10000111.

128-143		144-159		160-175		176-191		192-207		208-223		224-239		240-255	
E	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A
–	–	–	–	–	–	–	–	–	–	–	–	–	–	0	0
a	a	j	j	–	–	–	–	A	A	J	J	–	–	1	1
b	b	k	k	s	s	–	–	B	B	K	K	S	S	2	2
c	c	l	l	t	t	–	–	C	C	L	L	T	T	3	3
d	d	m	m	u	u	–	–	D	D	M	M	U	U	4	4
e	e	n	n	v	v	–	–	E	E	N	N	V	V	5	5
f	f	o	o	w	w	–	–	F	F	O	O	W	W	6	6
g	g	p	p	x	x	–	–	G	G	P	P	X	X	7	7
h	h	q	q	y	y	–	–	H	H	Q	Q	Y	Y	8	8
i	i	r	r	z	z	–	–	I	I	R	R	Z	Z	9	9
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line



Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a notch and connected to the metal lid on the bottom of the package.

Linear integrated circuits

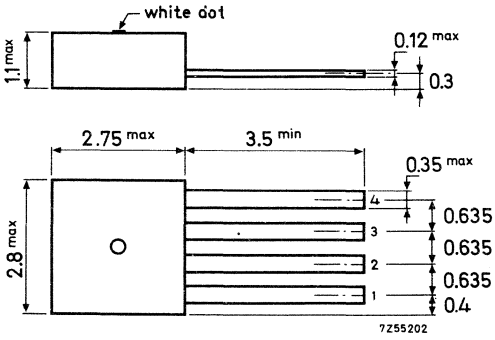
INTEGRATED CIRCUIT
AMPLIFIER FOR IN THE EAR HEARING AID

Monolithic semiconductor integrated-circuit amplifier in a plastic envelope, primarily intended for in the ear hearing aids.

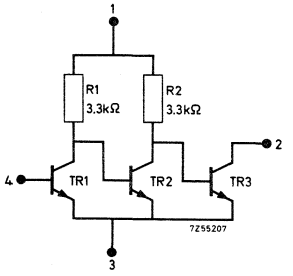
QUICK REFERENCE DATA				
For meaning of symbols: see page 3 fig. 1.				
Supply voltage	V_{1-3}	max.	5	V
Output current	I_2	max.	5	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	25	mW
In a practical circuit as given on page 3 fig. 1:				
Total supply current	I_{tot}	typ.	1	mA
Transducer gain	G_{tr}	>	75	dB
		typ.	80	dB
Power output at d_{tot} = 10 %	P_o	>	0.2	mW
Cut-off frequency (−3 dB)	f_c	>	20	kHz

PACKAGE OUTLINE

Dimensions in mm



CIRCUIT DIAGRAM



The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

RATINGS (Limiting values) [1])
(for meaning of symbols see page 3, fig.1)

Voltages				
Supply voltage	V_{1-3}	max.	5	V
Output voltage	V_{2-3}	max.	5	V [2])
Input voltage	$-V_{4-3}$	max.	5	V
Currents				
Output current	I_2	max.	5	mA
Input current	I_4	max.	5	mA
Power dissipation				
Total power dissipation (See page 6)	P_{tot}	max.	25	mW
Temperatures				
Storage temperature	T_{stg}	−20 to +80		°C
Ambient temperature	T_{amb}	max.	80	°C

CHARACTERISTICS at $V_{1-3} = 1.3$ V and $T_{amb} = 25$ °C unless otherwise specified
I_2 see figure 1

Supply current (no signal)	I_{tot}	<	1.2	mA
	I_1	typ.	0.34	mA
Transducer gain [3]) at f = 1 kHz	G_{tr}	>	75	dB
		typ.	80	dB
$V_{1-3} = 1.3$ V; $T_{amb} = -10$ °C	G_{tr}	typ.	78	dB
$V_{1-3} = 1.1$ V; $T_{amb} = 25$ °C	G_{tr}	typ.	76	dB

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

[2]) This value may be exceeded during inductive switch-off for transient energies < 10 μWs.

[3]) The transducer gain is defined as the ratio of the output power in the load of $|Z| = 1.5$ kΩ and the available input power of the source with $R_S = 5$ kΩ

$$G_{tr} = \frac{P_o}{V_i^2/4R_S}$$

CHARACTERISTICS (continued)

at V_{1-3} = 1.3 V and T_{amb} = 25 °C unless otherwise specified
I_2 see figure 1

Total distortion at f = 1 kHz				
P_o = 100 μW	d_{tot}	typ.	4	%
		<	6	%
P_o = 200 μW	d_{tot}	<	10	%
Noise figure at R_S = 5 kΩ				
Bandwidth f = 400 to 3200 Hz	F	<	6	dB
Cut-off frequency (−3 dB)	f_c	>	20	kHz
		>	50	kΩ
Value of R_F to adjust I_2 at 0.7 mA	R_F	typ.	300	kΩ
		<	700	kΩ

I_2 = 0.7 mA,
adjusted by means of R_F.
V_{1-3} = 1.3 V; T_{amb} = 25 °C.

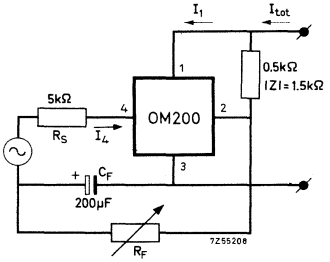


Fig.1

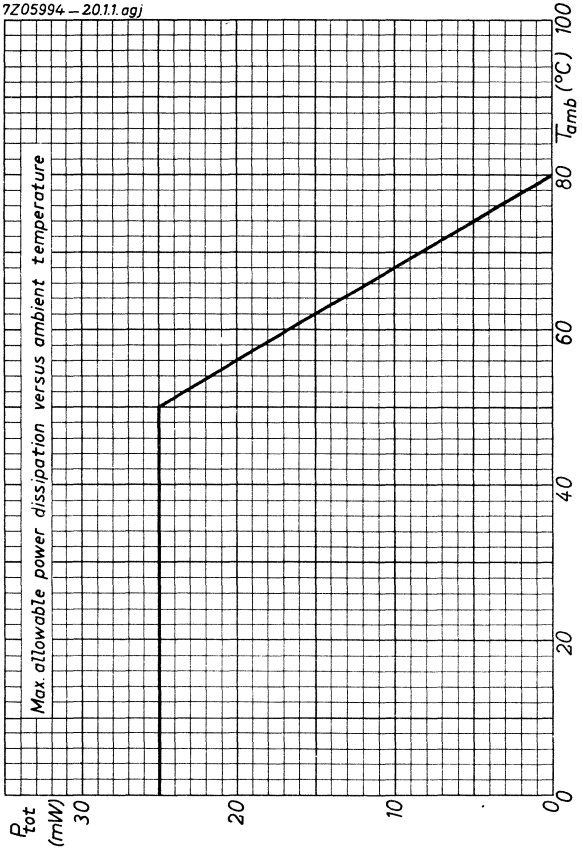
SOLDERING RECOMMENDATION

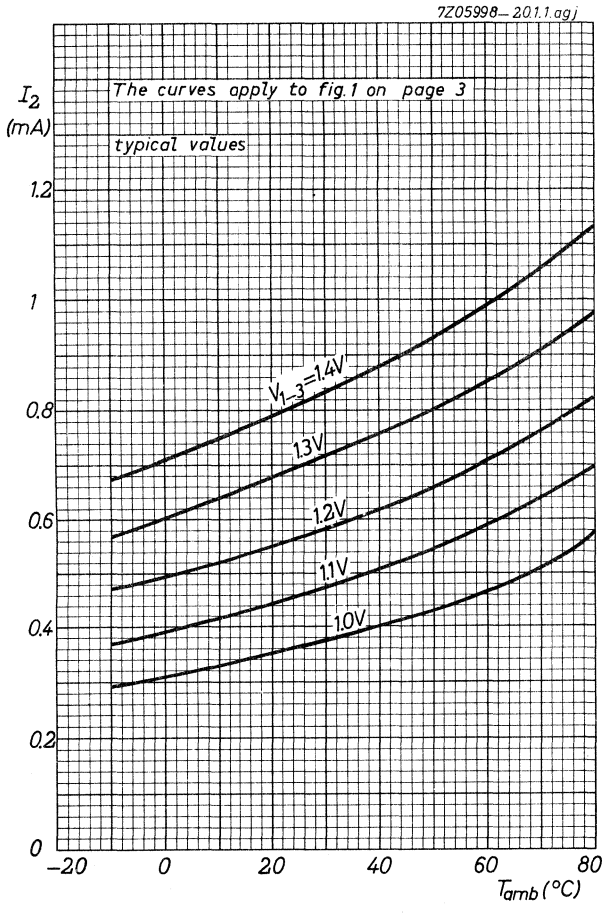
A: Iron soldering

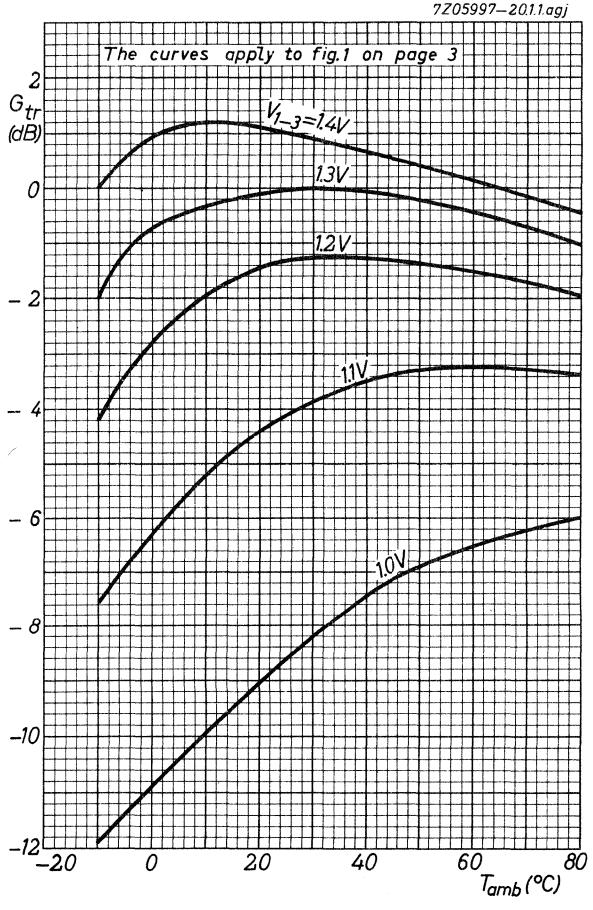
At a maximum iron temperature of 300 °C the maximum permissible soldering time is 3 seconds, provided the soldering spot is at least 0.5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

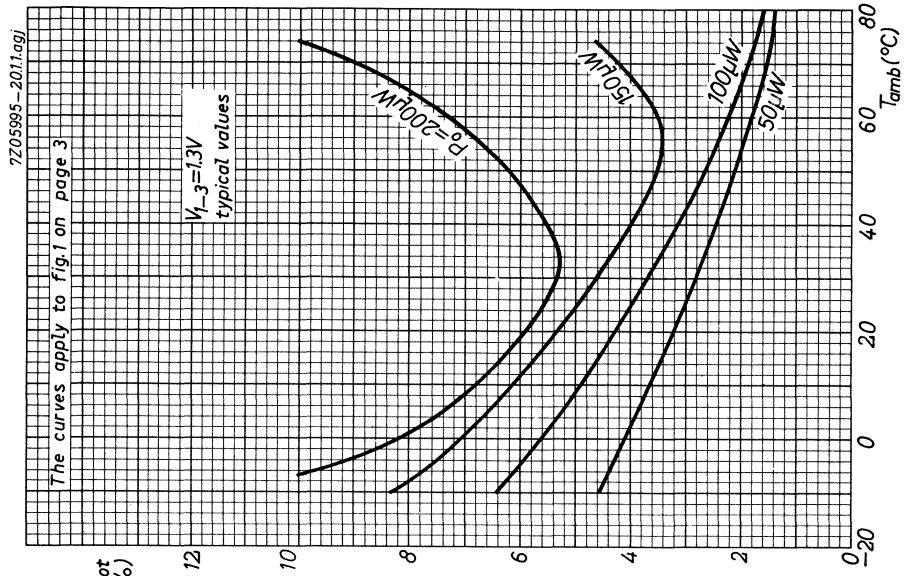
B: Dip soldering

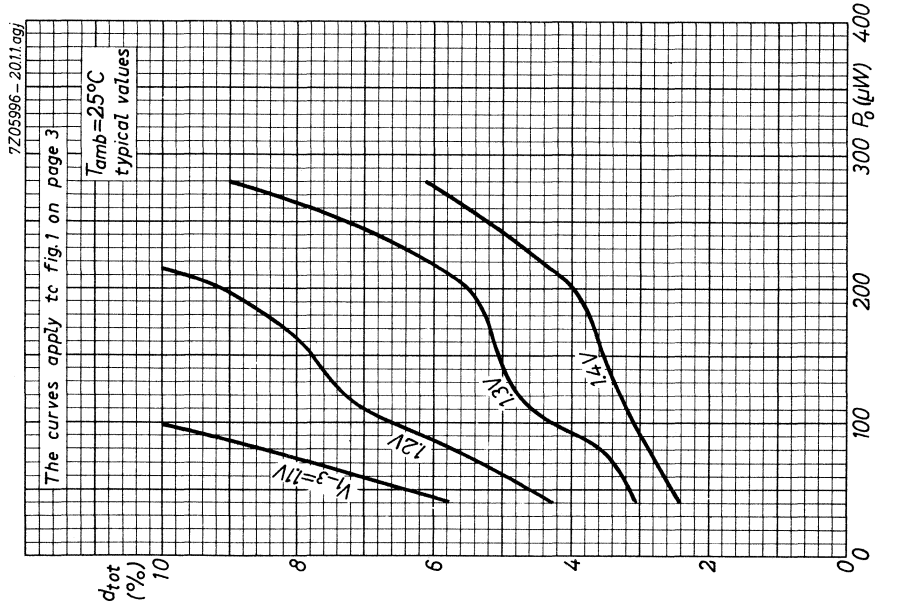
At a maximum solder temperature of 250 °C the maximum permissible soldering time is 3 seconds, provided the soldering spot is at least 0.5 mm from the seal.


7Z05994 – 20.1.1.agj
Max. allowable power dissipation versus ambient temperature
P_{tot} (mW)
30
20
10
0
0
20
40
60
80
100
T_{amb} (°C)


7Z05998–20.1.1.agj
The curves apply to fig.1 on page 3
typical values
I_2 (mA)
1.2
1
0.8
0.6
0.4
0.2
0
V_{1-3}=1.4V
1.3V
1.2V
1.1V
1.0V
–20
0
20
40
60
80
T_{amb} (°C)


7Z05997–20.1.1.agj
The curves apply to fig.1 on page 3
G_{tr} (dB)
2
0
– 2
– 4
– 6
– 8
–10
–12
V_{1-3}=1.4V
1.3V
1.2V
1.1V
1.0V
–20
0
20
40
60
80
T_{amb} (°C)


7Z05995-2011.agj
The curves apply to fig.1 on page 3
V_{1-3}=1.3V
typical values
P_o=200µW
150µW
100µW
50µW
d_{tot} (%)
12
10
8
6
4
2
0
−20
0
20
40
60
80
T_{amb}(°C)


7Z05996-2011.agj
The curves apply to fig.1 on page 3
T_{amb}=25°C
typical values
V_{1-3}=1.1V
1.2V
1.3V
1.4V
d_{tot} (%)
10
8
6
4
2
0
0
100
200
300
400
P_o(µW)

LOW-LEVEL AMPLIFIER

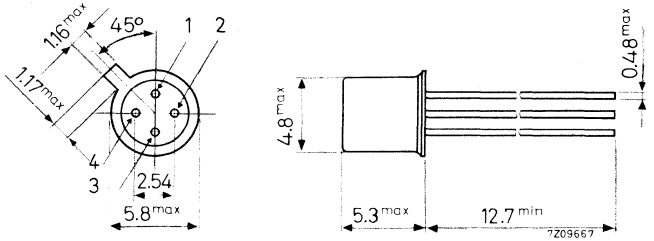
The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

QUICK REFERENCE DATA				
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Output current	I_3	max.	25	mA
Transducer gain at P_o = 10 mW				
R_L = 150 Ω; f = 1 kHz	G_{tr}	typ.	77	dB
Operating ambient temperature	T_{amb}	−20 to +100		°C

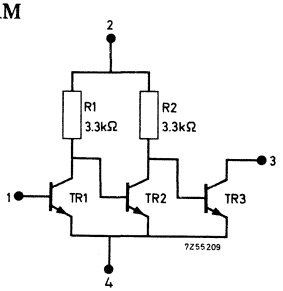
PACKAGE OUTLINE

Dimensions in mm

TO-72



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

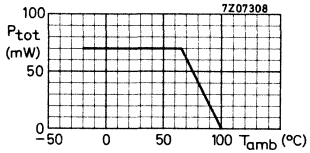
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Input voltage	$-V_{1-4}$	max.	5	V

Currents

Output current	I_3	max.	25	mA
Input current	I_1	max.	10	mA

Power dissipation

Total power dissipation up to $T_{amb} = 65\ ^oC$	P_{tot}	max.	70	mW



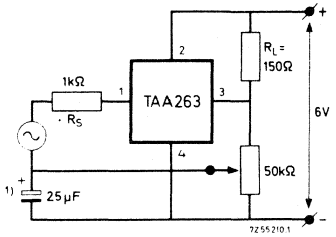
Temperatures

Storage temperature	T_{stg}	−65 to +100	^oC
Operating ambient temperature	T_{amb}	−20 to +100	^oC

CHARACTERISTICS

T_{amb} = 25 °C

Test circuit:



Currents				
Output current	I_3	typ.	12	mA
Total current drain (no signal)	I_2+I_3	<	16	mA
Over-all small signal current gain				
f = 1 kHz	$h_{f\ tot}$	typ.	5.10^5	
Transducer gain				
f = 1 kHz; P_o = 10 mW	G_{tr}	>	70	dB
		typ.	77	dB
Output power at f = 1 kHz; d_{tot} = 10%	P_o	>	10	mW
d_{tot} = 5%	P_o	>	8	mW
Noise figure				
f = 400 Hz to 6 kHz	F	typ.	5	dB
		<	10	dB
f = 450 kHz; Δf = 5 kHz	F	typ.	2.7	dB

1) $Z \leqslant 10\ \Omega$ at f = 1 kHz

CHARACTERISTICS (continued) T_{amb} = 25 °C

y parameters (point 4 common connection)

V_B = 6 V; I_3 = 3 mA; V_{3-4} = 4.2 V

f = 1 kHz

Input admittance	$y_i = g_i$	typ.	20	$\mu\Omega^{-1}$
Transfer admittance	$y_f = g_f$	typ.	11	Ω^{-1}
Output admittance	$y_o = g_o$	typ.	60	$\mu\Omega^{-1}$

f = 450 kHz

Input conductance	g_i	typ.	15	$\mu\Omega^{-1}$
Input capacitance	C_i	typ.	14	pF
Transfer admittance	$\|y_f\|$	typ.	9.4	Ω^{-1}
Phase angle of transfer admittance	φ_f	typ.	125°	
Output conductance	g_o	typ.	20	$\mu\Omega^{-1}$
Output capacitance	C_o	typ.	13	pF

GENERAL PURPOSE AMPLIFIER

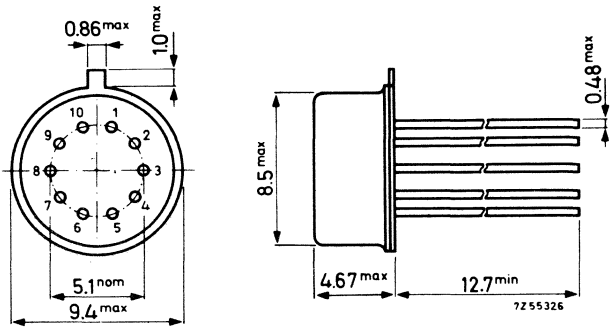
The TAA293 is a general purpose integrated amplifier which can be applied in various audio and i.f. applications. It configuration furthermore allows the use of the TAA293 in multivibrators, pulse amplifiers, trigger circuits, etc.

QUICK REFERENCE DATA				
Supply voltage	V_{7-4}	nom.	+ 6.0	V
Small signal current gain of first transistor I_8 = 1 mA; V_{8-1} = 1 V	h_{fe}	typ.	80	
Transducer gain	G_{tr}	typ.	80	dB
Noise figure (30 to 15 000 Hz)	F	typ.	6	dB
Frequency response (−3 dB)		typ.	600	kHz
Output power	P_o	>	10	mW

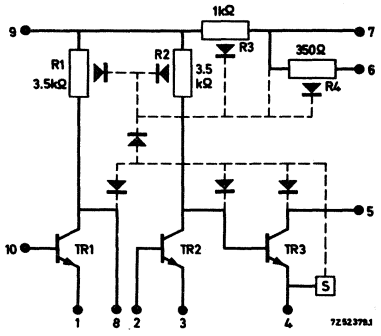
PACKAGE OUTLINE

Dimensions in mm

TO−74; reduced height



CIRCUIT DIAGRAM



Note:

The diodes drawn with dotted lines are the parasitic diodes formed by the P-N junction of the resistor-diffusions in the N-isle and of the N-isle to the P-substrate respectively. Taking account of the parasitic diodes one can prevent any unwanted effects due to their becoming conducting under certain conditions of d.c. potentials or signal voltages.

RATINGS Limiting values in Accordance with the Absolute Maximum System (IEC134)

Voltages

V_{9-1}	max.	7.0	V
V_{8-1}	max.	7.0	V
V_{8-10}	max.	7.0	V
V_{9-3}	max.	7.0	V
V_{9-4}	max.	7.0	V
V_{8-4}	max.	7.0	V
V_{7-4}	max.	7.0	V [1)]
V_{6-4}	max.	7.0	V
V_{5-4}	max.	7.0	V
V_{1-10}	max.	6.0	V
V_{3-2}	max.	6.0	V

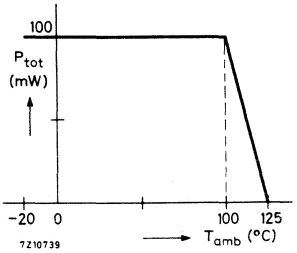
Currents

I_5	max.	40	mA
$-I_4$	max.	40	mA
$-I_1$	max.	20	mA
I_8	max.	20	mA
$-I_3$	max.	10	mA
I_{10}	max.	10	mA
I_2	max.	10	mA

1) Pin 7 must be at the highest potential to avoid unwanted influence of the parasite diodes.

RATINGS (continued)

Total power dissipation



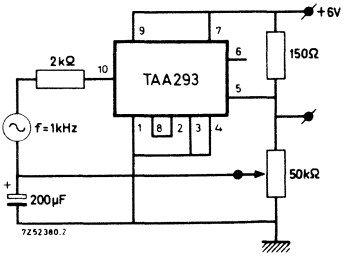
Temperatures

Storage temperature	T_{stg}	−20 to + 125	°C	←
Ambient temperature	T_{amb}	−20 to + 125	°C	

CHARACTERISTICS at T_{amb} = 25 °C; V_{7-4} = 6 V

Collector current				
of the last transistor	I_5	typ.	12	mA
Small signal current gain				
of first transistor I_8 = 1 mA; V_{8-1} = 1 V	h_{fe}	> typ.	30 80	
Saturation voltages				
V_{7-1} = 6 V; R_{9-10} = 35 kΩ	$V_{8-1\ sat}$	typ.	100	mV
V_{7-4} = 6 V; R_4 = 2 kΩ; V_{2-3} = 0	$V_{5-4\ sat}$	typ.	600	mV
Noise figure of first transistor				
I_1 = 100 μA; R_S = 2kΩ; V_{8-1} = 6 V B = 30 Hz to 15000 Hz	F	typ. <	6 10	dB dB
Transducer gain at f = 1 kHz				
P_o = 10 mW	G_{tr}	> typ.	70 80	dB dB
Output power at d_{tot} = 10%	P_o	>	10	mW

Test circuit for measuring the transducer gain and the output power



INTEGRATED 1 WATT AUDIO AMPLIFIER

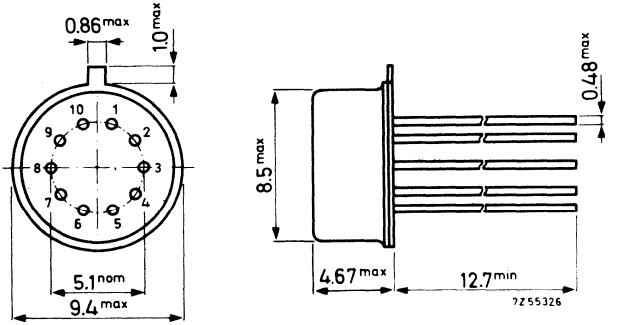
A complete a.f. amplifier in monolithic integrated form incorporating special measures to prevent cross-over distortion throughout an exceptionally wide usable range of supply voltage (4.5 V to 10 V. This, in combination with its low drain current, makes the TAA300 ideally suited for use in battery operated equipment. Due to the high a.c. feedback (≈ 20 dB) the distortion and spread in gain is very low.

QUICK REFERENCE DATA				
Supply voltage	V_B	nom.	9	V
Output power	P_o	typ.	1	W
Input signal for P_o = 1 W	V_i	typ.	8.5	mV
Input impedance	$\|Z_i\|$	typ.	15	kΩ
Load impedance	R_L		8	Ω
Total current (no signal)	I_{tot}	typ.	8	mA

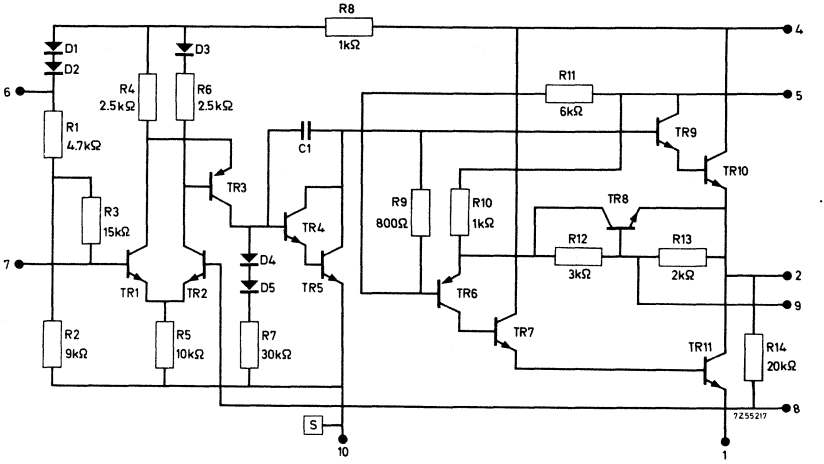
PACKAGE OUTLINE

Dimensions in mm

TO-74; reduced height



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages (see test set-up on page 4)

V_{4-1}	max.	10.5	V
V_{7-8}	max.	6	V
V_{8-7}	max.	6	V
V_{2-9}	max.	6	V
V_{2-1}	max.	10.5	V
V_{4-2}	max.	10.5	V

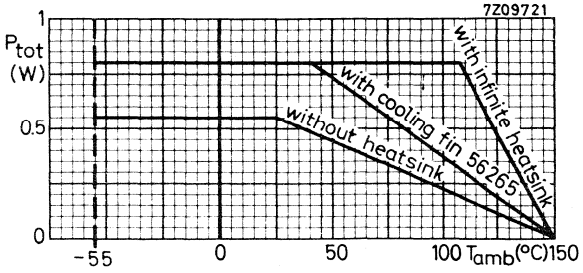
Currents (see test set-up on page 4)

$-I_1$	max.	600	mA
$\pm I_2$	max.	600	mA
$+I_4$	max.	600	mA

Total power dissipation	P_{tot}	see next page
Temperatures		
Storage temperature	T_{stg}	−55 to +150 °C
Operating ambient temperature	T_{amb}	−55 to +150 °C

RATINGS (continued)

Maximum allowable total power dissipation versus ambient temperature

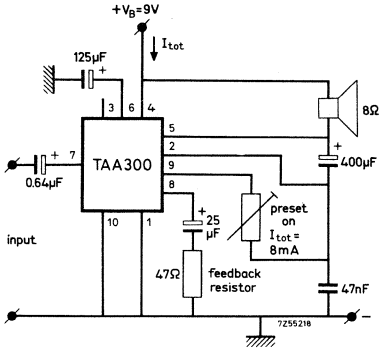


CHARACTERISTICS at T_{amb} = 25 °C; V_B = 9 V

Measured in the test set-up on page 4

Output power at d_{tot} = 10%	P_o	typ.	1	W
Bandwidth (−3 dB)	B	>	10	kHz
		typ.	25	kHz
Total current (d.c.)				
no signal and excluding output transistors:	I_{tot}	typ.	4	mA
with signal at P_o = 1 W:	I_{tot}	typ.	180	mA
Total distortion at P_o = 0.5 W	d_{tot}	typ.	0.7	%
		<	3	%
Input signal at P_o = 1 W	V_i	typ.	8.5	mV
P_o = 0.5 W	V_i	<	8.5	mV
Input impedance	$\lvert Z_i \rvert$	>	10	kΩ
		typ.	15	kΩ
Efficiency	η	typ.	60	%
Signal to noise ratio related to P_o = 1 W				
R_S = 2 kΩ; B = 30 Hz to 15 kHz	$\frac{S}{N}$	>	70	dB
		typ.	75	dB
Noise output power				
input short circuited; B = 30 Hz to 15 kHz	P_N	typ.	10	nW
		<	20	nW
Preset resistor for I_{tot} = 8 mA	R_{pr}	4 to 25		kΩ

TEST SET-UP



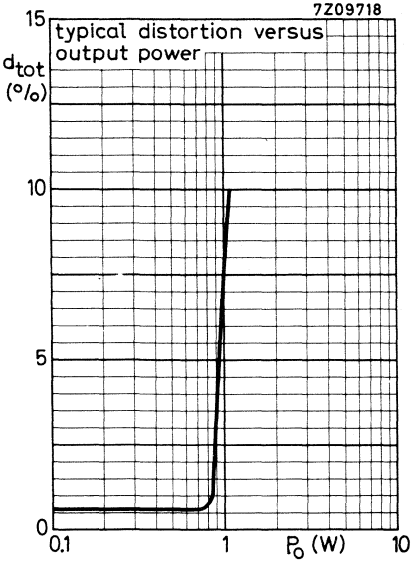
To prevent high-frequency instability, the following precautions must be taken.

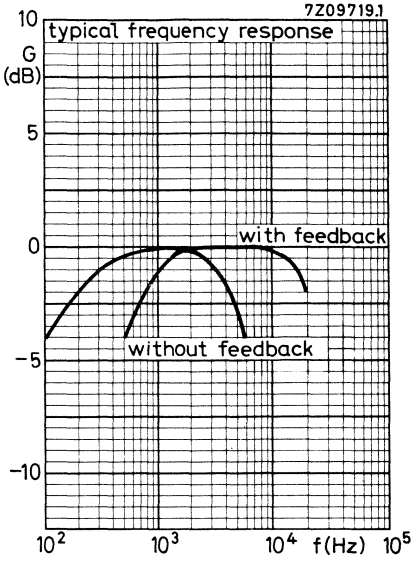
a. Keep the lead inductance from the positive voltage supply to pin 4 to a minimum.

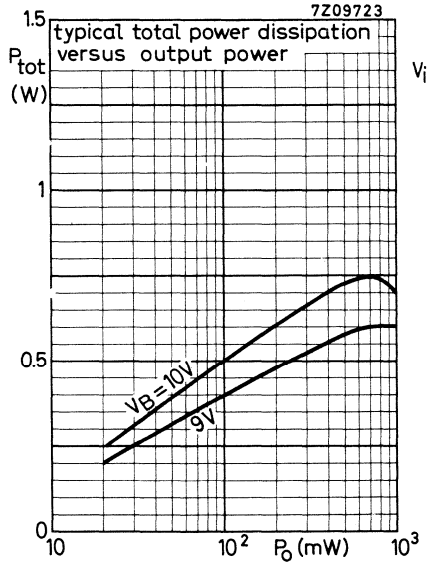
b. Because of the high internal resistance of batteries (especially at end of life) a large capacitance should be connected between pin 4 and ground.

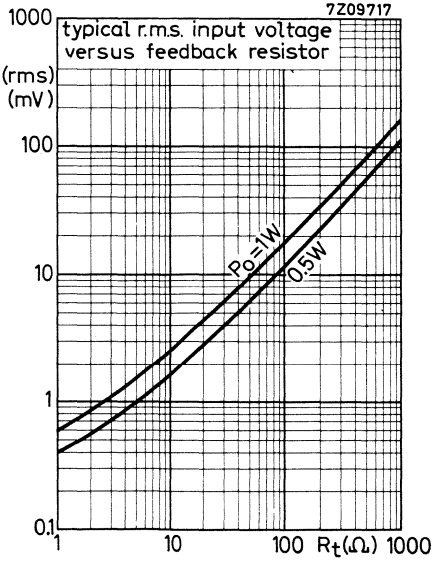
c. A capacitor of at least 47 nF should be connected between pin 2 and ground to prevent instability of the lower Darlington output transistor (see also test set-up).

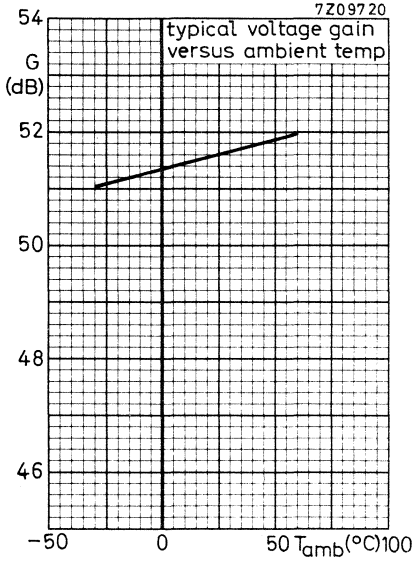
d. Avoid coupling between output and input leads (especially those carrying signals from a high-impedance source). This coupling can be reduced by using short leads, shielded input cable or by limiting the upper frequency to 15 kHz by means of a capacitor of 560 pF between pin 7 and ground.

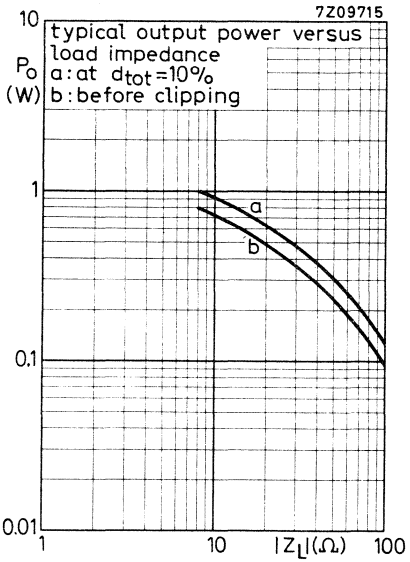

7Z09718
typical distortion versus output power
d_{tot} (%)
15
10
5
0
0.1
1
P_o (W)
10

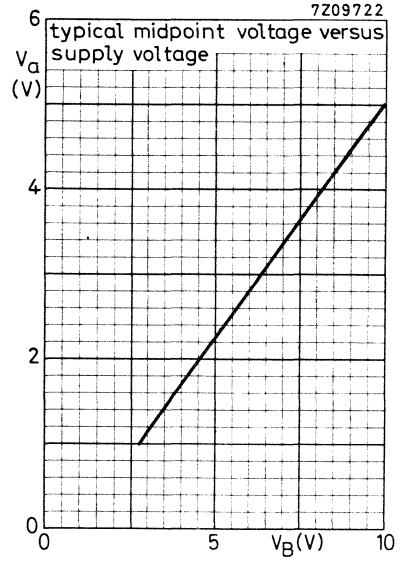

7Z09719.1
typical frequency response
G (dB)
10
5
0
−5
−10
with feedback
without feedback
10^2
10^3
10^4
f(Hz)
10^5

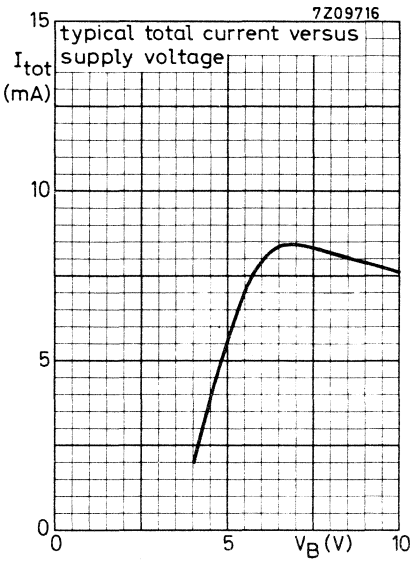

7Z09723
typical total power dissipation versus output power
P_{tot} (W)
1.5
1
0.5
0
V_B=10V
9V
10
10^2
P_o (mW)
10^3


7Z09717
typical r.m.s. input voltage versus feedback resistor
V_i(rms) (mV)
1000
100
10
1
0.1
P_o=1W
0.5W
1
10
100
R_t(Ω)
1000


7Z09720
typical voltage gain
versus ambient temp
G
(dB)
54
52
50
48
46
−50
0
50
T_{amb}(°C)
100


7Z09715
typical output power versus
load impedance
a: at d_{tot}=10%
b: before clipping
P_o
(W)
10
1
0.1
0.01
a
b
1
10
$|Z_L|$(Ω)
100


7Z09722
typical midpoint voltage versus
supply voltage
V_a
(V)
6
4
2
0
0
5
V_B(V)
10


7Z09716
typical total current versus
supply voltage
I_{tot}
(mA)
15
10
5
0
0
5
V_B(V)
10

A.F. PREAMPLIFIER

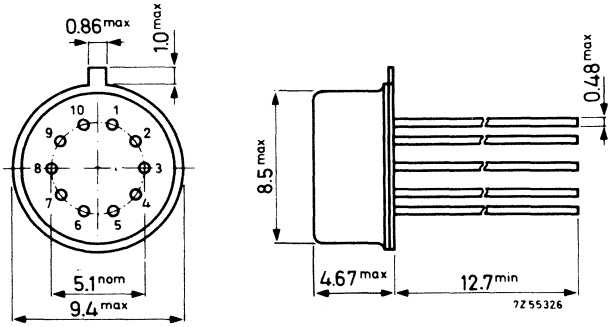
The TAA310 is a monolithic integrated circuit designed for use as an a.f. high-gain preamplifier, with a very low noise figure (< 4 dB) and a high voltage gain of at least 90 dB. Because this gain can be achieved at a low load impedance (1 kΩ) and the input impedance is high, the TAA310 is specially suited for the recording and playback amplifier in tape recorders.

QUICK REFERENCE DATA				
Supply voltage	V_B	nom.	+7	V
Voltage gain	G_V	typ.	100	dB
Noise figure (B = 30 to 15.000 Hz)	F	typ.	2.5	dB
Input impedance	z_i	typ.	20	kΩ

PACKAGE OUTLINE

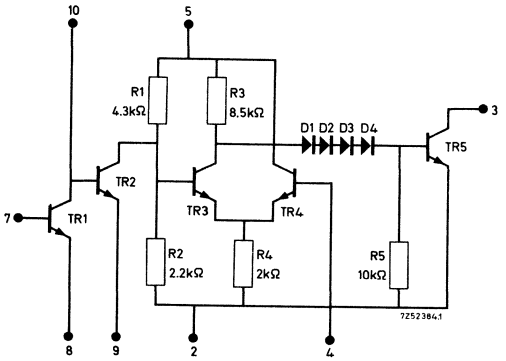
TO-74; reduced height

Dimensions in mm



Pins 1 and 6 are not connected

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

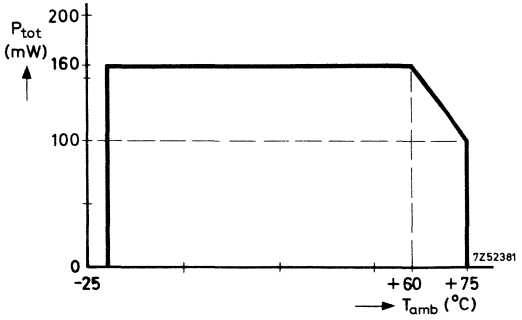
V_{5-2}	max.	9.5	V
V_{3-2}	max.	9.5	V
V_{10-8}	max.	6	V
V_{8-7}	max.	6	V
V_{9-10}	max.	6	V
V_{4-2}	max.	6	V

The pins 3, 4, 5 and 10 must never have a negative potential with respect to pin 2 (substrate).

Currents

I_3	max.	20	mA
I_7	max.	3	mA
$-I_8$	max.	10	mA
$-I_9$	max.	10	mA
I_{10}	max.	10	mA
I_4	max.	3	mA

Total power dissipation



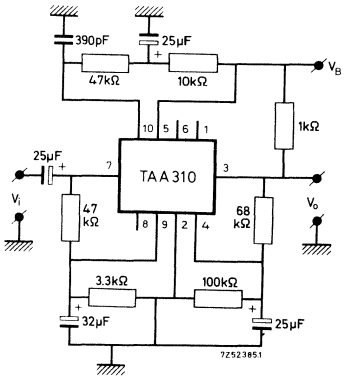
Temperatures

Storage temperature	T_{stg}	−20 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +75	°C

CHARACTERISTICS at T_{amb} = 25 °C

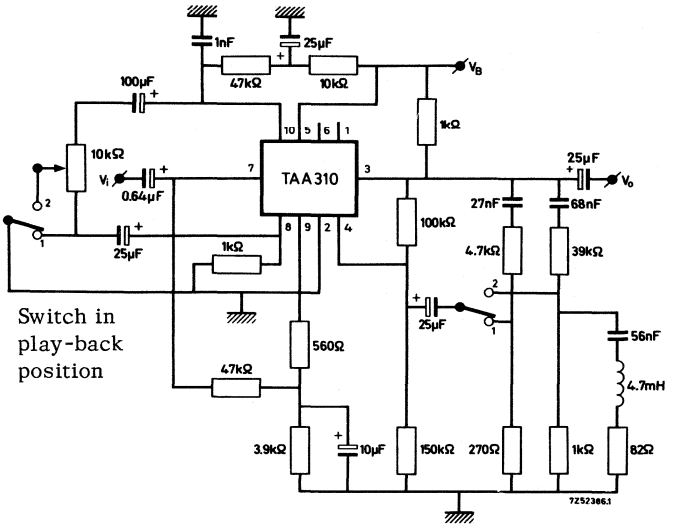
D.C. current gain				
of first transistor I_{10} = 100 μA; V_{10-7} = 0	h_{FE}	>	40	
Input impedance at f = 1 kHz				
I_{10} = 100 μA; V_{10-7} = 0	z_i	typ.	20	kΩ
Voltage gain	G_v	> typ.	93 100	dB dB
Noise figure				
R_S = 2 kΩ; B = 30 to 15 000 Hz	F	typ. <	2.5 4	dB dB
Output voltage at d_{tot} = 10%	$V_{o(rms)}$	typ.	2	V
Cut-off frequency (−3 dB)	f_c	≥	15	kHz
Saturation voltage				
of output transistor at I_3 = 7 mA	$V_{3-2\ sat}$	typ. <	0.8 1.2	V V
D.C. collector voltage				
of output transistor at I_9 = 200 μA	V_{3-2}	typ. 3.4 to	3.8 4.2	V V

Test circuit for measuring G_v, F, $V_{o(rms)}$, f_c and V_{3-2} at V_B = 7 V



APPLICATION INFORMATION

Practical tape-recorder preamplifier with a TAA310.

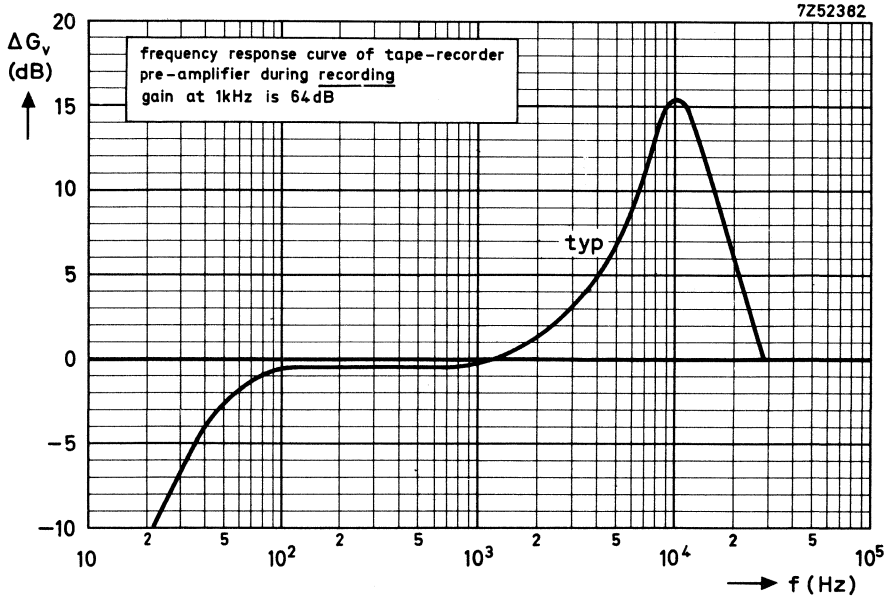


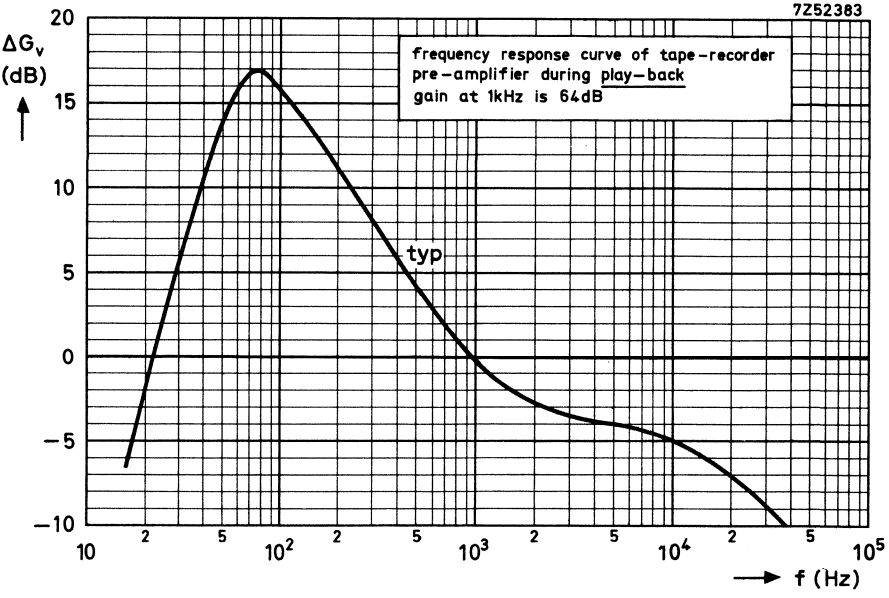
Data for use as recording amplifier (measured at f = 1 kHz)

Voltage gain	G_v		64 ± 2	dB
Frequency response (see page 6)				
Distortion at $V_{o(rms)}$ = 0.5 V	d_{tot}	<	0.5	%
Volume control range		typ.	75	dB
Signal handling		>	20	mV
Gain variation at V_B decreasing from 7 to 5 V	ΔG_v	typ.	3	dB

Data for use as play-back amplifier (measured at f= 1 kHz)

Voltage gain	G_v		64 ± 2	dB
Frequency response (see page 6)				
Distortion at $V_{o(rms)}$ = 0.5 V	d_{tot}	<	0.5	%
Gain variation at V_B decreasing from 7 to 5 V	ΔG_v	typ.	3	dB


7Z52382
frequency response curve of tape-recorder
pre-amplifier during recording
gain at 1kHz is 64dB
typ
ΔGv (dB)
20
15
10
5
0
−5
−10
10
2
5
10²
10³
10⁴
10⁵
f (Hz)


7Z52383
frequency response curve of tape-recorder
pre-amplifier during play-back
gain at 1kHz is 64dB
typ
ΔGv (dB)
20
15
10
5
0
−5
−10
10
2
5
10²
10³
10⁴
10⁵
f (Hz)

INTEGRATED MOST AMPLIFIER

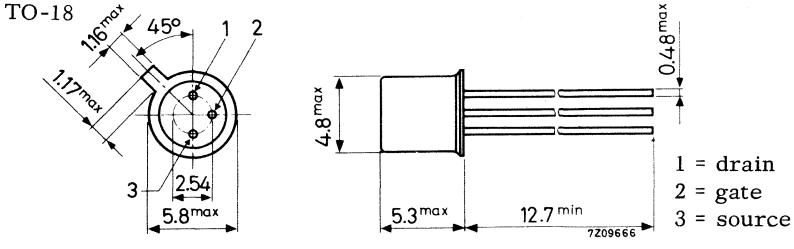
The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.
The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

QUICK REFERENCE DATA				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Drain current	$-I_D$	max.	25	mA
Gate-source voltage $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ.	11	V
Gate-source resistance $-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	>	100	GΩ
Transfer admittance at f = 1 kHz $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$\|y_{fs}\|$	typ.	75	$m\Omega^{-1}$

PACKAGE OUTLINE

Dimensions in mm

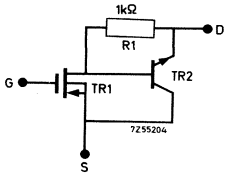
TO-18



Source connected to the case

Accessories available: 56246, 56263

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non repetitive peak gate-source voltage ($t \leq 10$ ms)	$-V_{GSM}$	max.	100	V
Current				
Drain current	$-I_D$	max.	25	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	200	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +125		°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0.5	°C/mW

CHARACTERISTICS T_j = 25 °C unless otherwise specified

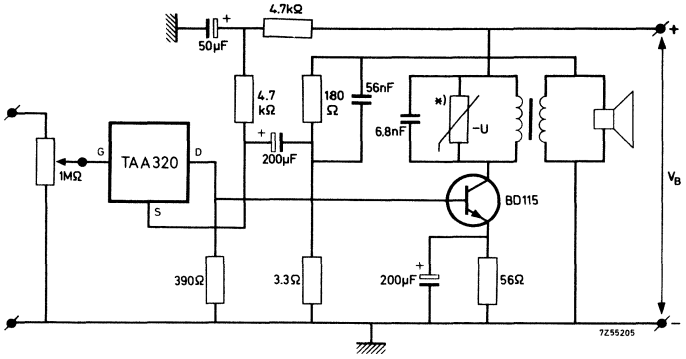
Drain current			
$-V_{DS}$ = 20 V; V_{GS} = 0	$-I_{DSS}$	typ. 5 < 1	nA μA
Gate-source voltage [1]			
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ. 11 9 to 14	V V
Gate-source resistance			
$-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	> 100	GΩ
Equivalent noise voltage			
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V B = 50 Hz to 15 kHz	v_n	typ. 25	μV
y parameters at f = 1 kHz			
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V			
Transfer admittance	$\|y_{fs}\|$	typ. 75 40 to 120	$m\Omega^{-1}$ $m\Omega^{-1}$
Input capacitance	C_{is}	typ. 8	pF
Feedback capacitance	$-C_{rs}$	typ. 1.5	pF
Output conductance	g_{os}	typ. 0.65	$m\Omega^{-1}$

NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

1) $-V_{GS}$ decreases about 6 mV/°C with increasing ambient temperature at a constant $-I_D$.

APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115



* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

Supply voltage	V_B	=	100	V
Collector current of BD115	I_C	typ.	50	mA
Drain current of TAA320	$-I_D$	typ.	9.5	mA
Primary d.c. resistance of output transformer			140	Ω
Primary inductance of output transformer			2.7	H
A.C. collector load for BD115			1.8	kΩ

Performance at f = 1 kHz; feedback = 16 dB

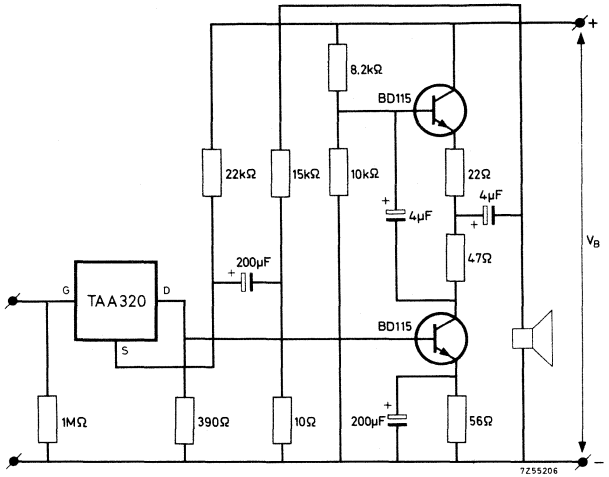
Output power at d_{tot} = 10% (on primary of the output transformer)	P_o	typ.	2.6	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	13.5	mV
Input voltage for P_o = 2 W	$V_{i(rms)}$	typ.	86	mV
Total distortion at P_o = 2 W	d_{tot}	typ.	3.6	%
Minimum frequency response (-3 dB)		60 Hz to 20		kHz
Signal-noise ratio at P_o = 2 W		typ.	73	dB

Mounting instruction for BD115

Proper continuous operation is ensured up to T_{amb} = 50 °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 cm^2 with a clamping washer of type 56218.
If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 cm^2.
Recommended diameter of hole in heatsink: 7.7 mm.

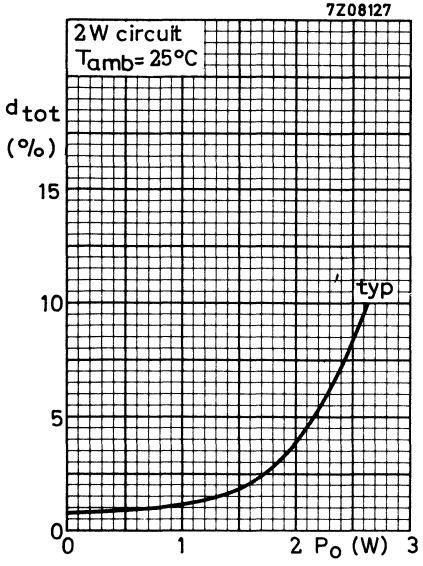
APPLICATION INFORMATION (continued)

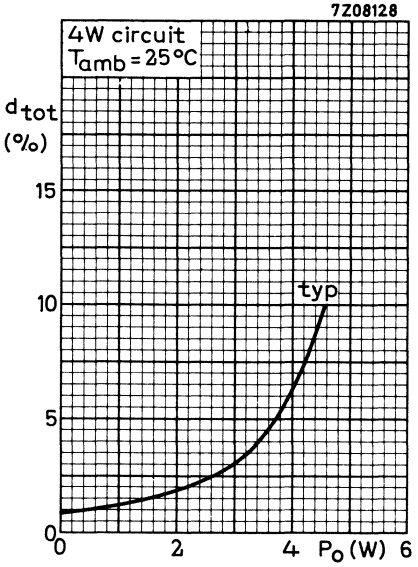
4 W audio amplifier with TAA320 and 2 transistors of type BD115.

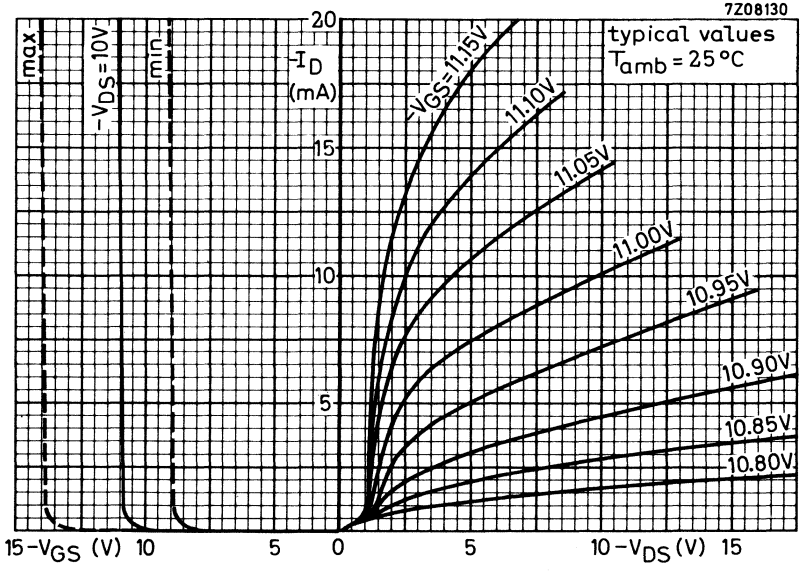


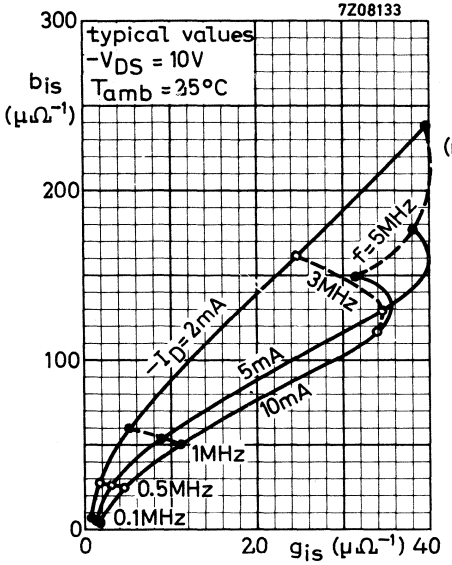
Supply voltage	V_B	=	200	V
Collector current of a BD115	I_C	typ.	52	mA
Drain current of TAA320	$-I_D$	typ.	8.6	mA
Performance at f = 1 kHz; feedback = 12 dB				
Output power at d_{tot} = 10%	P_o	typ.	4.5	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	7.5	mV
Input voltage for P_o = 4 W	$V_{i(rms)}$	typ.	67	mV
Total distortion at P_o = 4 W	d_{tot}	typ.	6	%
Minimum frequency response (−3 dB)		50 Hz to 20		kHz
Signal-noise ratio at P_o = 4 W		typ.	73	dB

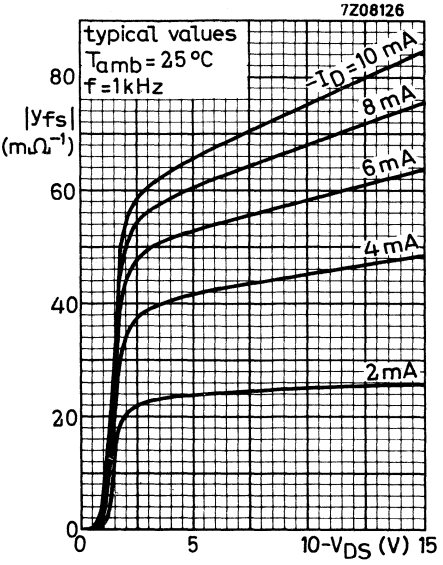
Mounting instruction for BD115 see page 4

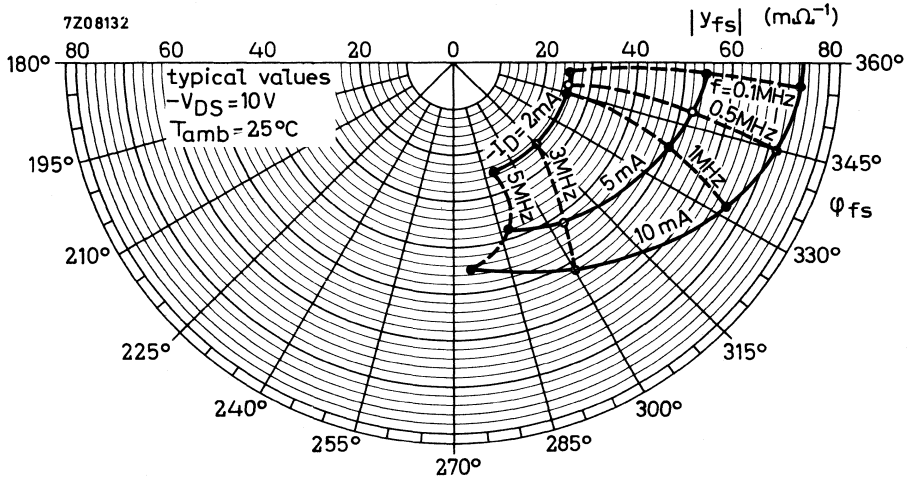

7Z08127
2W circuit
T_{amb} = 25 °C
d_{tot} (%)
15
10
5
0
typ
0
1
2
P_o (W)
3

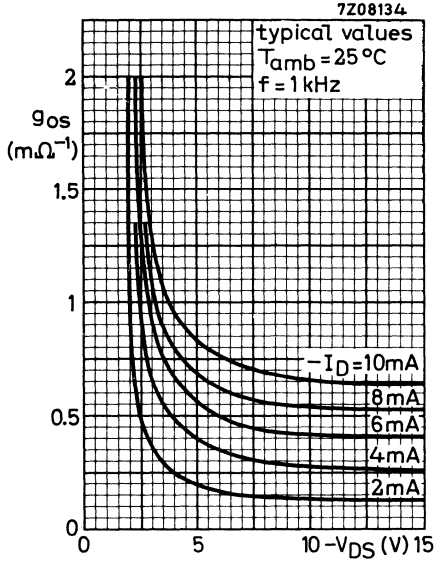

7Z08128
4W circuit
T_{amb} = 25 °C
d_{tot} (%)
15
10
5
0
typ
0
2
4
P_o (W)
6

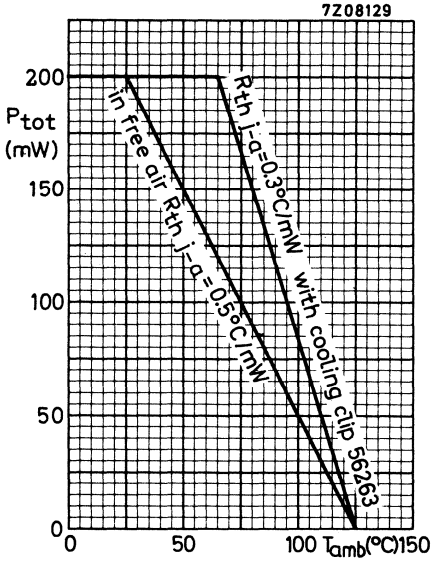

7Z08130
typical values
T_{amb} = 25 °C
max
min
$-V_{DS}$ = 10V
$-I_D$ (mA)
20
15
10
5
$-V_{GS}$ = 11.15V
11.10V
11.05V
11.00V
10.95V
10.90V
10.85V
10.80V
15 $-V_{GS}$ (V) 10
5
0
5
10 $-V_{DS}$ (V) 15

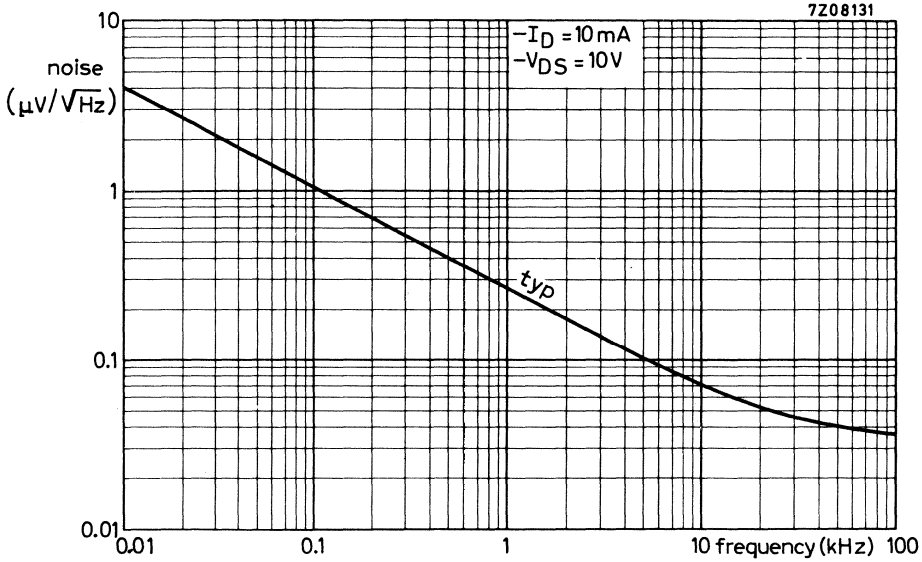

7Z08133
typical values
$-V_{DS}$ = 10V
T_{amb} = 25°C
b_{is} ($\mu\Omega^{-1}$)
300
200
100
0
0
20
g_{is} ($\mu\Omega^{-1}$) 40
$-I_D$=2mA
5mA
10mA
f=5MHz
3MHz
1MHz
0.5MHz
0.1MHz


7Z08126
typical values
T_{amb} = 25°C
f = 1kHz
$|y_{fs}|$ ($m\Omega^{-1}$)
80
60
40
20
0
0
5
10-V_{DS} (V) 15
$-I_D$=10 mA
8 mA
6 mA
4 mA
2mA


7Z08132
$|y_{fs}|$ ($m\Omega^{-1}$)
80
60
40
20
0
20
40
60
80
180°
195°
210°
225°
240°
255°
270°
285°
300°
315°
330°
345°
360°
φ_{fs}
typical values
$-V_{DS}$ = 10V
T_{amb} = 25°C
f=0.1MHz
0.5MHz
1MHz
3MHz
5MHz
$-I_D$=2mA
5mA
10 mA


7Z08134
typical values
T_{amb} = 25 °C
f = 1 kHz
g_{os} ($m\Omega^{-1}$)
2
1.5
1
0.5
0
$-I_D$ = 10 mA
8 mA
6 mA
4 mA
2 mA
0
5
10
$-V_{DS}$ (V)
15


7Z08129
P_{tot} (mW)
200
150
100
50
0
in free air Rth j-a = 0.5°C/mW
Rth j-a = 0.3°C/mW with cooling clip 56263
0
50
100
T_{amb} (°C)
150


7Z08131
noise
($\mu V/\sqrt{Hz}$)
10
1
0.1
0.01
$-I_D$ = 10 mA
$-V_{DS}$ = 10 V
typ
0.01
0.1
1
10
frequency (kHz)
100

WIDEBAND DIFFERENTIAL LIMITING AMPLIFIER

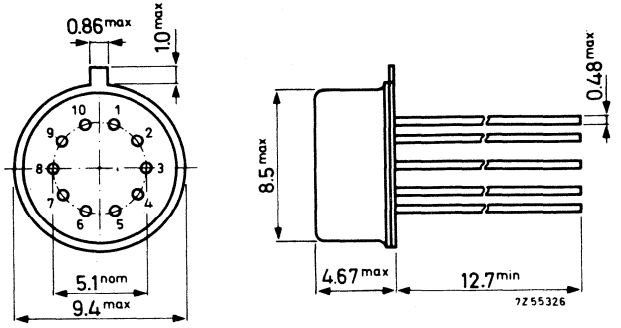
A monolithic integrated i.f. amplifier for f.m. Differential amplification with current driven long-tailed paires gives high a.m. rejection, making the amplifier suitable for use with very simple f.m. detectors. The TAA350 can be driven either symmetri cally or asymmetrically.

QUICK REFERENCE DATA		
Supply voltage	6	V
Frequency	5.5	MHz
Total current	typ. 20	mA
Voltage gain	typ. 80	dB
Input limiting voltage	typ. 100	μV
Frequency response (−3 dB)	typ. 12	MHz
Output impedance	typ. 75	Ω

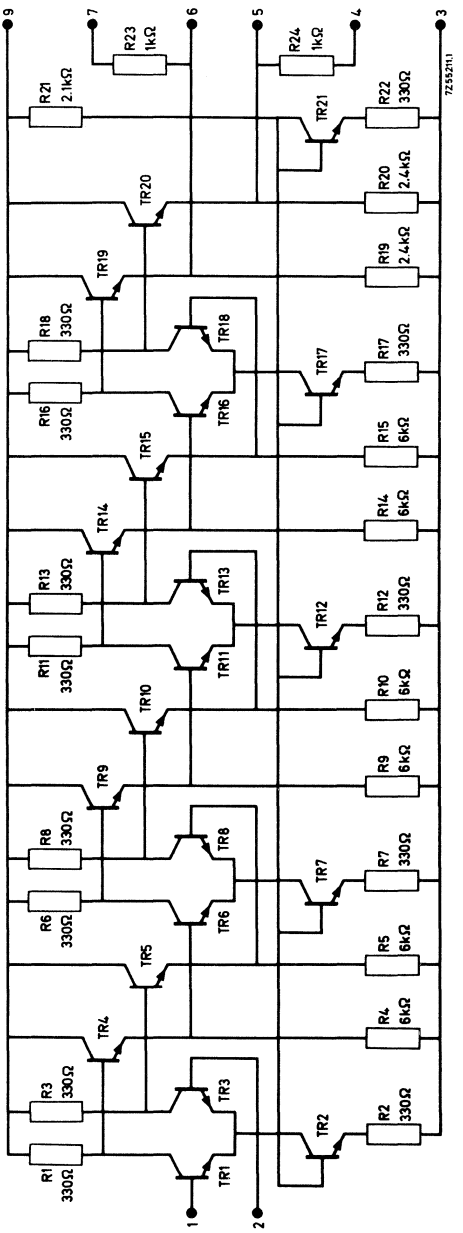
PACKAGE OUTLINE

Dimensions in mm

TO-74; reduced height



CIRCUIT DIAGRAM



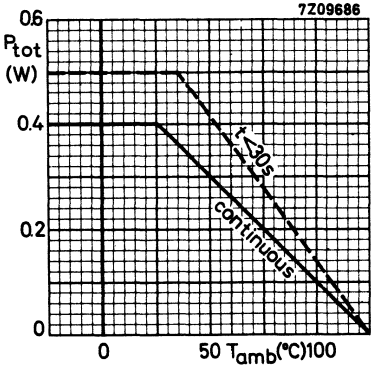
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages with respect to pin 3

Pin No.1 when $V_{2-3} = V_{1-3} \leq V_{9-3}$	V_{1-3}	0 to +10	V
Pin No.2 when $V_{1-3} = V_{2-3} \leq V_{9-3}$	V_{2-3}	0 to +10	V
Pin No.4 (do not apply an external voltage source)	V_{4-3}	0 to +10	V
Pin No.5 when at $\lvert I_5 \rvert < 20$ mA; $V_{5-3} \leq V_{9-3}$	V_{5-3}	0 to +10	V
Pin No.6 when at $\lvert I_6 \rvert < 20$ mA; $V_{6-3} \leq V_{9-3}$	V_{6-3}	0 to +10	V
Pin No.7 (do not apply an external voltage source)	V_{7-3}	0 to +10	V
Pin No.9 (with lower d.c. potential on all other terminals)	V_{9-3}	0 to +10	V

Do not connect pins 8 and 10, except to earth.
The maximum signal voltage between pins 1 and 2 is 6 V.

Total power dissipation



Temperatures

Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +125	°C

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

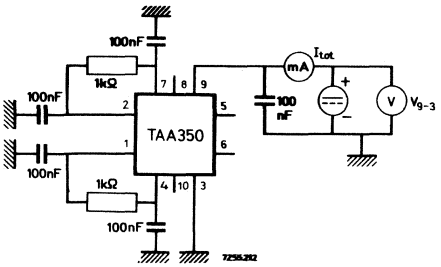
Because the TAA350 has a low ohmic output impendance and is usually driven by a bandpass or parallel tuned filter, the characteristics are described in terms of four pole hybrid k parameters.

The four-pole equations are:

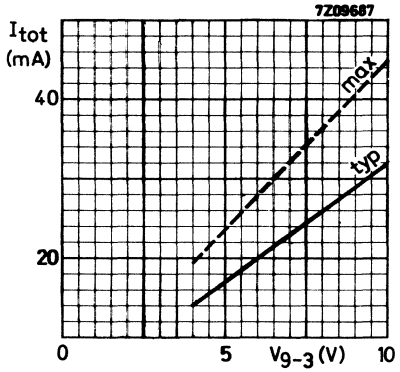
$$I_i = k_i V_i + k_r I_o$$

$$V_o = k_f V_i + k_o I_o$$

Total current (d.c.) [1])



Test circuit for measuring I_{tot} = (V_{9-3})



k parameters (see pages 6 to 9)

f = 5.5 MHz; V_{9-3} = 6 V

Input conductance (input pin 2)	g_i	typ.	400	$\mu\Omega^{-1}$
Input susceptance (input pin 2)	b_i	typ.	550	$\mu\Omega^{-1}$
Reverse current transfer ratio (output pin 6, input pin 2) [2])	$\lvert k_r \rvert$	typ.	−90	dB
Small signal voltage gain (input pin 2, output pin 6)	$\lvert k_f \rvert$	typ.	67	dB
Real part of output impedance (output pin 6)	$Re(k_o)$	typ.	75	Ω
Imaginary part of output impedance (output pin 6)	$Im(k_o)$	typ.	20	Ω

f = 10.7 MHz; V_{9-3} = 6 V

Reverse current transfer ratio (output pin 6, input 2) [2])	$\lvert k_r \rvert$	typ.	−80	dB
Small signal voltage gain (input pin 2, output pin 6)	$\lvert k_f \rvert$	typ.	65	dB

Input limiting voltage (see pp 5 and 8) [3])

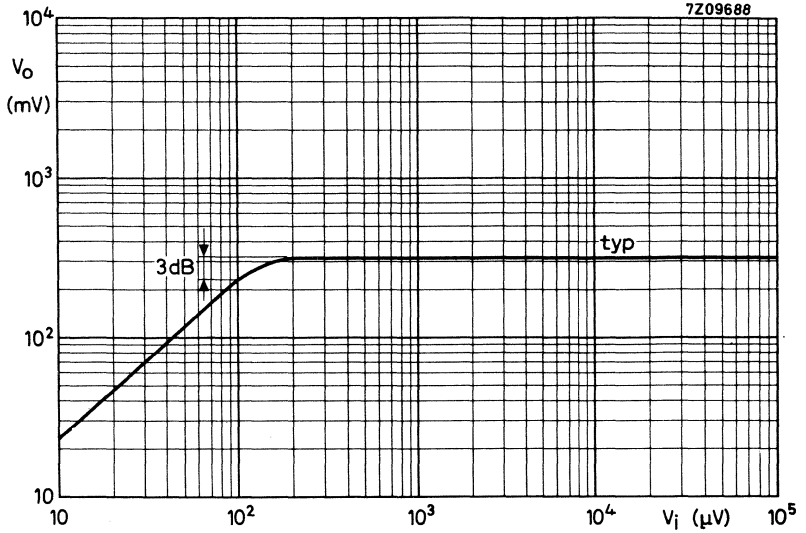
f = 5.5 MHz; V_{9-3} = 6 V	$V_{i\,lim}$	typ.	100	μV

[1]) The power dissipation is obtained from $V_{9-3} \times I_{tot}$.

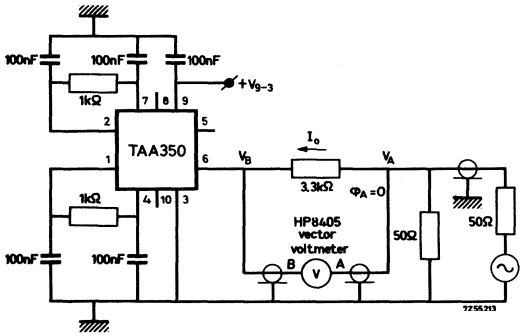
[2]) The output is considered open for $R_L \geq 10$ kΩ and $C_L \leq 10$ pF.

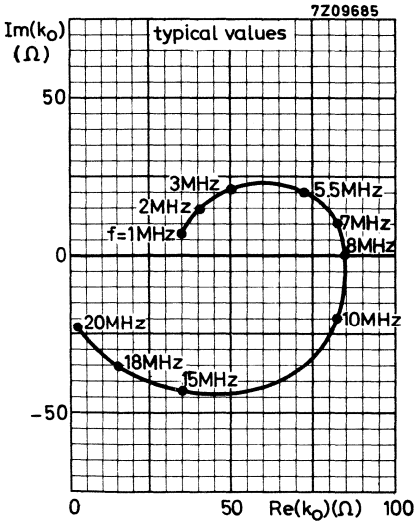
[3]) $V_{i\,lim}$ is defined as the input signal voltage which reduces the output voltage 3 dB from its max. level (see also page 5).

CHARACTERISTICS (continued)



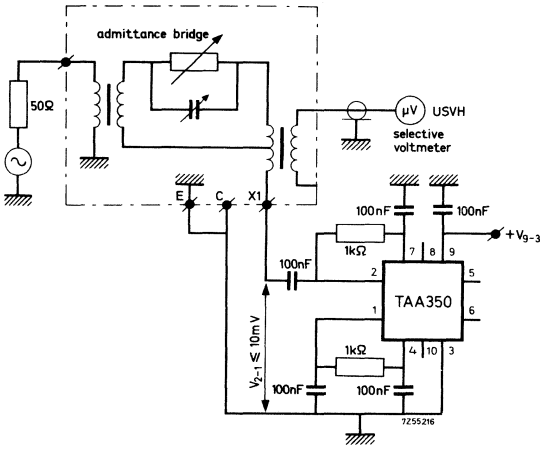
Test circuit for measuring the output characteristic

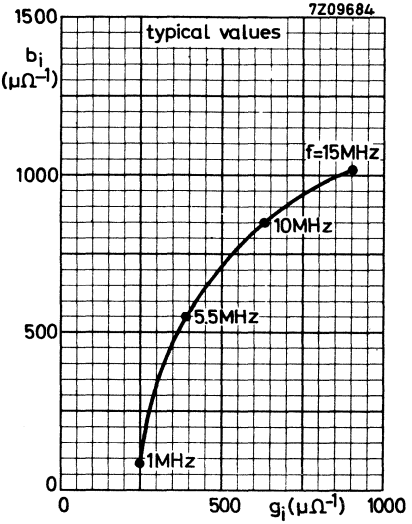




CHARACTERISTICS (continued)

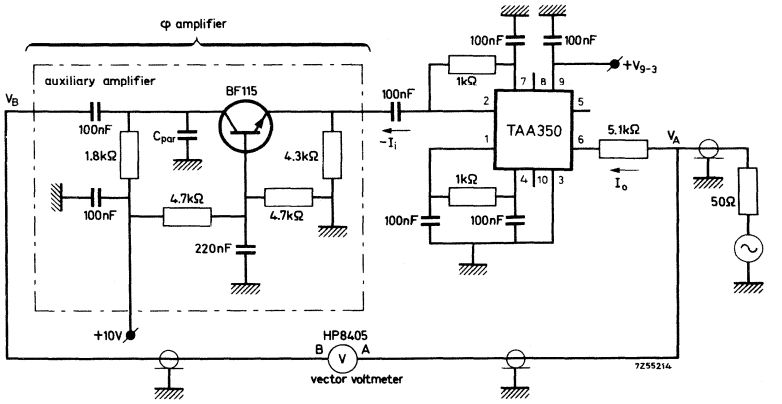
Test circuit for measuring the input characteristic

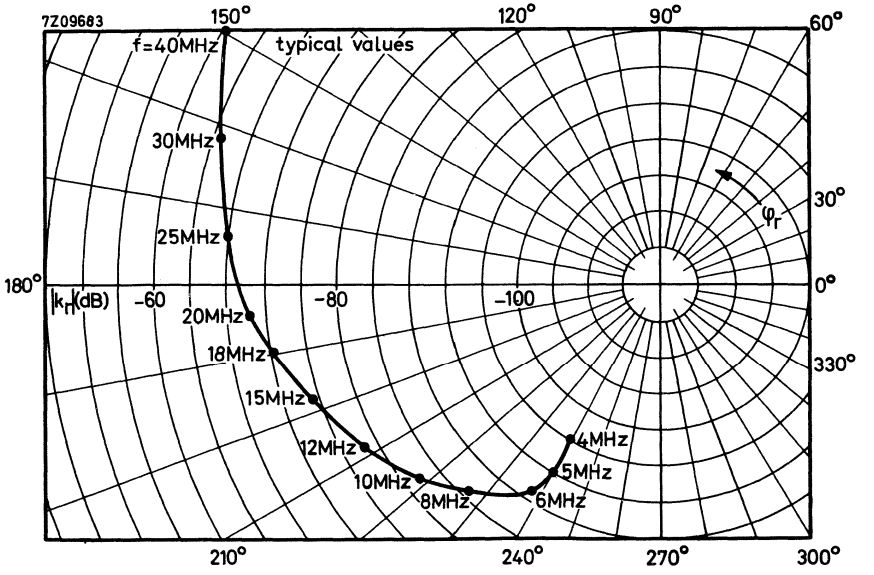




CHARACTERISTICS (continued)

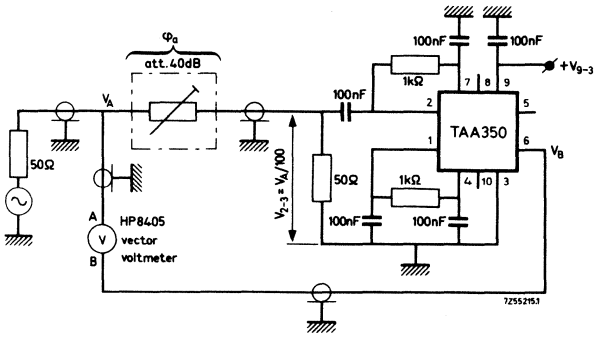
Test circuit for measuring the reverse current transfer ratio





CHARACTERISTICS (continued)

Test circuit for measuring the small signal voltage gain and the input limiting voltage



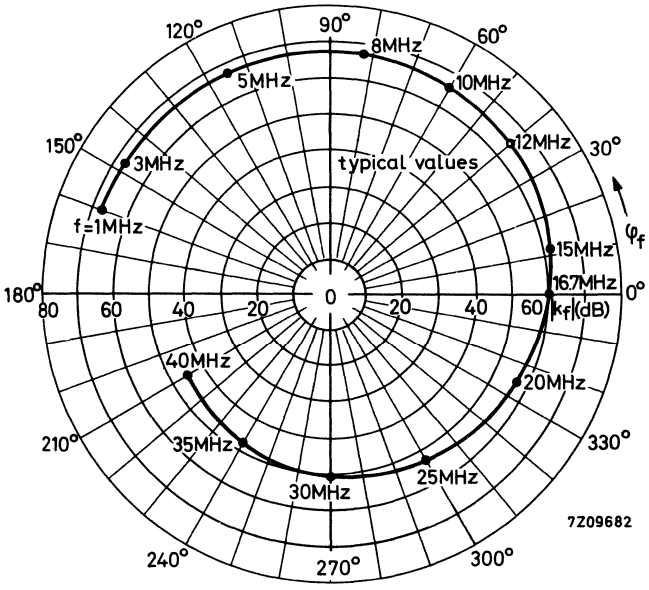
$\overline{k_f} = |k_f| . e^{j\varphi f}$, where

$|k_f| = (20 \log \frac{V_B}{V_A} + 40)$ dB; $\varphi_f = \varphi_{AB} - \varphi_a$

φ_{AB} = phase angle between V_A and V_B

$V_{i\ lim} = V_{Bmax} - 3$ dB

To find V_{Bmax} raise V_A until V_B remains constant



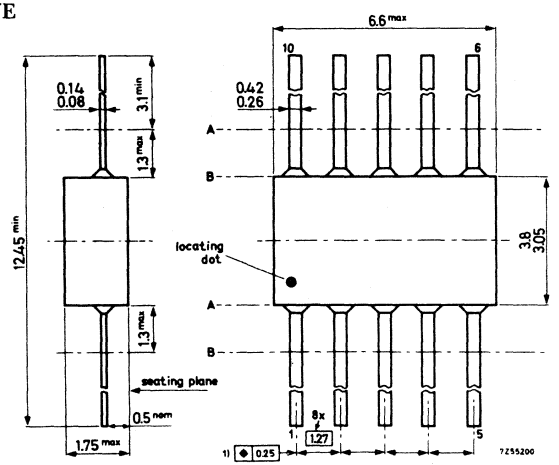
HEARING-AID AMPLIFIER

Integrated monolithic a.f. amplifier for use in hearing aids. The collector current of the class A output transistor can be determined externally, making the circuit suitable for a wide range of output powers at a low current consumption. Provision is made for the use of peak-clipping and frequency compensation circuits, and special measures have been taken to minimize the influence of temperature and supply voltage variations.

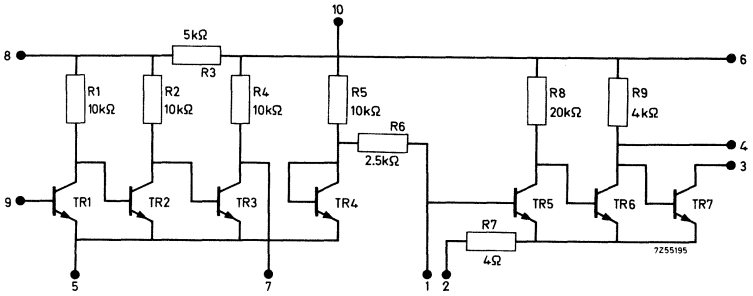
QUICK REFERENCE DATA				
Supply voltage	V_B	nom.	1.3	V
Transducer gain	G_{tr}	typ.	90	dB
Output power at d_{tot} = 10%	P_o	typ.	1.5	mW
Saturation voltage of TR7 at I_C = 5 mA; V_{6-2} = 1.3 V	V_{3-2sat}	<	300	mV
Current consumption of all stages except output stage	I	typ.	0.35	mA
Noise figure	F	typ.	3	dB

PACKAGE OUTLINE

TO-89



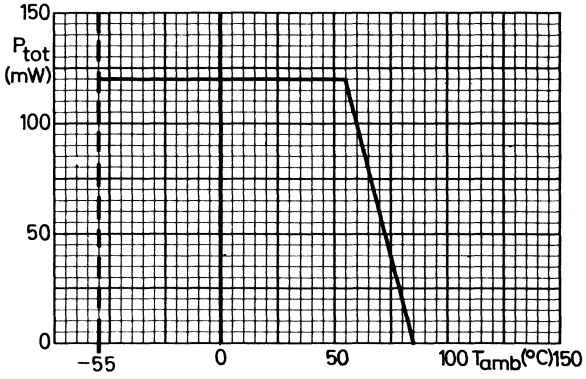
CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages	V_{6-2}	max.	5	V
	V_{3-2}	max.	5	V
	V_{8-2}	max.	5	V
	V_{5-9}	max.	5	V
Currents	I_2	max.	20	mA
	I_3	max.	20	mA

Maximum allowable total power dissipation versus ambient temperature



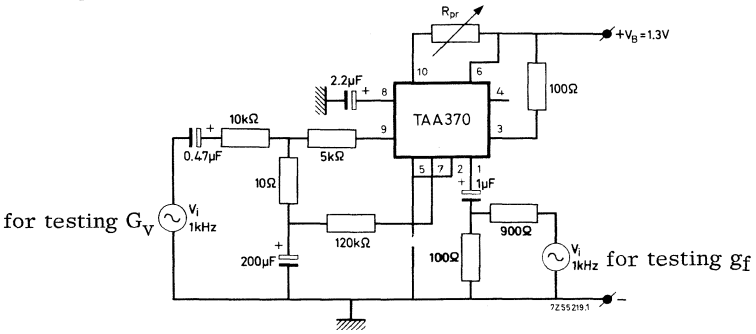
Temperatures

Storage temperature	T_{stg}	−55 to +85	°C
Operating ambient temperature	T_{amb}	−55 to +85	°C

CHARACTERISTICS (see also test circuit) T_{amb} = 25 °C

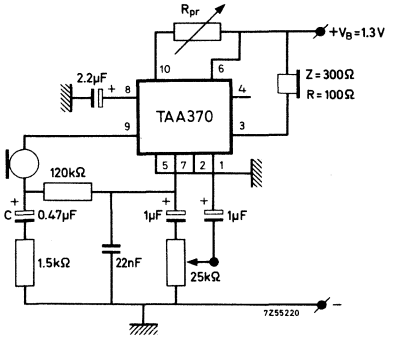
Supply voltage	V_B	nom.	1.3	V
Voltage gain of first 3 transistors (pin 9 to 7)	G_v	>	60	dB
Transconductance of last 3 transistors (pin 1 to 3)	g_f	200 to 280		$m\Omega^{-1}$
Saturation voltage of last transistor (TR7) at I_C = 5 mA; V_{6-2} = 1.3 V	$V_{3-2\,sat}$	<	300	mV
Current consumption of all stages except output stage	I	typ.	0.35	mA
		<	0.5	mA
Noise figure R_S = 5 kΩ; B = 400 to 3200 Hz	F	typ.	3	dB
		<	6	dB

Test circuit



APPLICATION INFORMATION

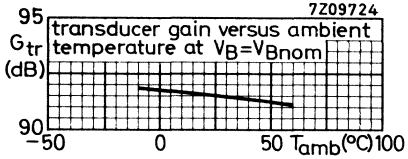
The TAA370 in a 1.5 mW amplifier

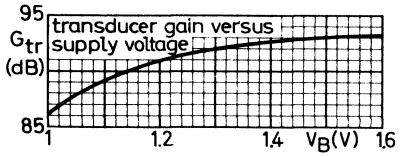


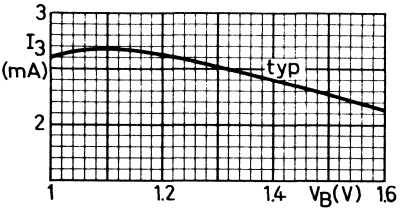
I_3 = 2.5 mA

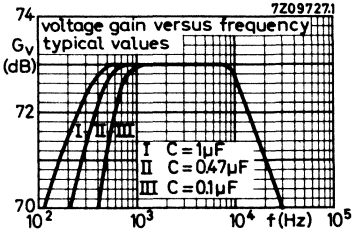
I_{tot} = 2.85 mA

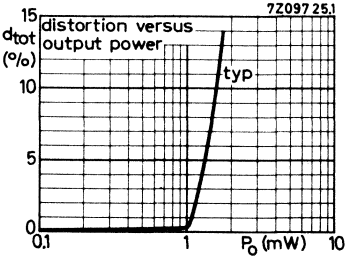
R_{pr} = 4 kΩ











LOW FREQUENCY AMPLIFIER

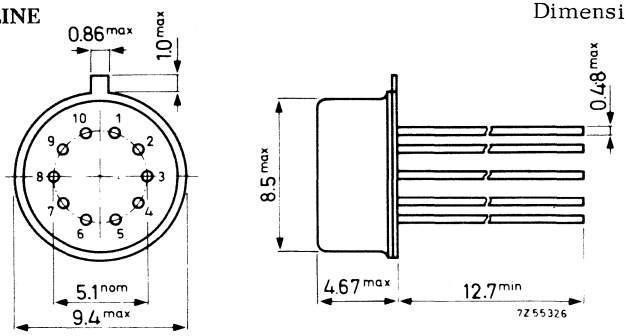
The TAA435 is a silicon monolithic integrated a.f. preamplifier and driver stage. Combined with a complementary output stage an output power of 4 W can be achieved.

QUICK REFERENCE DATA				
with AD161/AD162 output stage				
Supply voltage	V_B	nom.	14	V
Ambient temperature	T_{amb}	nom.	25	°C
Voltage gain	G_v	typ.	80	dB
Output power at d_{tot} < 10%	P_o	>	4	W
Noise figure at B = 60 Hz to 10 kHz	F	typ.	6	dB

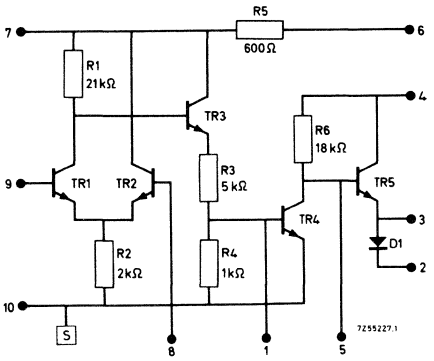
PACKAGE OUTLINE

TO-74
reduced height

Dimensions in mm



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

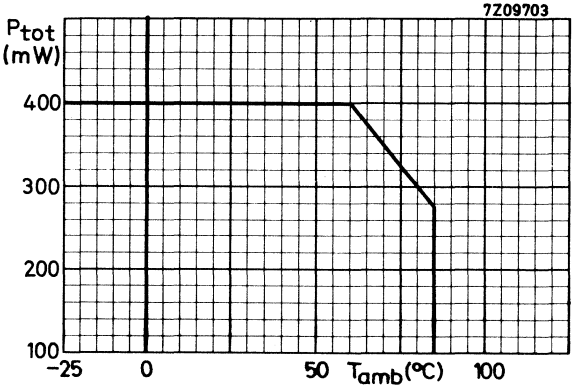
V_{6-10}	max.	18	V
$-V_{9-10}$	max.	5	V
V_{4-10}	max.	24	V
V_{3-10}	max.	20	V

Supply current

I_4	max.	70	mA

Total power dissipation

Maximum allowable total power dissipation versus ambient temperature.



Temperatures

Operating ambient temperature	T_{amb}	−25 to +85	°C
Storage temperature	T_{stg}	−35 to +125	°C

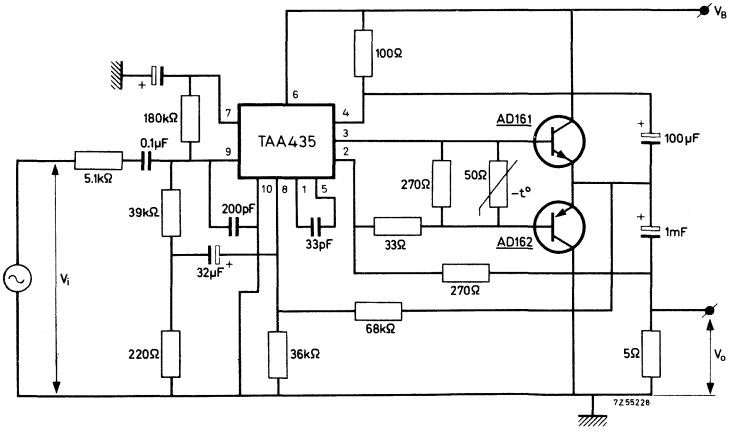
CHARACTERISTICS at V_B = 10 to 18 V; T_{amb} = 25 °C

Forward voltage at $-I_2$ = 30 mA	V_{3-2}	typ.	0.8	V
Collector-emitter voltage at I_4 = 50 mA	V_{4-3}	<	3.5	V

CHARACTERISTICS at V_B = 14 V; T_{amb} = 25 °C (measured in circuit below)

Voltage gain at f = 1 kHz; without feedback	G_v	typ.	80	dB
with feedback	G_v	typ.	50	dB
Input impedance at f = 1 kHz	$\|Z_{9-10}\|$	>	70	kΩ
Noise figure at B = 60 Hz to 10 kHz	F	typ.	6	dB
Cut-off frequency (−3 dB)	f_c	>	10	kHz
Output power at f = 1 kHz; d_{tot} = 10%	P_o	>	4	W
Total distortion at f = 1 kHz; P_o = 1 W	d_{tot}	<	1	%
Input signal for P_o = 4 W	$V_{i(rms)}$	typ.	15	mV

Test circuit:



FM CHANNEL AMPLIFIER

The TAA450 is a monolithic integrated circuit containing an i.f. amplifier with limiting characteristics for use up to frequencies of 10 MHz, a ratio detector and an l.f. amplifier with connections brought out for remote volume control.

QUICK REFERENCE DATA

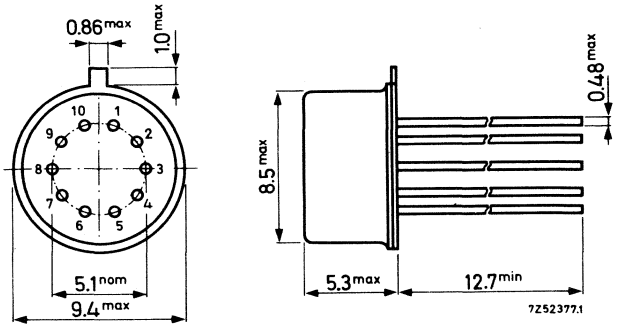
Operating characteristics of i.f. amplifier at f = 5.5 MHz
Supply voltage V_B = 7.5 V; T_{amb} = 25 °C

Voltage gain	G_v	typ.	69	dB
Start of limiting	V_i	typ.	300	μV

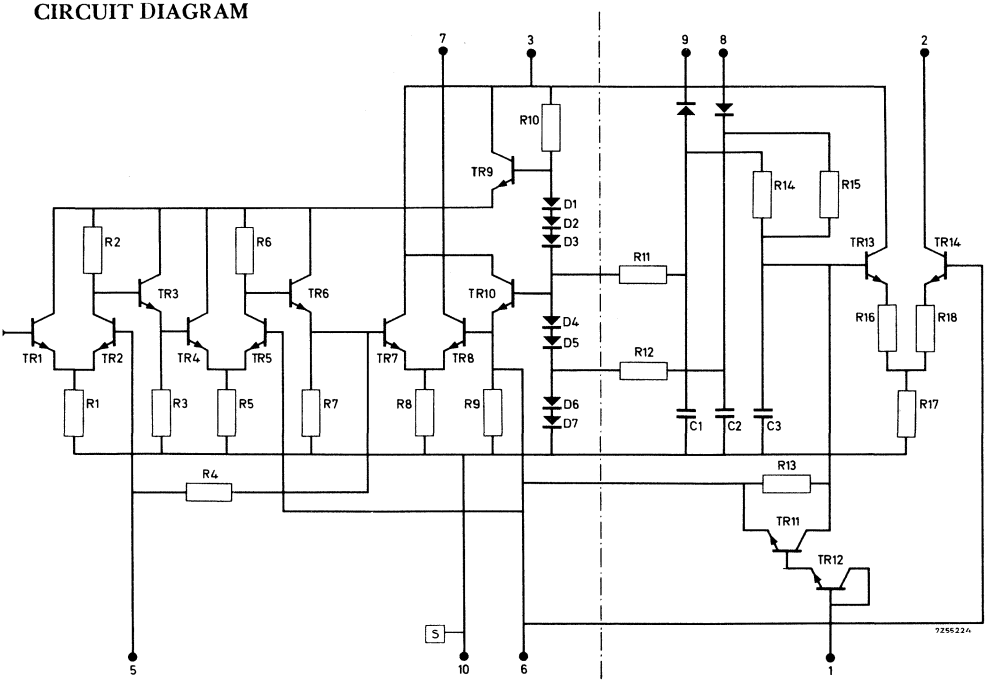
PACKAGE OUTLINE

Dimensions in mm

TO-74; reduced height



CIRCUIT DIAGRAM



RATINGS (Limiting values in accordance with the Absolute Maximum System (IEC 134)

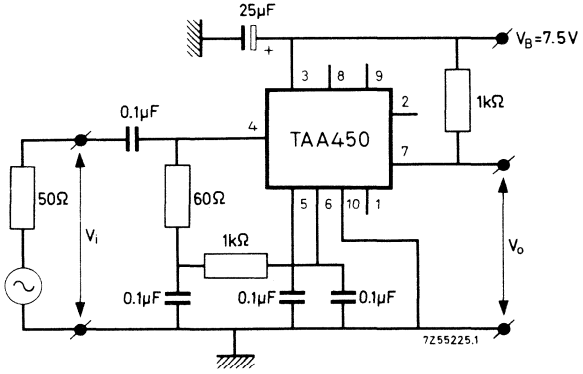
Supply voltage (d.c.) i.f. amplifier	$V_7 = V_3$	max. 12	V
a.f. amplifier	V_2	max. 18	V [1]
Total power dissipation	P_{tot}	max. 380	mW
Storage temperature	T_{stg}	−20 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +60	°C

[1] During warming-up in tube receivers this value may be exceeded up to 30 V.

CHARACTERISTICS for i.f. amplifier part at V_B = 7.5 V; T_{amb} = 25 °C

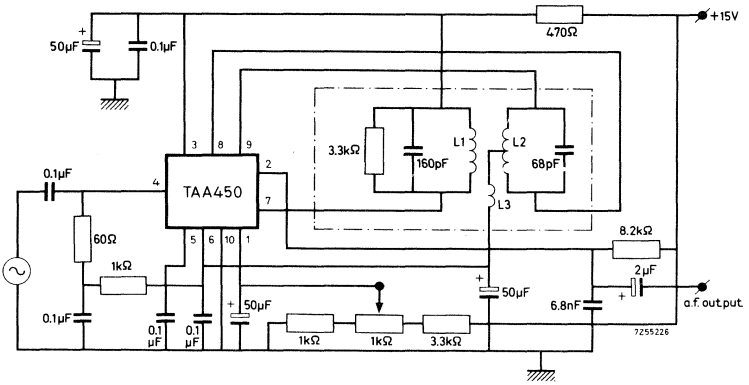
Voltage gain				
V_i = 100 μV: f = 1 MHz	G_v	typ.	71	dB
V_i = 100 μV: f = 4.5 MHz	G_v	typ.	69	dB
V_i = 100 μV: f = 5.5 MHz	G_v	>	66	dB
		typ.	69	dB
Start of limiting at f = 5.5 MHz	V_i	typ.	300	μV
Output current (peak to peak) at V_i = 5 mV	$I_{7(p-p)}$	typ.	2.8	mA
Input resistance	R_i	>	2.5	kΩ
Input capacitance	C_i	typ.	7	pF
		<	10	pF
Output resistance	R_o	>	10	kΩ
Output capacitance	C_o	typ.	4	pF
		<	6	pF
Total current	I_B	typ.	18	mA
		<	22	mA

Test circuit



APPLICATION INFORMATION

Circuit with the TAA450 in an i.f.-l.f. amplifier of a television receiver.



Primary: frame core AP3014/02
Secondary: no frame core
L1 = 19 turns 0.12 mm stranded Cu wire
L2 = 2 x 17 turns 0.12 mm stranded Cu wire; bifilarly wounded
L3 = 14 turns 0.12 mm stranded Cu wire; bifilarly wounded with L1
Top-top distance of frequency response curve: ≥ 250 kHz

Intermediate frequency	f_0	= 5.5 MHz
Frequency deviation	Δf	$\pm$ 15 kHz
Modulation frequency	f_m	= 400 Hz
Ambient temperature	T_{amb}	= 25 °C

Start of limiting		V_i	typ.	300	µV
I.F. output voltage at pin 7 with $V_i \geq 300$ µV		V_7	typ.	1.2	V
L.F. output voltage at $V_i \geq 300$ µV		$V_{o(rms)}$	typ.	600	mV
A.M. suppression					
f_m = 1 kHz; m = 0.3; $V_i \geq 2$ mV			$\geq$	42	dB
Volume control range		ΔV_o	$\geq$	30	dB
Distortion at $\Delta f \pm 15$ kHz	without volume control	d	typ.	0.015	
	with volume control	d	typ.	0.02	
$\Delta f \pm 50$ kHz	without volume control	d	typ.	0.025	
	with volume control	d	typ.	0.05	
Supply current l.f. part (pin 2)		I_{P_2}	typ.	1	mA

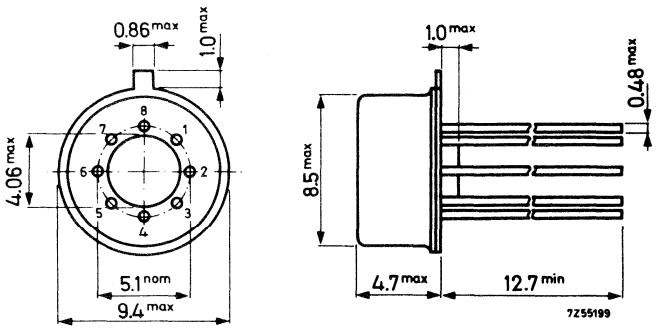
OPERATIONAL AMPLIFIER

The TAA521 is a silicon monolithic integrated operational amplifier in an XA8 (TO-99) metal envelope.
It has a high gain, low offset, high input impedance, high output voltage swing and low power dissipation. The operating temperature range is 0 to +70 °C.

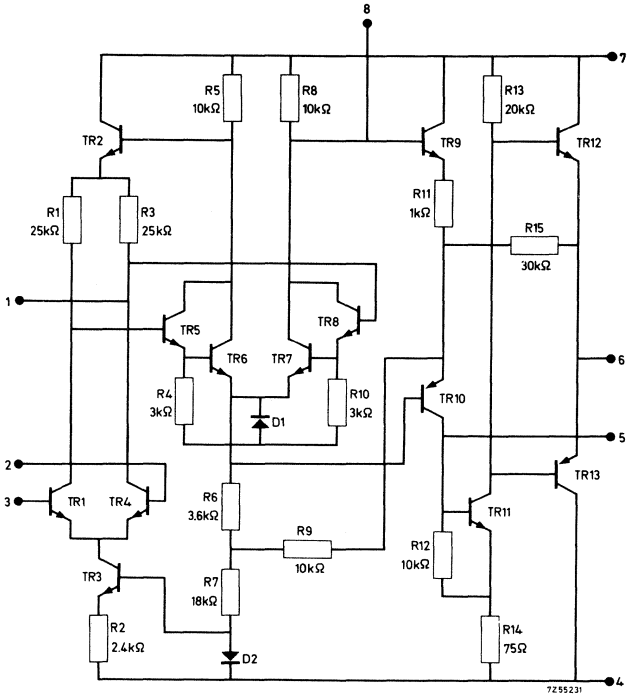
QUICK REFERENCE DATA				
Positive supply voltage	V_P		15	V
Negative supply voltage	$-V_N$		15	V
Characteristics at T_{amb} = 25 °C				
Voltage gain	G_V	typ.	45000	
Common mode rejection ratio	CMRR	typ.	90	dB
Input offset voltage drift; R_S = 50 Ω	$\frac{\Delta V_{io}}{\Delta T}$	typ.	6	μV/°C
$R_S \leq 10$ kΩ	$\frac{\Delta V_{io}}{\Delta T}$	typ.	10	μV/°C
Differential input resistance	R_i	typ.	250	kΩ
Peak output voltage swing at $R_L \geq 10$ kΩ	V_{OM}	typ.	±14	V
Power dissipation	P_{tot}	typ.	80	mW

PACKAGE OUTLINE Dimensions in mm

TO-99



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Positive supply voltage	V_P	max.	18	V
Negative supply voltage	$-V_N$	max.	18	V
Common mode voltage	V_i	max.	±10	V
Differential mode voltage	V_{2-3}	max.	±5	V
Power dissipation up to T_{case} = 70 °C	P_{tot}	max.	250	mW
Output short circuit duration (T_{amb} = 25 °C)	t	max.	5	s
Temperatures				
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

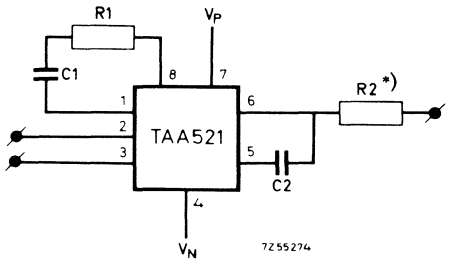
CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 25°C unless otherwise specified

Voltage gain; $R_L \geq 2$ kΩ; $V_O = \pm 10$ V	G_v	>	15000	
		typ.	45000	
Input offset voltage; $R_S \leq 10$ kΩ				
$V_P = -V_N$ = 9 to 15 V	V_{io}	typ.	2.0	mV
		<	7.5	mV
Input bias current	I_i	typ.	0.3	μA
		<	1.5	μA
Input offset current	I_{io}	typ.	0.1	μA
		<	0.5	μA
Common mode rejection ratio; $R_S \leq 10$ kΩ	CMRR	>	65	dB
		typ.	90	dB
Input voltage range	V_i	>	±8.0	V
		typ.	±10	V
Differential input resistance	R_i	>	50	kΩ
		typ.	250	kΩ
Output resistance	R_o	typ.	150	Ω
Supply voltage rejection ratio; $R_S \leq 10$ kΩ	SVRR	typ.	25	μV/V
		<	200	μV/V
Peak output voltage swing at $R_L \geq 10$ kΩ	V_{OM}	>	±12	V
		typ.	±14	V
$R_L \geq 2$ kΩ	V_{OM}	>	±10	V
		typ.	±13	V
Power dissipation at $V_O = 0$	P_{tot}	typ.	80	mW
		<	200	mW

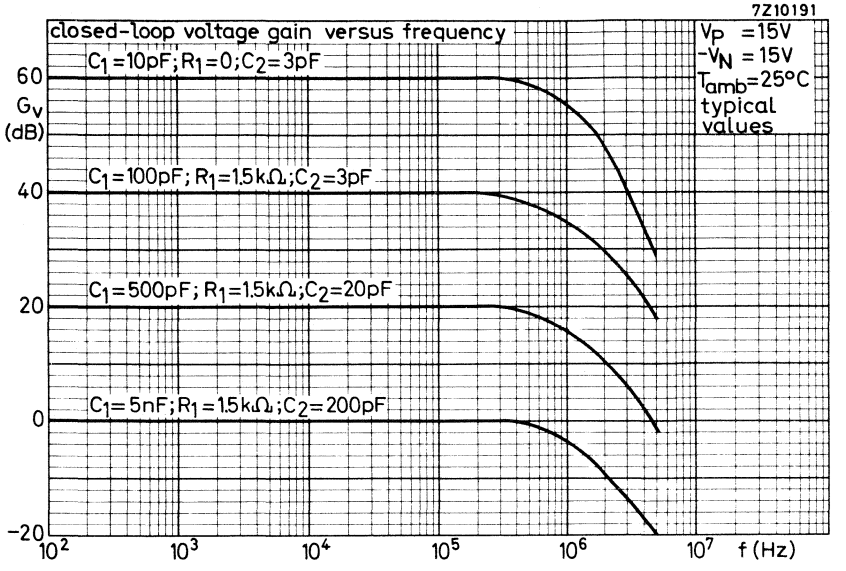
CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 0 to +70 °C unless otherwise specified

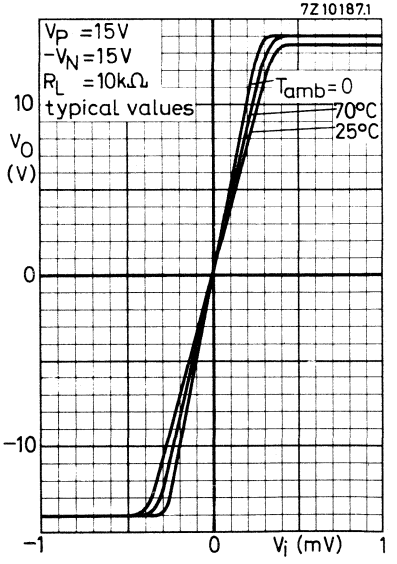
Voltage gain; $R_L \geq 2$ kΩ; $V_o = \pm 10$ V	G_v	>	12000	
Input offset voltage; $R_S \leq 10$ kΩ; $V_P = -V_N$ = 9 to 15 V	V_{io}	<	10	mV
Input offset voltage drift; R_S = 50 Ω	$\frac{\Delta V_{io}}{\Delta T}$	typ.	6	μV/°C
$R_S \leq 10$ kΩ	$\frac{\Delta V_{io}}{\Delta T}$	typ.	10	μV/°C
Input bias current	I_i	<	2	μA
Input offset current	I_{io}	<	0.75	μA

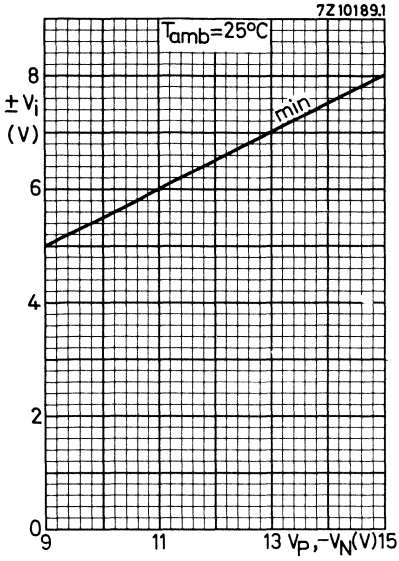
Frequency compensation circuit :

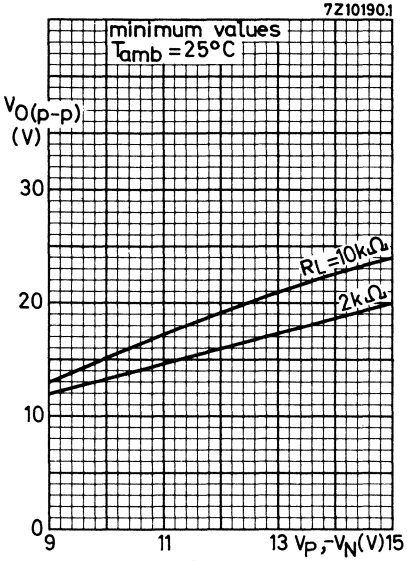


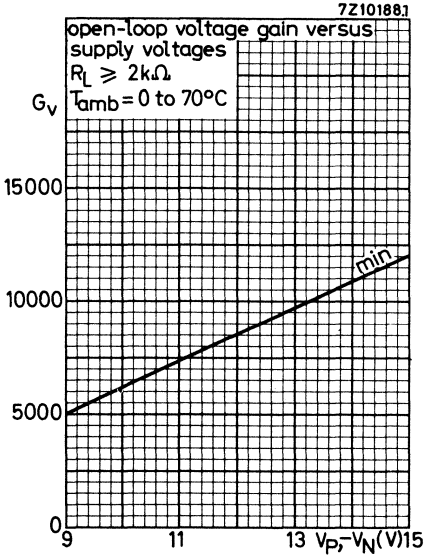
*) For operation with a capacitive load use R2 = 50 Ω.


7Z10191
closed-loop voltage gain versus frequency
C1 =10pF; R1 =0; C2 =3pF
C1 =100pF; R1 =1.5kΩ; C2 =3pF
C1 =500pF; R1 =1.5kΩ; C2 =20pF
C1 =5nF; R1 =1.5kΩ; C2 =200pF
VP =15V
-VN =15V
Tamb =25°C
typical values
Gv (dB)
60
40
20
0
-20
10^2
10^3
10^4
10^5
10^6
10^7
f (Hz)


7Z10187.1
VP =15V
-VN =15V
RL =10kΩ
typical values
Tamb =0
70°C
25°C
VO (V)
10
0
-10
-1
0
Vi (mV)
1


7Z10189.1
Tamb=25°C
min
±Vi (V)
8
6
4
2
0
9
11
13
VP,-VN(V)15


7Z10190.1
minimum values
Tamb=25°C
VO(p-p) (V)
30
20
10
0
RL=10kΩ
2kΩ
9
11
13
VP,-VN(V)15


7Z10188.1
open-loop voltage gain versus supply voltages
RL ≥ 2kΩ
Tamb=0 to 70°C
Gv
15000
10000
5000
0
min
9
11
13
VP,-VN(V)15

OPERATIONAL AMPLIFIER

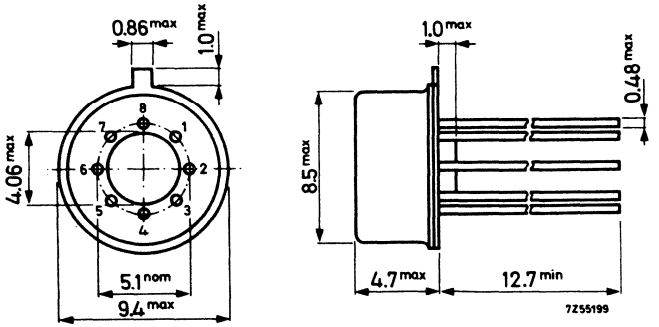
The TAA522 is a silicon monolithic integrated operational amplifier in an XA8 (TO-99) metal envelope. It has a high gain, low offset, high input impedance, high output voltage swing and low power dissipation. The operating temperature range is −55 to +125 °C.

QUICK REFERENCE DATA				
Positive supply voltage	V_P		15	V
Negative supply voltage	$-V_N$		15	V
Characteristics at T_{amb} = −55 to +125 °C				
Voltage gain	G_v	typ.	45000	
Common mode rejection ratio	CMRR	typ.	90	dB
Input offset voltage drift; R_S = 50 Ω	$\frac{\Delta V_{io}}{\Delta T}$	typ.	3	μV/°C
$R_S \leq 10$ kΩ	$\frac{\Delta V_{io}}{\Delta T}$	typ.	6	μV/°C
Differential input resistance	R_i	typ.	100	kΩ
Peak output voltage swing at $R_L \geq 10$ kΩ	V_{OM}	typ.	±14	V

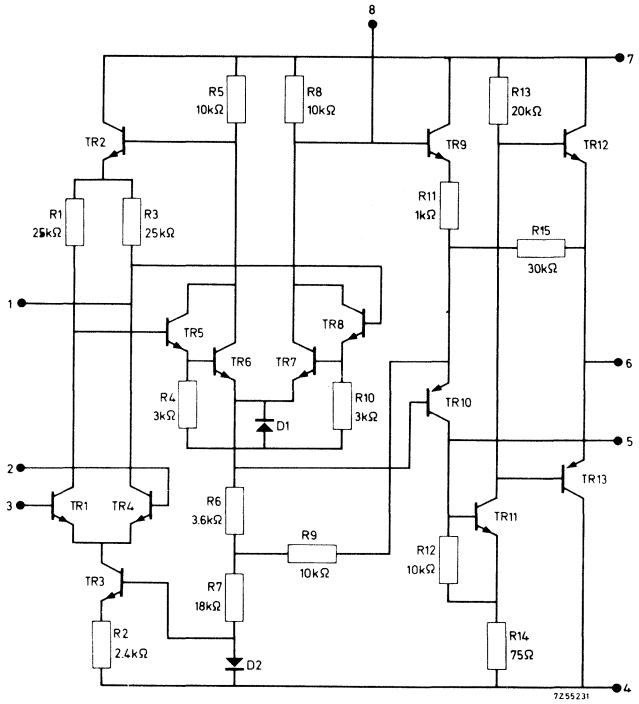
PACKAGE OUTLINE

Dimensions in mm

TO-99



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Positive supply voltage	V_P	max.	18	V
Negative supply voltage	$-V_N$	max.	18	V
Common mode voltage	V_i	max.	±10	V
Differential mode voltage	V_{2-3}	max.	±5	V
Power dissipation up to T_{case} = 125 °C [1])	P_{tot}	max.	300	mW
Output short circuit duration (T_{amb} = 25 °C)	t	max.	5	s
Temperatures				
Operating ambient temperature	T_{amb}	−55 to +125		°C
Storage temperature	T_{stg}	−65 to +150		°C

CHARACTERISTICS at $V_P = -V_N$ = 9 to 15 V; T_{amb} = 25 °C unless otherwise specified

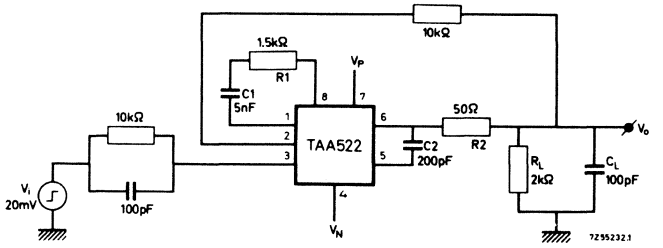
Input offset voltage; $R_S \leq 10$ kΩ	V_{io}	typ. <	1.0 5.0	mV mV
Input bias current	I_i	typ. <	0.2 0.5	μA μA
Input offset current	I_{io}	typ. <	50 200	nA nA
Differential input resistance	R_i	> typ.	150 400	kΩ kΩ
Output resistance	R_o	typ.	150	Ω
Power dissipation at V_O = 0; $V_P = -V_N$ = 15 V	P_{tot}	typ. <	80 165	mW mW
Transient reponse (see also test circuit on page 4)				
Rise time	t_r	typ. <	0.3 1.5	μs μs
Overshoot	$\frac{\Delta V}{V_o}$	typ. <	10 30	% %

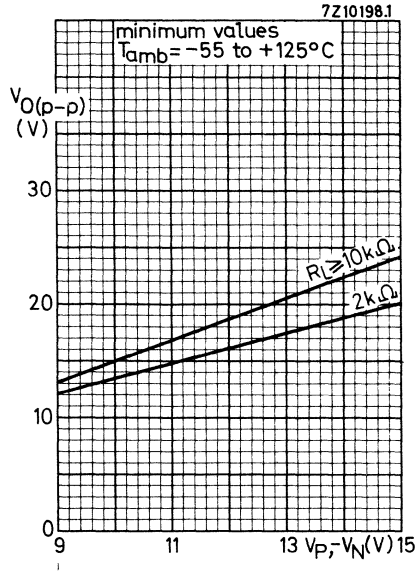
[1]) Rating applies to case temperatures up to 125 °C; derate linearly at 5.5 mW/°C for ambient temperatures above 95 °C.

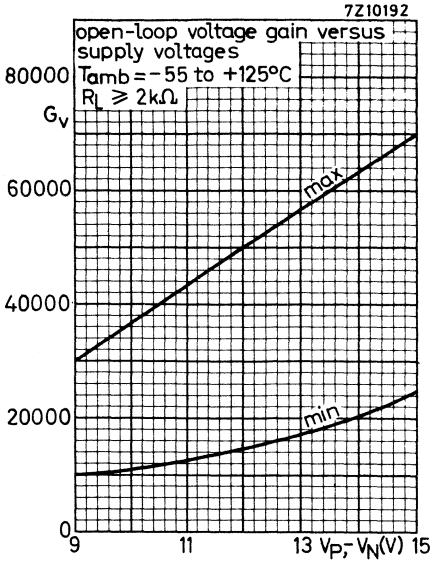
CHARACTERISTICS at $V_P = -V_N = 9$ to 15 V; $T_{amb} = -55$ to $+125$ °C unless otherwise specified

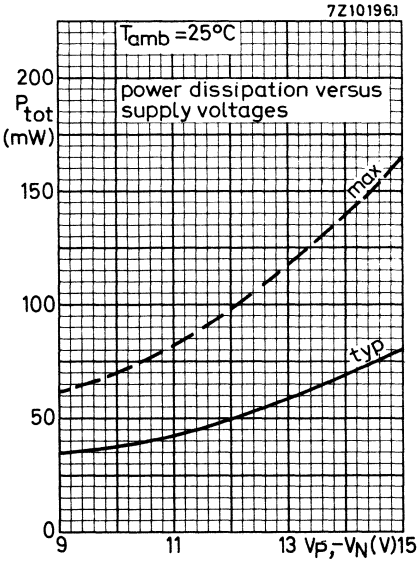
Voltage gain at $V_P = -V_N = 15$ V $R_L \geq 2$ kΩ; $V_O = \pm 10$ V	G_v		25000 to 70000 typ. 45000	
Input offset voltage; $R_S \leq 10$ kΩ	V_{io}	<	6	mV
Input offset voltage drift; $R_S = 50$ Ω	$\frac{\Delta V_{io}}{\Delta T}$	typ.	3	μV/°C
$R_S \leq 10$ kΩ	$\frac{\Delta V_{io}}{\Delta T}$	typ.	6	μV/°C
Input voltage range at $V_P = -V_N = 15$ V	V_i	> typ.	± 8 ±10	V V
Peak output voltage swing at $V_P = -V_N = 15$ V				
$R_L \geq 10$ kΩ	V_{OM}	> typ.	±12 ±14	V V
$R_L \geq 2$ kΩ	V_{OM}	> typ.	±10 ±13	V V
Common mode rejection ratio; $R_S \leq 10$ kΩ	CMRR	> typ.	70 90	dB dB
Supply voltage rejection ratio; $R_S \leq 10$ kΩ	SVRR	typ. <	25 150	μV/V μV/V
Input bias current				
at $T_{amb} = -55$ °C	I_i	typ. <	0.5 1.5	μA μA
Input offset current				
at $T_{amb} = -55$ °C	I_{io}	typ. <	0.1 0.5	μA μA
at $T_{amb} = +125$ °C	I_{io}	typ. <	20 200	nA nA
Differential input resistance	R_i	> typ.	40 100	kΩ kΩ

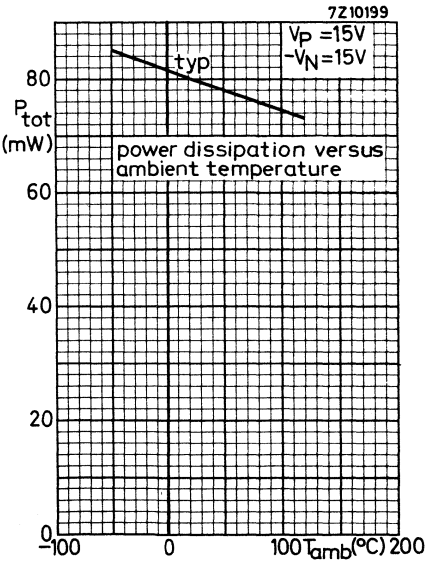
Test circuit for transient response:



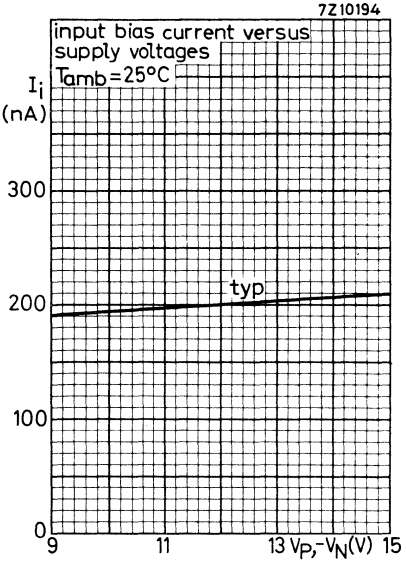

7Z10198.1
minimum values
Tamb = −55 to +125°C
VO(p-p) (V)
30
20
10
0
RL ≥ 10kΩ
2kΩ
9
11
13 VP;-VN(V) 15


7Z10192
open-loop voltage gain versus supply voltages
Tamb = −55 to +125°C
RL ≥ 2kΩ
Gv
80000
60000
40000
20000
0
max
min
9
11
13 VP;-VN(V) 15

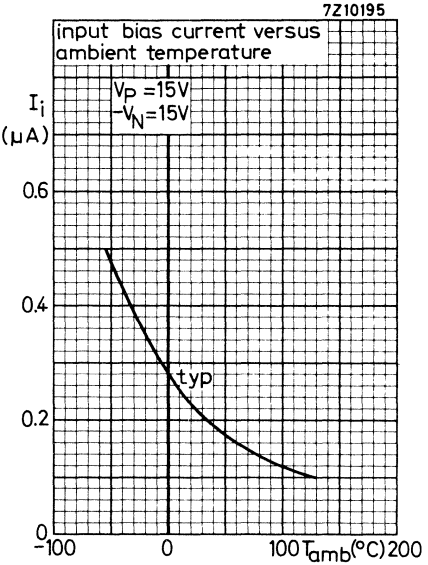

7Z10196.1
Tamb = 25°C
power dissipation versus supply voltages
Ptot (mW)
200
150
100
50
0
max
typ
9
11
13 VP;-VN(V) 15


7Z10199
VP = 15V
-VN = 15V
typ
power dissipation versus ambient temperature
Ptot (mW)
80
60
40
20
0
−100
0
100 Tamb(°C) 200

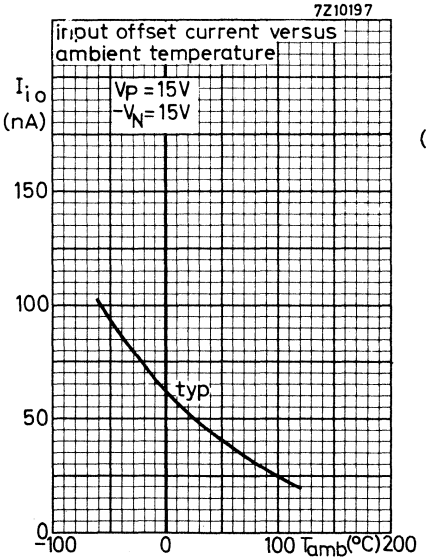
7Z10194



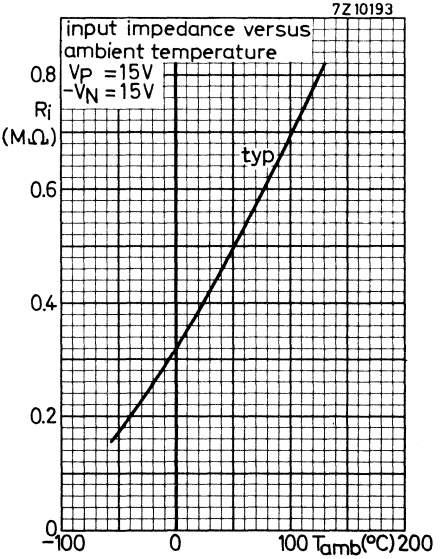
7Z10195

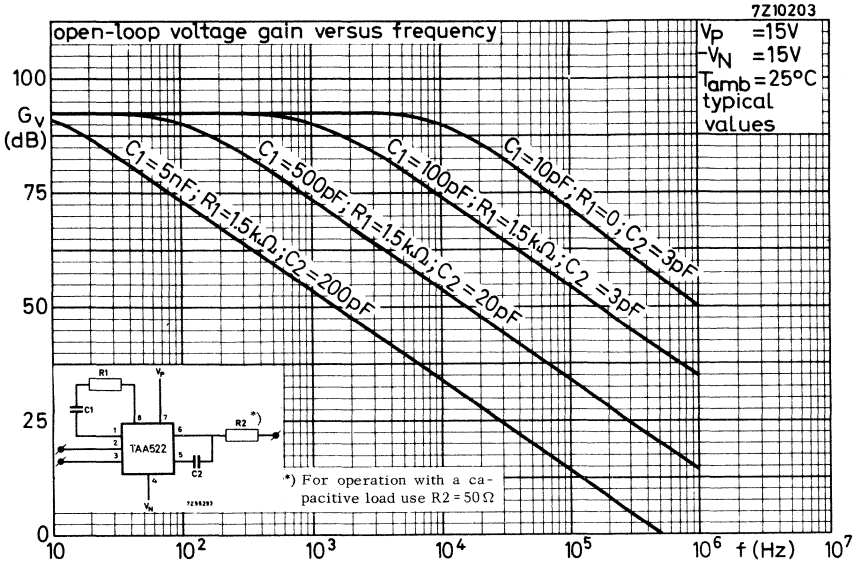


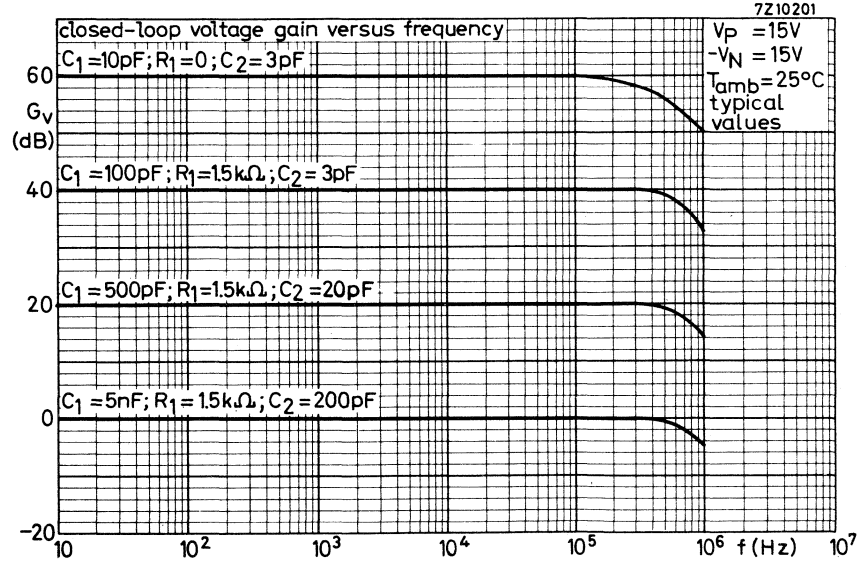
7Z10197

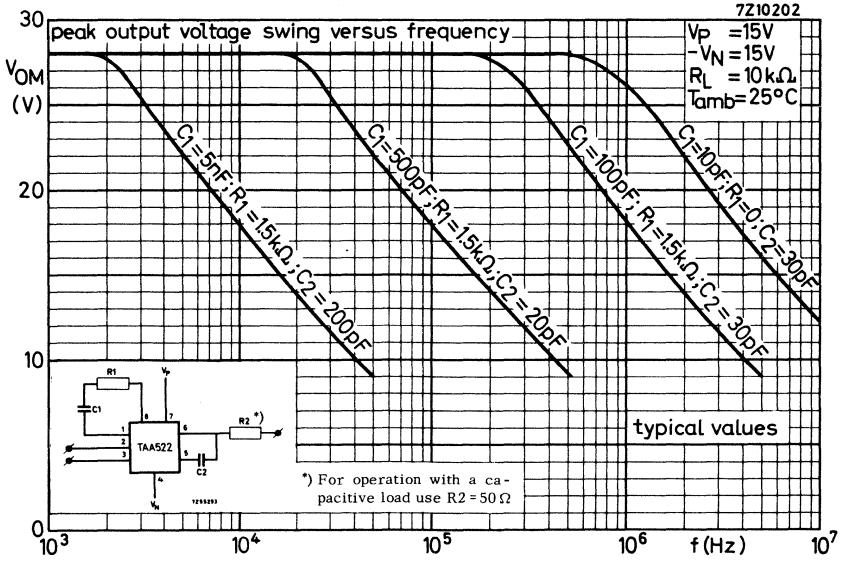


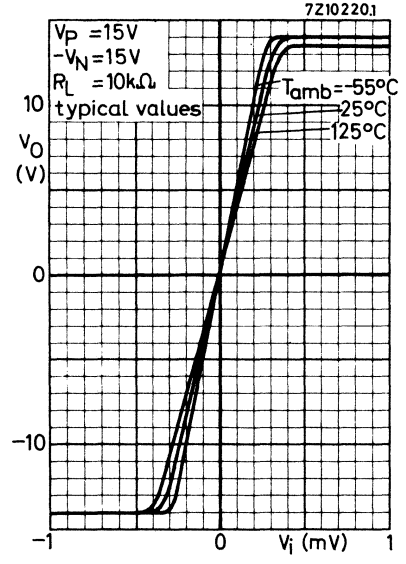
7Z10193

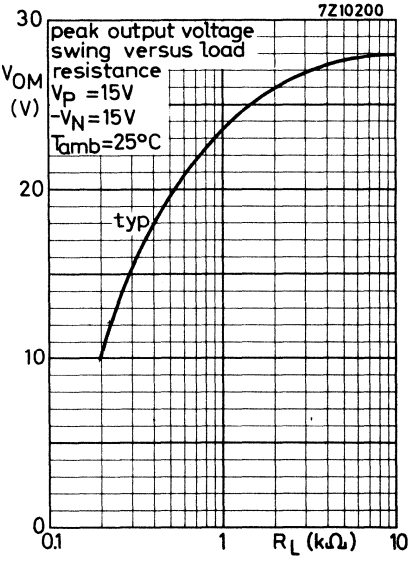



7Z10203
open-loop voltage gain versus frequency
V_P =15V
$-V_N$ =15V
T_{amb}=25°C
typical values
G_V (dB)
100
75
50
25
0
C_1=10pF; R_1=0; C_2=3pF
C_1=100pF; R_1=1.5kΩ; C_2 =3pF
C_1=500pF; R_1=1.5kΩ; C_2=20pF
C_1=5nF; R_1=1.5kΩ; C_2=200pF
R1
C1
TAA522
R2 *)
C2
*) For operation with a capacitive load use R2 = 50Ω
10
10^2
10^3
10^4
10^5
10^6 f (Hz)
10^7


7Z10201
closed-loop voltage gain versus frequency
V_P =15V
$-V_N$ =15V
T_{amb}=25°C
typical values
G_V (dB)
60
40
20
0
-20
C_1=10pF; R_1=0; C_2=3pF
C_1=100pF; R_1=1.5kΩ; C_2=3pF
C_1=500pF; R_1=1.5kΩ; C_2=20pF
C_1=5nF; R_1=1.5kΩ; C_2=200pF
10
10^2
10^3
10^4
10^5
10^6 f (Hz)
10^7


7Z10202
peak output voltage swing versus frequency
V_P =15V
$-V_N$ =15V
R_L =10kΩ
T_{amb}=25°C
V_{OM} (V)
30
20
10
0
C_1=5nF; R_1=1.5kΩ; C_2=200pF
C_1=500pF; R_1=1.5kΩ; C_2=20pF
C_1=100pF; R_1=1.5kΩ; C_2=30pF
C_1=10pF; R_1=0; C_2=30pF
typical values
R1
C1
R2 *)
C2
TAA522
*) For operation with a capacitive load use R2 = 50 Ω
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z10220.1
V_P =15V
$-V_N$=15V
R_L =10kΩ
typical values
T_{amb}=-55°C
25°C
125°C
V_O (V)
10
0
−10
−1
0
V_i (mV)
1


7Z10200
peak output voltage swing versus load resistance
V_P =15V
$-V_N$=15V
T_{amb}=25°C
V_{OM} (V)
30
20
10
0
typ.
0.1
1
R_L (kΩ)
10

VOLTAGE STABILIZER

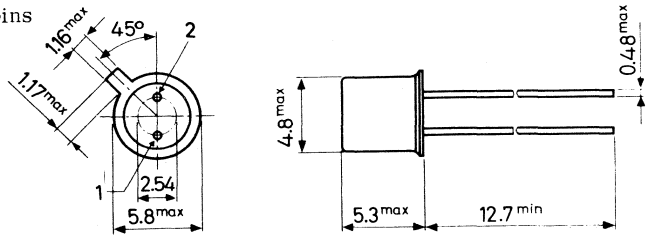
The TAA550 is an integrated monolithic voltage stabilizer, especially designed to provide the supply voltage for variable capacitance diodes in television tuners independent of supply voltage and temperature variations.
The TAA550 is supplied in 3 voltage groups, identified by a coloured dot on the envelope:

Stabilized voltage V_{12}: 31 to 32 V red dot
32 to 34 V yellow dot
34 to 35 V green dot

QUICK REFERENCE DATA			
Supply current	I_1	typ. 5	mA
Stabilized voltage	V_{12}	31 to 35	V
Differential internal resistance	r_{12}	typ. 10	Ω

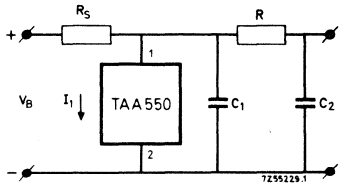
PACKAGE OUTLINE Dimensions in mm

TO-18; 2 pins



pin 1 connected to the case

RECOMMENDED CIRCUIT

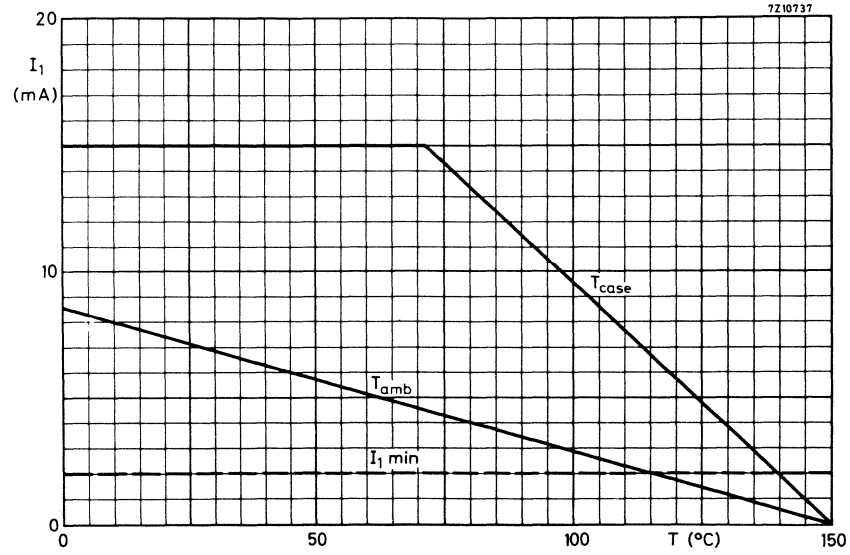


$V_B >> V_{12}$
I_1 typ. 5 mA
$R \geq 22\ \Omega$
C_1 = 300 to 4700 pF

C_2: to be connected if decoupling for low frequent noise is necessary.
In practice values up to 10 μF are used.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Maximum allowable supply current versus temperature



Temperatures			
Storage temperature	T_{stg}	-20 to +150	°C
Operating ambient temperature	T_{amb}	-20 to +150	°C

CHARACTERISTICS

Recommended supply current	I_1	>	2	mA
		typ.	5	mA
Stabilized voltage	V_{12}		31 to 35	V
Differential internal resistance at f = 1 kHz				
I_1 = 5 mA	r_{12}	typ.	10	Ω
		<	25	Ω
Temperature coefficient at T_{amb} = 10 to 50 °C	$\frac{\Delta V_{12}}{\Delta T_{amb}}$	typ.	-0.13	mV/°C
			-3.1 to +1.55	mV/°C

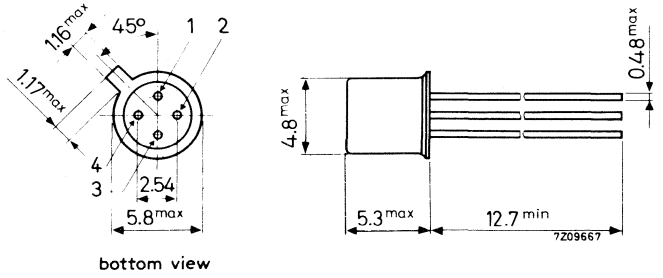
LEVEL DETECTOR

The TAA560 is a silicon monolithic integrated level detector in a (TO-72) metal envelope. A Darlington input circuit forms a Schmitt-trigger that operates at a low current level. Due to the three-stage current amplifier an output current of maximum 50 mA can be delivered.
It is primarily intended for battery fed timing circuits, such as in camera shutter control.

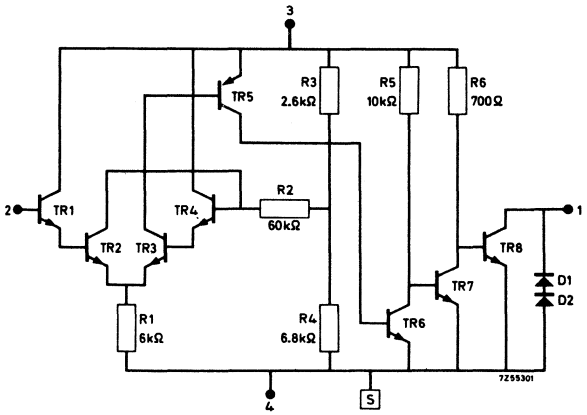
QUICK REFERENCE DATA			
Total supply voltage	V_{3-4}	2.5	V
Ambient temperature	T_{amb}	25	°C
Threshold voltage (switching off TR8)	V_{2-4}	1.4 to 1.6	V
OFF-state of TR8			
Output current	I_1	$\leq$ 0.1	μA
ON-state of TR8			
Output current	I_1	max. 50	mA
Operating ambient temperature	T_{amb}	0 to +60	°C

PACKAGE OUTLINE Dimensions in mm

(TO-72)



CIRCUIT DIAGRAM

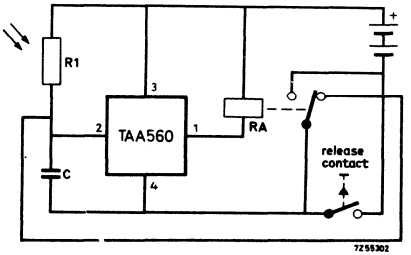


RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Total supply voltage	V_{3-4}	max.	4.5	V
Input voltage	V_{2-4}	max.	4.5	V
Output voltage	V_{1-4}	max.	12.5	V
Output current	I_1	max.	50	mA
Total power dissipation	P_{tot}	max.	120	mW
Storage temperature	T_{stg}		−55 to +100	°C
Operating ambient temperature	T_{amb}		0 to + 60	°C

CHARACTERISTICS

Recommended circuit for camera shutter time control:



Notes:

a. For shutter time range of 2 ms to 2 s; C ≈ 100nF; $R_1 \leq 20\ M\Omega$

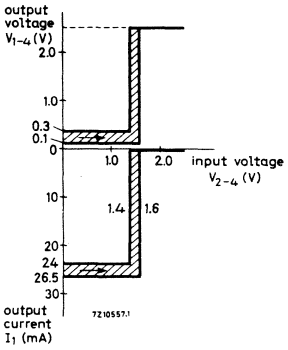
b. Solenoid inductance $L_S \leq 40$ mH and resistance $R_S = 91\ \Omega$; $V_{3-4} = 2.5$ V

CHARACTERISTICS (continued) at T_{amb} = 25 °C; $R_1 \leq 20$ MΩ; R_L = 91 Ω

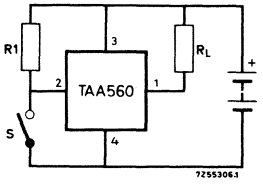
Threshold voltage

Switching TR8 to OFF-state				
at V_{3-4} = 2.5 V	$V_{2-4(H)}$	1.4 to 1.6		V [1]
	$V_{2-4(H)}$	typ.	1.5	V
at V_{3-4} = 4.5 V	$V_{2-4(H)}$	typ.	2.9	V
Switching TR8 to ON-state				
at V_{3-4} = 2.5 V	$V_{2-4(L)}$	typ.	1.2	V
at V_{3-4} = 4.5 V	$V_{2-4(L)}$	typ.	1.4	V
ON-state of TR8 (switch S closed)				
Output voltage at V_{3-4} = 2.5 V	V_{1-4}	≤	300	mV
Output current at V_{3-4} = 2.5 V	I_1	≤	26.5	mA
Current drain at V_{3-4} = 2.5 V	I_3	typ.	3.5	mA
OFF-state of TR8 (switch S open)				
Output current at V_{3-4} = 2.5 V	I_1	≤	0.1	μA
Current drain	I_3	typ.	4.1	mA

Transfer characteristic:



Test circuit:



[1]) See transfer characteristic.

LIMITER-AMPLIFIER

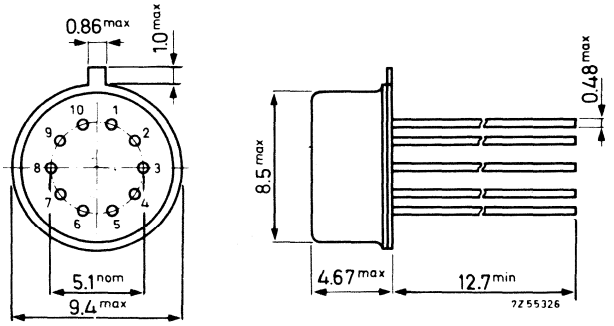
The TAA570 is a four-stage limiter-amplifier in a TO-74 metal envelope, with f.m. detector and remote control stage.
Excellent a.m. suppression is obtained by the use of a differential amplifier equipped with long-tailed pairs. The f.m. detector is a symmetrical phase detector. The remote control stage has a control range of about 80 dB on the a.f. output signal.

QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	12	V
Frequency	f_o		5.5	MHz
Total current drain	I_{tot}	typ.	19	mA
Input limiting voltage	$V_{i\ lim}$	typ.	100	μV
A.M. rejection at V_i = 10 mV		typ.	47	dB
Output at 50 kHz frequency deviation	$V_{o(rms)}$	typ.	1.8	V
Distortion at a frequency deviation of of 50 kHz and full gain	d	typ.	2.5	%

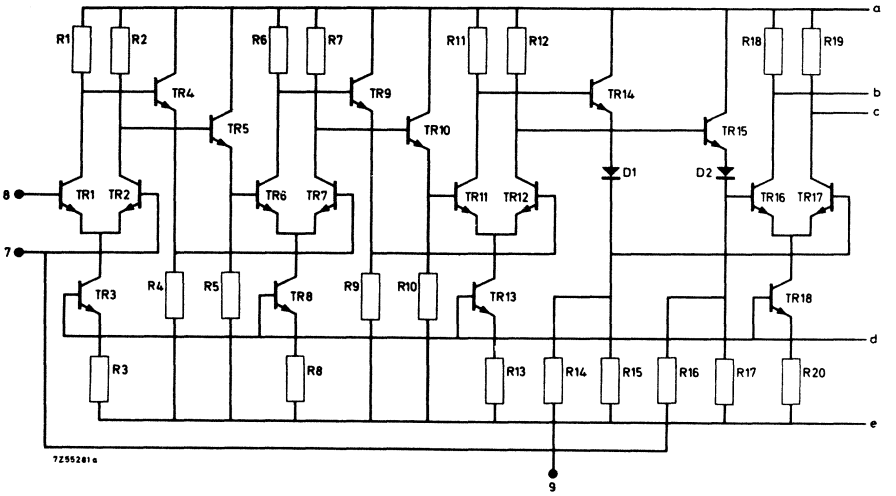
MECHANICAL DATA

Dimensions in mm

TO-74



CIRCUIT DIAGRAM

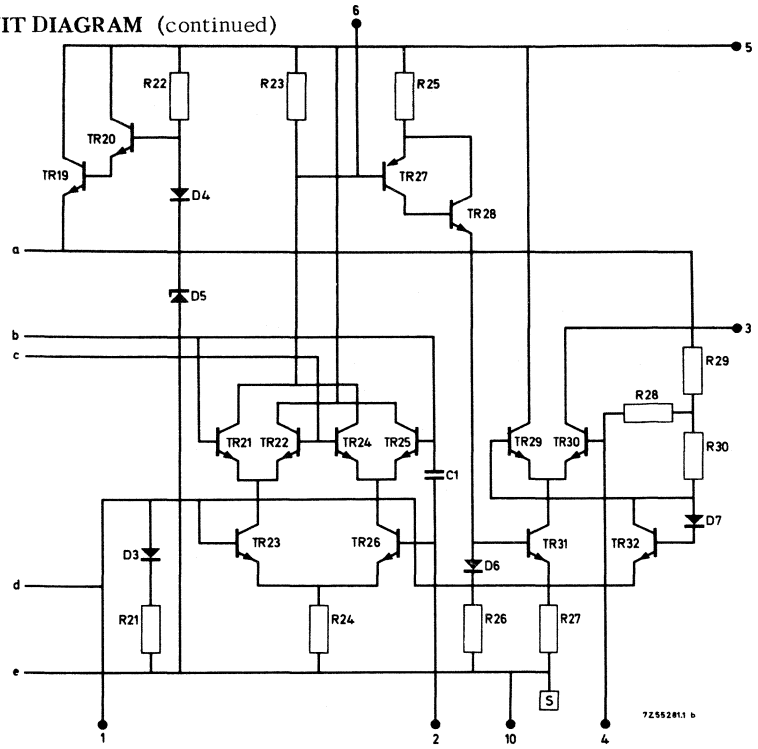


RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

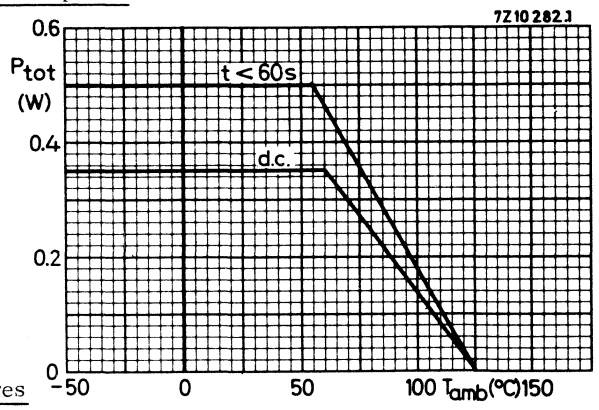
Pin No.1 voltage (do not apply an external voltage source)		
Pin No.2 voltage (do not apply an external voltage source)		
Pin No.3 voltage	V_{3-10}	0 to +18 V
Pin No.4 voltage; $I_4 < 1$ mA	V_{4-10}	0 to +6 V
Pin No.5 voltage	V_{5-10}	0 to +18 V
Pin No.6 voltage (do not apply an external voltage source)		
Pin No.7 voltage; $I_7 < 1$ mA	V_{7-10}	0 to +6 V
Pin No.8 voltage; $I_8 < 1$ mA	V_{8-10}	0 to +6 V
Pin No.9 voltage	V_{9-10}	0 to +6 V

CIRCUIT DIAGRAM (continued)



RATINGS (continued)

Total power dissipation



Temperatures

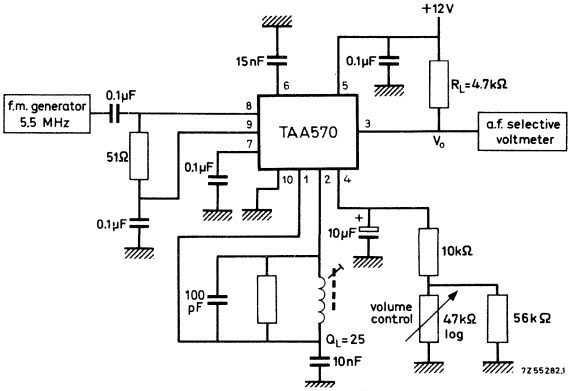
Storage temperature	T_{stg}	−25 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +125	°C

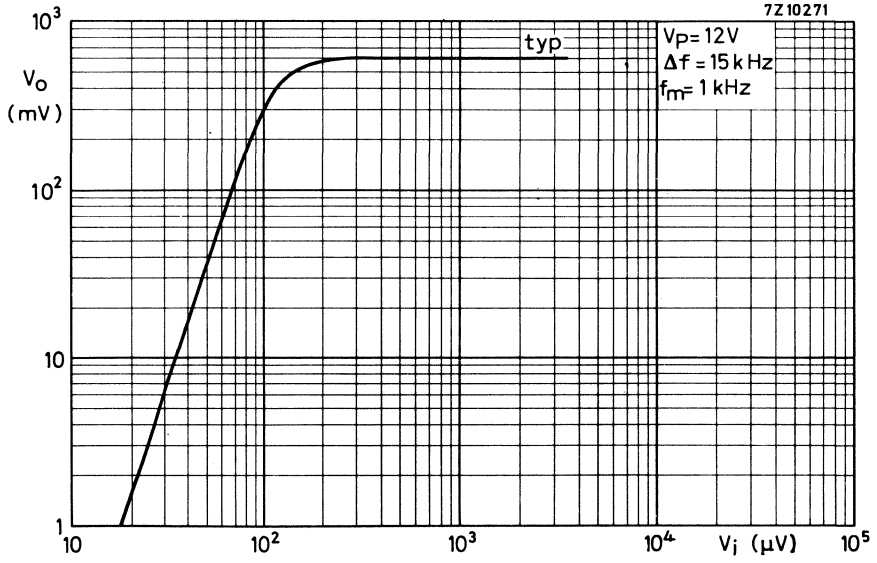
CHARACTERISTICS

Input limiting voltage

f_o = 5.5 MHz; Δf = ±15 kHz; f_m = 1 kHz — $V_{i\,lim}$ typ. 100 μV

Test circuit for measuring $V_o = f(V_i)$



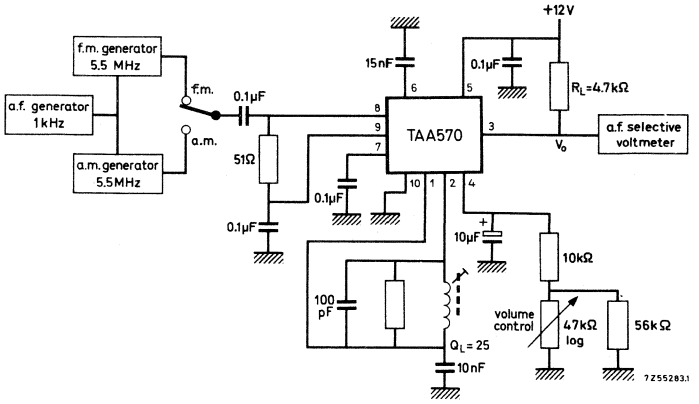


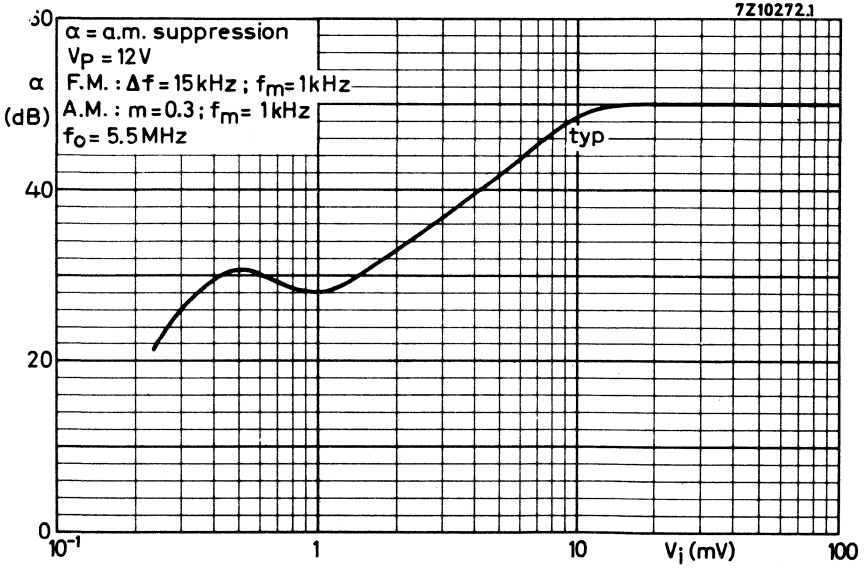
CHARACTERISTICS (continued)

A.M. suppression

F.M. : f_o = 5.5 MHz; ΔF=±15 kHz; f_m = 1 kHz
A.M. : f_o = 5.5 MHz; m = 0.3; f_m = 1 kHz

Test circuit for measuring α(AM-suppression) = f(V_i)





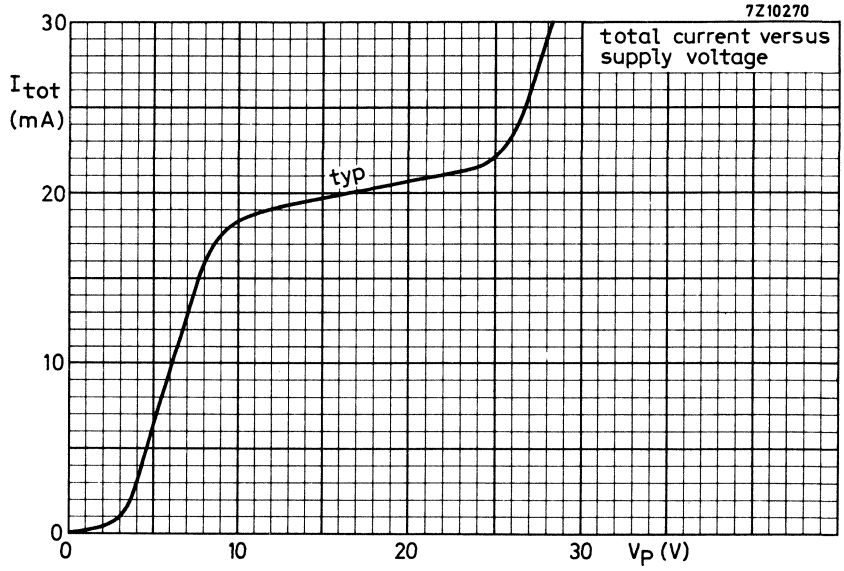
CHARACTERISTICS (continued)

Distortion at full gain and $\Delta f = \pm 15$ kHz	d	typ.	1 %
$\Delta f = \pm 50$ kHz	d	typ.	2.5 %

measuring conditions: f_o = 5.5 MHz
f_m = 1 KHz

The distortion measurements are made with the test circuit on page 4.

Total current

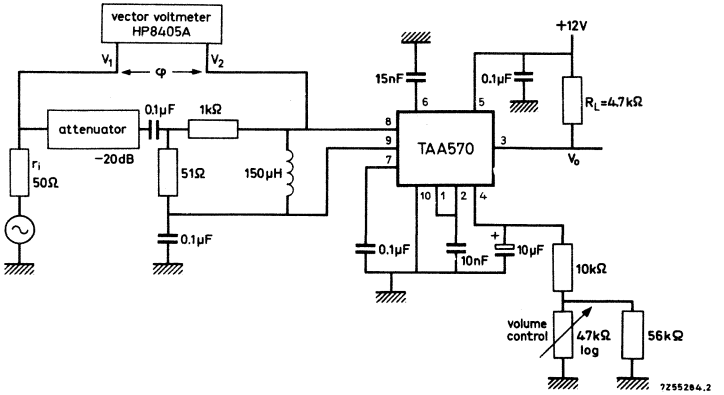


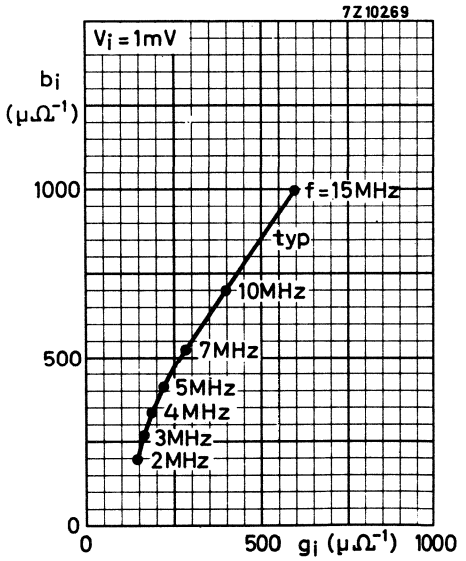
CHARACTERISTICS (continued)

y parameters

Input admittance at f_O = 5.5 MHz y_i typ. (230 + j450) $\mu\Omega^{-1}$

Test circuit for measuring $y_i = f(f)$

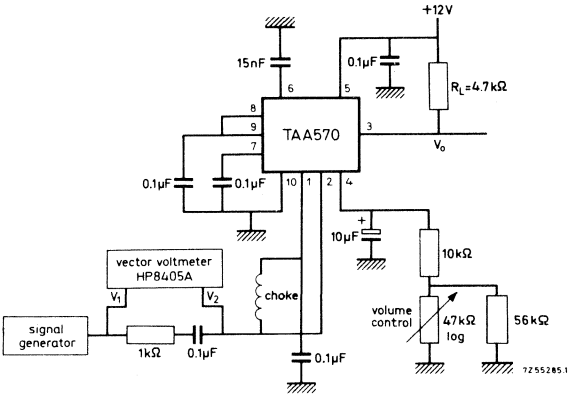


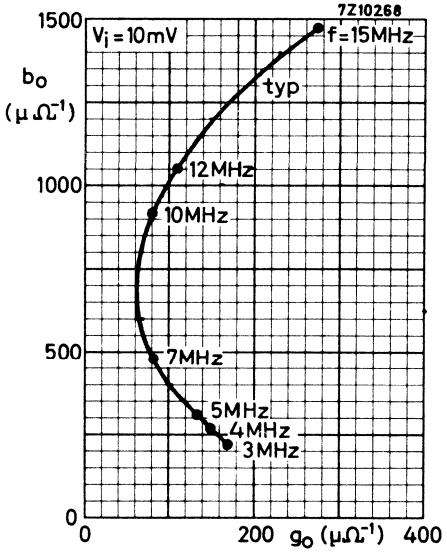


CHARACTERISTICS (continued)

Output admittance at f_o = 5.5 MHz y_o typ. (120 + j330) $\mu\Omega^{-1}$

Test circuit for measuring $y_o = f(f)$

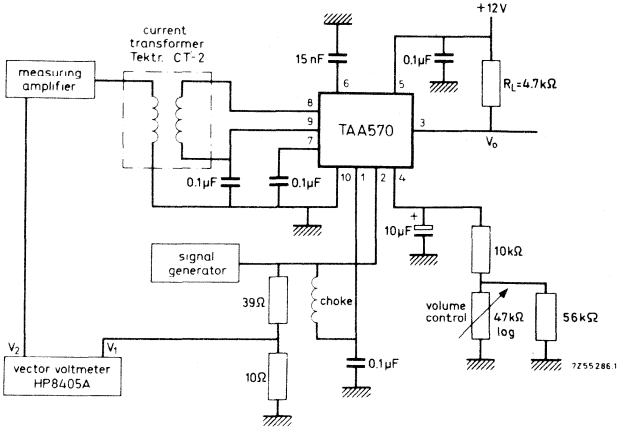


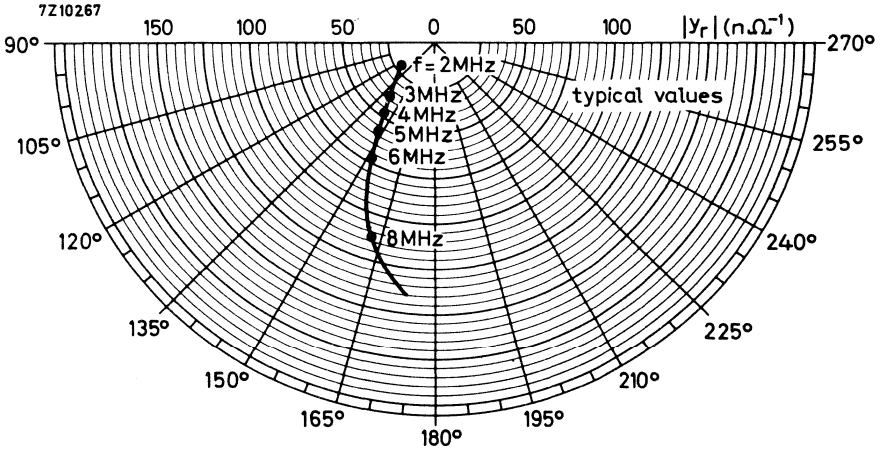


CHARACTERISTICS (continued)

Feedback admittance at f_o = 5.5 MHz $\quad y_r$ typ. $|65|\, e^{j150^o}$ nΩ^{-1}

Test circuit for measuring $y_r = f(f)$

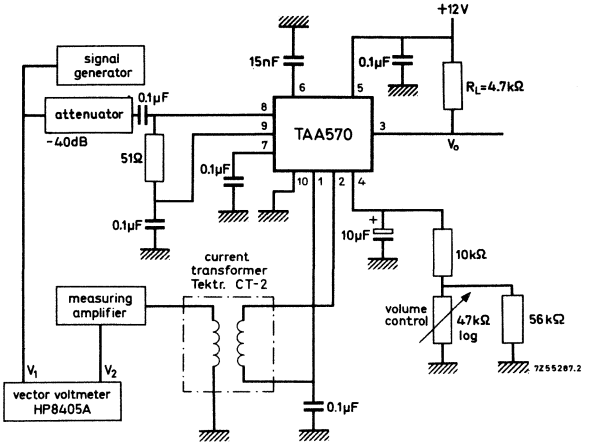


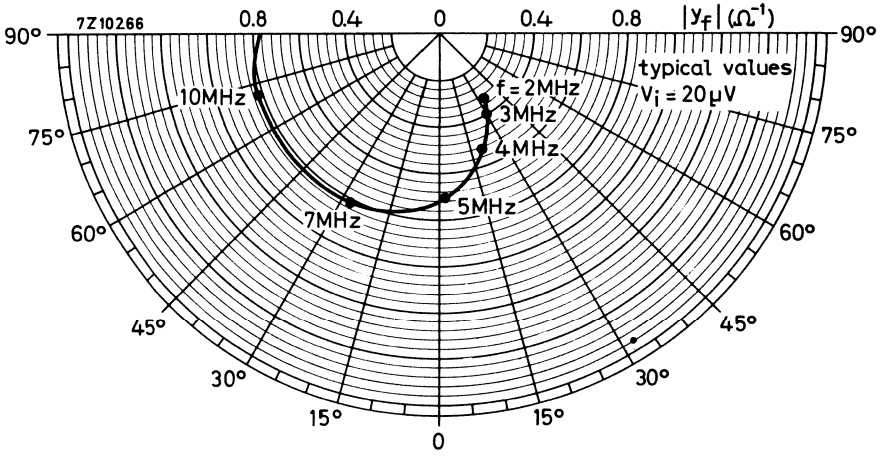


CHARACTERISTICS (continued)

Transfer admittance at f_o = 5.5 MHz y_f typ. $|0.76|\, e^{-j6^o}\ \Omega^{-1}$

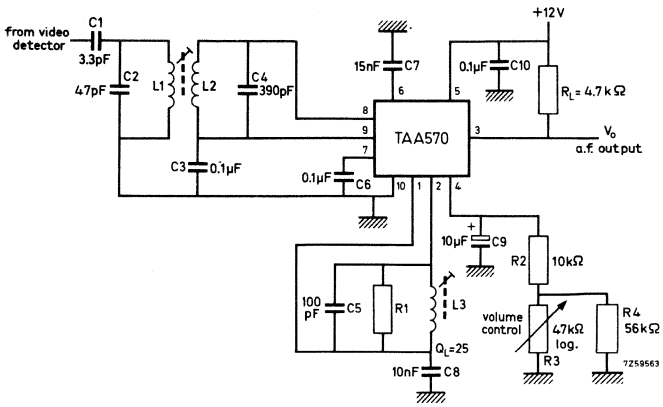
Test circuit for measuring $y_f = f(f)$





APPLICATION INFORMATION

Practical circuit



The input bandpass filter is connected to the video detector via a small capacitor of 3.3 pF. The input bandpass filter (kQ = 1) has the following characteristics:

$$L1 = 18\ \mu H;\ G_{L1} = 56\ \mu\Omega^{-1};\ Q_{L1} = 42;\ C = 47\ pF$$
$$L2 = 2.2\ \mu H;\ G_{L2} = 490\ \mu\Omega^{-1};\ Q_{L2} = 23;\ C = 390\ pF$$

The transfer voltage is $\frac{V_1}{V_2} = 0.54$

The detector coil L3 = 8.3 μH; C = 100 pF, has a loaded Q of 25.
A typical output voltage at this Q and full gain is 550 mV for Δf = 15 kHz with output signal distortion of 1 %.

LEVEL DETECTOR

The TAA580 is a plastic encapsulated silicon monolithic level detector. The circuit consists of a Schmitt-trigger, a three stage current amplifier and two further transistors to give flexibility in coupling to other circuits. The trigger voltage is adjustable within a limited range. The output stage can deliver 70 mA. The TAA580 is designed primarily for timing functions as in camera shutter control. Two TAA580 can be combined for a delayed action shutter.

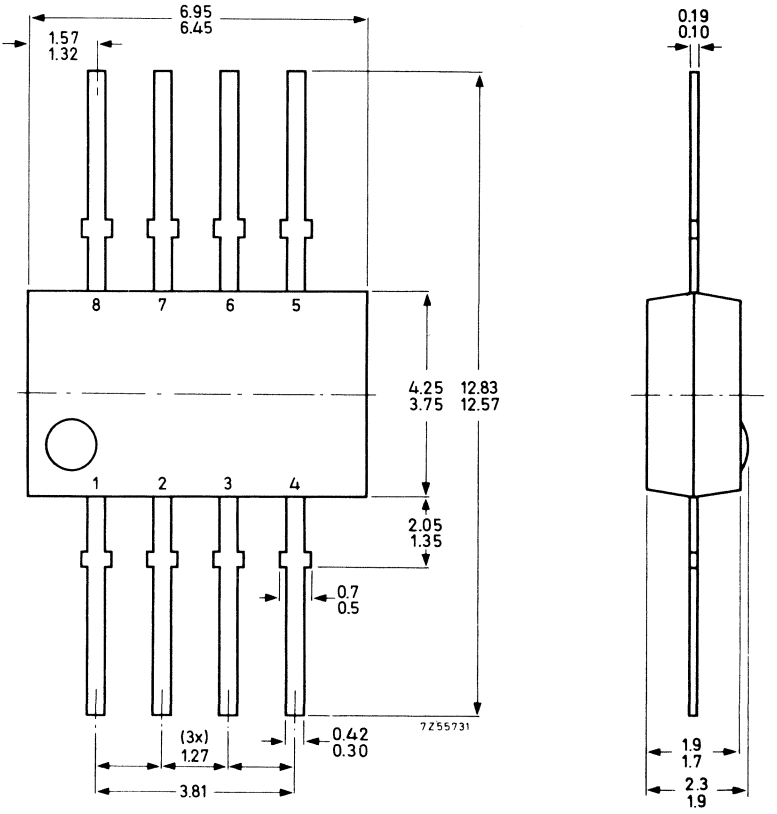
QUICK REFERENCE DATA				
Total supply voltage	V_{8-5}	nom.	2	V
Threshold voltage (adjustable)	V_{2-5}	1.4 to	1.9	V
On-state of TR9:				
Output current	I_4	max.	70	mA
Output voltage at I_4 = 28 mA	V_{4-5}	<	200	mV
OFF-state of TR9:				
Output current at V_{8-5} = 4.5 V; V_{2-5} = 3.15 V	I_4	≤	200	μA

PACKAGE OUTLINE see page 2

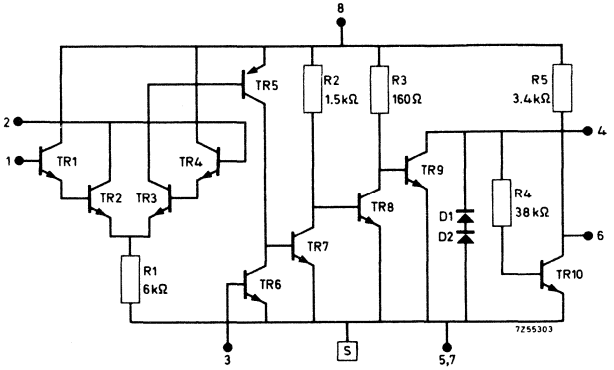
PACKAGE OUTLINE

Dimensions in mm

Pin 5 and 7 are internally connected



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Total supply voltage	V_{8-5}	max.	4.5	V
Output voltage	V_{4-5}	max.	12.5	V
Output current	I_4	max.	70	mA
Total power dissipation	P_{tot}	max.	180	mW
Storage temperature	T_{stg}	−55 to	+100	°C
Operating ambient temperature	T_{amb}	−20 to	+60	°C

CHARACTERISTICS at T_{amb} = −20 to +60 °C; R1 ≤ 70 MΩ; R_L = 64 Ω

Threshold voltage range at pin 6

V_{8-5} = 2 V; V_{3-5} = 0	V_{2-5}	1.4 to 1.9	V	
V_{8-5} = 4.5 V; V_{3-5} = 0	V_{2-5}	3.6 to 4.2	V	

Output voltage at pin 6

V_{8-5} = 4.5 V; V_{2-5} = 3.15 V [1]	V_{6-5}	≤	300	mV [2]

Output voltage at pin 4

V_{8-5} = 2 V; V_{2-5} = 1.9 V [1]	V_{4-5}	≤	200	mV [3]

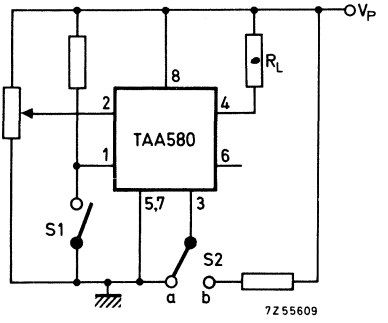
Output current

V_{8-5} = 2 V	I_4	≤	30.5	mA [2]
V_{8-5} = 4.5 V; V_{2-5} = 3.15 V [1]	I_4	≤	200	μA [3]

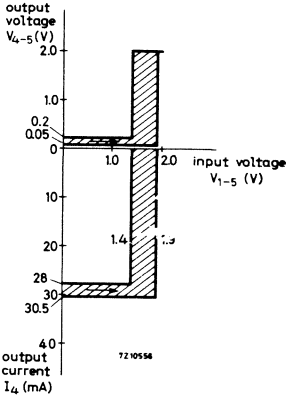
Current drain

V_{8-5} = 4.5 V	I_8	typ.	35	mA

Test circuit:

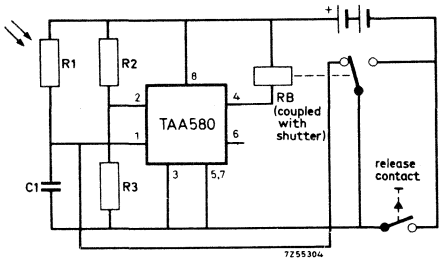


Transfer characteristic:

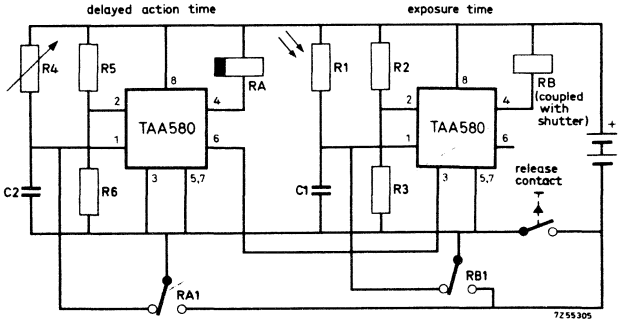


[1]) Unloaded voltage at potentiometer tap.
[2]) Switch S1 closed; switch S2 in position b.
[3]) Switch S1 closed; switch S2 in position a.

CHARACTERISTICS (continued)



Camera shutter time control



Delayed action shutter

Notes:

a. For shutter time range of 1 ms to 20 s; $C_1 \approx 270$ nF; $R_1 \leq 70$ MΩ.

b. Solenoid inductance $L_S \leq 180$ mH
   R_S values: 64 Ω to 114 Ω
   } DATA for RB and RA

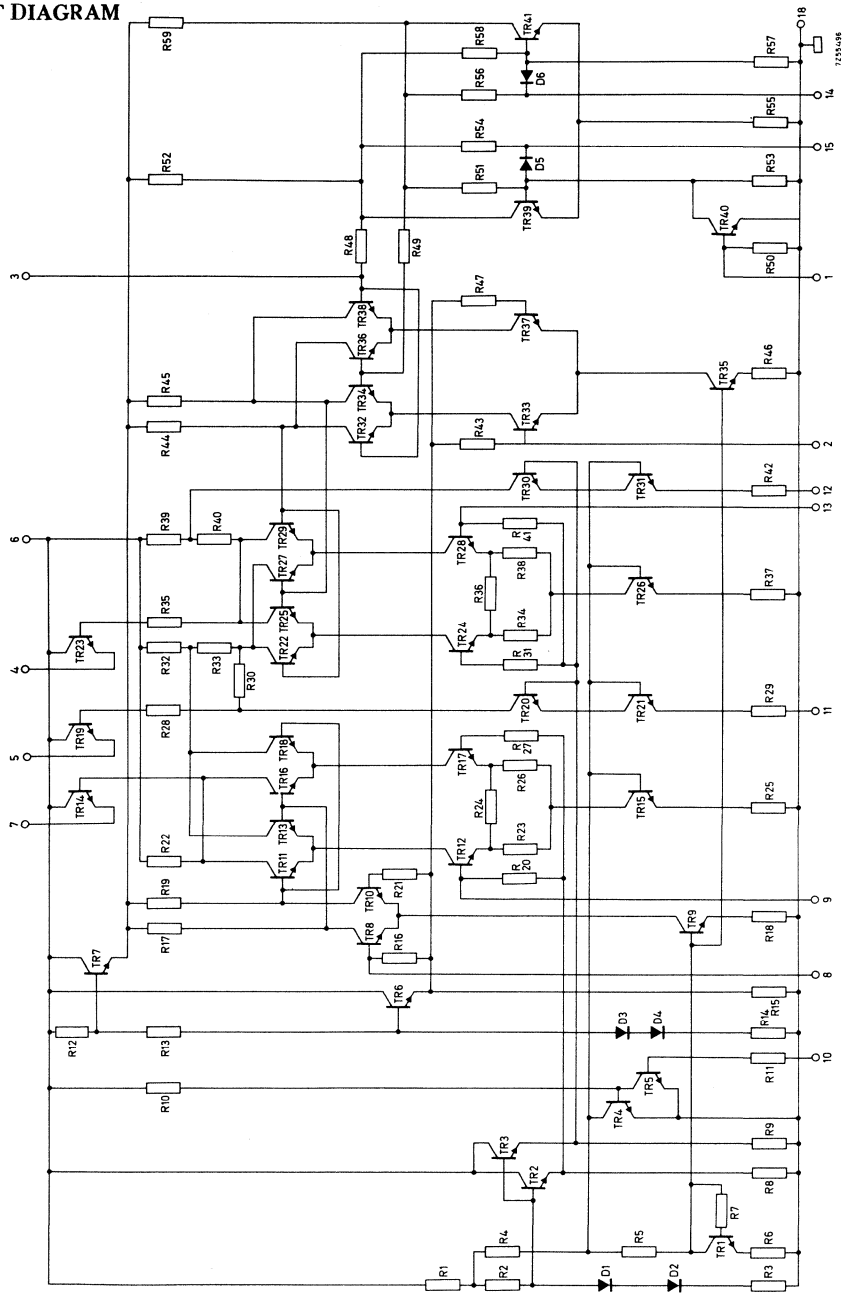
SYNCHRONOUS DEMODULATOR FOR COLOUR DIFFERENCE DRIVE

The TAA630 is a synchronous demodulator for direct drive of colour difference output stages with clamping circuits in television sets. The circuit consists of 2 amplifying synchronous demodulators for the B-Y and R-Y signals, a matrix, a PAL switch, a bistable multivibrator and colour killer switch.

QUICK REFERENCE DATA				
Supply voltage	V_{6-16}	nom.	12	V
Ambient temperature	T_{amb}		25	°C
Gain of R-Y demodulator	$G_{v(R-Y)}$	typ.	7	
Gain of B-Y demodulator	$G_{v(B-Y)}$	typ.	12.5	
Input impedance of R-Y and B-Y channel	$\lvert Z_{9-16} \rvert$	typ.	1	kΩ
	$\lvert Z_{13-16} \rvert$	typ.	1	kΩ
Output impedance of R-Y, B-Y and G-Y channel	$\lvert Z_{4-16} \rvert$	≤	100	Ω
	$\lvert Z_{5-16} \rvert$	≤	100	Ω
	$\lvert Z_{7-16} \rvert$	≤	100	Ω

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) See General Section

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

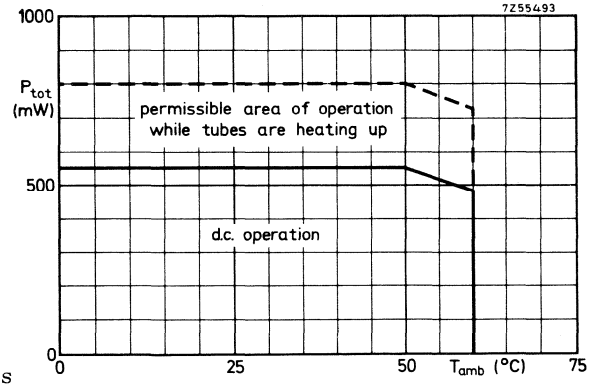
Supply voltage	V_{6-16}	max. 13.2	V
	V_{6-16}	max. 16	V [1])

Currents

Pin No.4 current	I_4	max. 5	mA
Pin No.5 current	I_5	max. 5	mA
Pin No.7 current	I_7	max. 5	mA

Power dissipation

Total power dissipation	P_{tot}	max. 550	mW
	P_{tot}	max. 800	mW [1])



Temperatures

Storage temperature	T_{stg}	−20 to +80	°C
Operating ambient temperature	T_{amb}	−20 to +60	°C

[1]) Permissible while tubes are heating up.

CHARACTERISTICS at V_{6-16} = 12 V; V_{10-16} = 0.9 V; T_{amb} = 25 °C

Gain of colour difference signals				
$V_{i(p-p)}$ = 50 mV; f = 4.4 MHz	$G_{v(R-Y)}$	typ.	7	[1]
G-Y = 0.51 (R-Y) -0.19 (B-Y)	$\frac{G_{v(B-Y)}}{G_{v(R-Y)}}$	typ.	1.78	
Input impedance of R-Y and B-Y channels				
$V_{i(rms)}$ = 20 mV (sine wave); f = 4.4 MHz				
at input F_{R-Y}; input resistance	R_{13-16}	typ.	1000	Ω
input capacitance	C_{13-16}	≤	10	pF
at input F_{B-Y}; input resistance	R_{9-16}	typ.	1000	Ω
input capacitance	C_{9-16}	≤	10	pF
Input impedance of reference inputs				
$V_{i(rms)}$ = 400 mV (sine wave); f = 4.4 MHz				
at reference R-Y input	$\|Z_{2-16}\|$	typ.	900	Ω
at reference B-Y input	$\|Z_{8-16}\|$	typ.	900	Ω
Colour difference output voltages				
(peak to peak values) output R-Y	$V_{4-16(p-p)}$	≤	3.2	V [2][3]
output B-Y	$V_{7-16(p-p)}$	≤	4.0	V [2][3]
output G-Y	$V_{5-10(p-p)}$	≤	1.8	V [2][3]
Output impedances of R-Y, B-Y and G-Y channels				
at output R-Y	$\|Z_{4-16}\|$	≤	100	Ω
at output B-Y	$\|Z_{7-16}\|$	≤	100	Ω
at output G-Y	$\|Z_{5-16}\|$	≤	100	Ω

[1]) Ratio of peak to peak values of input and output voltage measured in test circuit on page 6.

$G_{v(R-Y)} = \frac{V_{4-16}}{V_{13-16}}$; $G_{v(B-Y)} = \frac{V_{7-16}}{V_{9-16}}$

[2]) Linearity of gain ≥ 0.7

[3]) Measured in the test circuit on page 6.

CHARACTERISTICS (continued)

Colour difference d.c. output voltages

at output B-Y	V_{7-16}	typ. 7.4 V [1]
at output R-Y	adjustable to the same level as V_{7-16} [1][2]	
at output G-Y	adjustable to the same level as V_{7-16} [1][2]	

Output voltage; 7.8 kHz (square wave; peak to peak value)

$R_{load} \geq 10$ kΩ; $V_{14-16} = V_{15-16} = 2.5$ to 5 V	$V_{3-10(p-p)}$	typ. 3 V

Input voltages

Reference voltages (peak to peak value)

at reference R-Y	$V_{2-16(p-p)}$	typ. 1 V [3]
at reference B-Y	$V_{8-16(p-p)}$	typ. 1 V [3]

Horizontal deflection pulses (peak value)

at pin No. 14	$-V_{14-16M}$	2.5 to 5 V
at pin No. 15	$-V_{15-16M}$	2.5 to 5 V

Identification signal (peak to peak value)	$V_{1-16(p-p)}$	typ. 4 V

Colour killer voltage

colour "on"	V_{10-16}	$\geq$ 0.9 V
colour "off"	V_{10-16}	$\leq$ 0.3 V

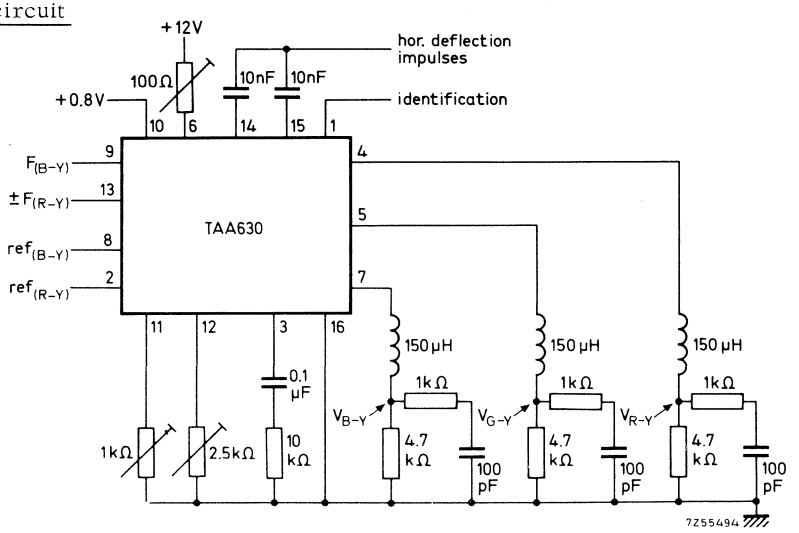
[1]) Measured in the test circuit on page 6.

[2]) To be adjusted with a variable voltage ($V \leq 1.2$ V) or with resistors connected between pin 11 and pin 16 for G-Y and between pin 12 and pin 16 for R-Y.

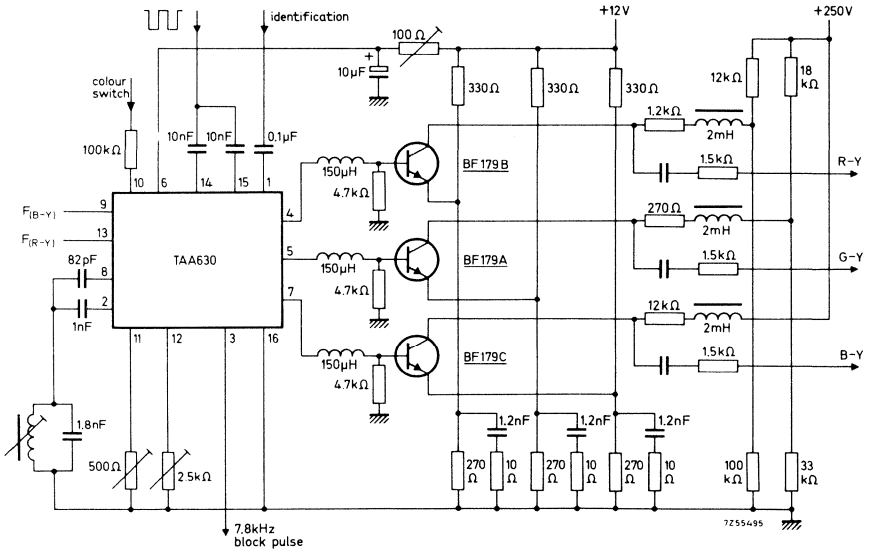
[3]) Permissible range 0.5 to 5 V.

CHARACTERISTICS (continued)

Test circuit



APPLICATION INFORMATION



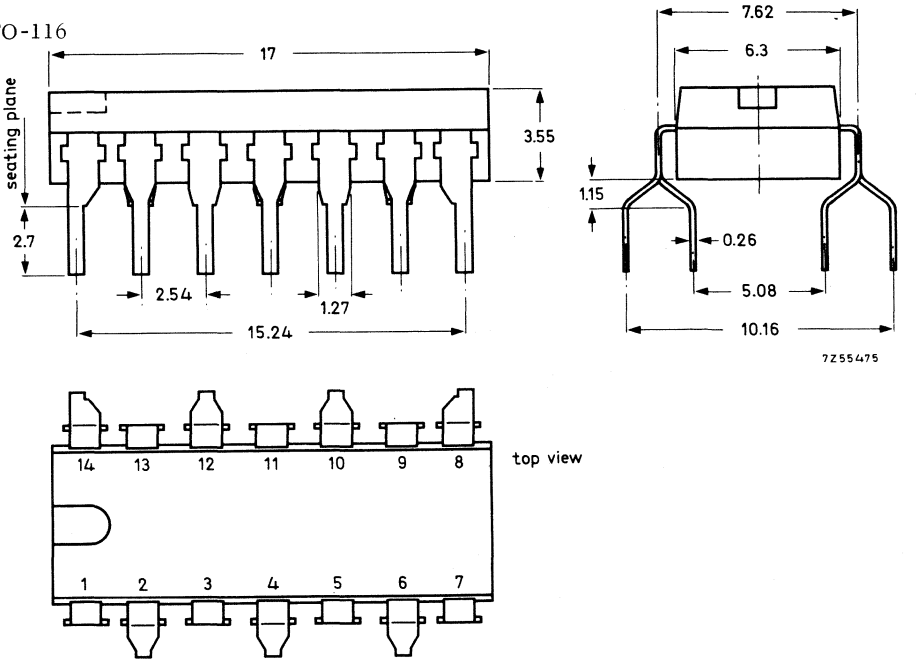
LIMITER AMPLIFIER

The TAA640 is a monolithic integrated four-stage limiter amplifier with f.m. detector and a.f. pre-amplifier. The envelope is TO-116. A differential amplifier with long-tailed pairs ensures excellent limiting action. The f.m. detector is a modified slope detector. Volume of the a.f. output can be remotely controlled over a range of 60 dB.

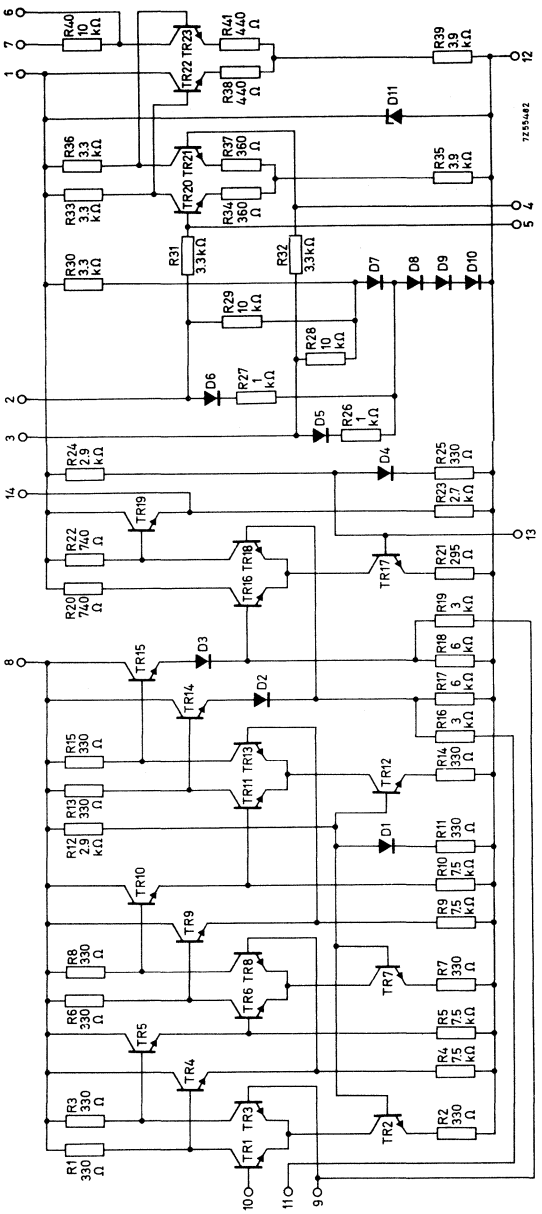
QUICK REFERENCE DATA				
Supply voltage	V_{7-12}	typ.	22	V
Total current drain	I_{tot}	typ.	26.7	mA
Input limiting voltage	$V_{i\,lim}$	typ.	100	μV
A.M. rejection at V_i = 5 mV; $\Delta f = \pm 15$ kHz		typ.	44	dB
A.F. output voltage at $\Delta f = \pm 50$ kHz	$V_{o(rms)}$	typ.	1.6	V
Total distortion at $\Delta f = \pm 50$ kHz	d_{tot}	$\leq$	5	%
Total distortion at $\Delta f = \pm 15$ kHz	d_{tot}	typ.	1.6	%

PACKAGE OUTLINE

TO-116



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages	V_{7-12}	max.	32	V	[1]
	V_{8-12}	max.	9	V	[1]
Currents	I_{tot}	max.	40	mA	[1][2]
	I_1	max.	28	mA	[1]
Total power dissipation	P_{tot}	max.	350	mW	
Operating ambient temperature	T_{amb}	−20 to +60		°C	
Storage temperature	T_{stg}	−20 to +80		°C	

CHARACTERISTICS at I_{tot} = 26.7 mA; T_{amb} = 25 °C; f = 5.5 MHz; f_{mod} = 1 kHz measured in the test circuit on page 3.

Voltages	V_{1-12}	typ.	7.4	V
		≤	8.5	V
	V_{7-12}	typ.	22	V
Current	I_7	typ.	0.7	mA
I.F. voltage gain	G_v	≥	70	dB
		typ.	76	dB
Input limiting voltage (−3 dB)		typ.	100	μV
I.F. output voltage at V_i = 5 mV	$V_{o(p-p)}$	typ.	1.7	V
A.F. output voltage at V_i = 5 mV; Δf = ± 50 kHz	V_o	typ.	1.6	V
Total distortion				
V_i = 5 mV; Δf = ± 50 kHz	d_{tot}	≤	5	%
V_i = 5 mV; Δf = ± 15 kHz	d_{tot}	typ.	1.6	%
Remote volume control range (a.f.)	ΔV_o	≥	60	dB
AM rejection at V_i = 5 mV				
Δf = ±15 kHz, m = 0.3		typ.	44	dB

[1]) Permissible while tubes are heating up.

[2]) $I_{tot} = I_1 + I_7 + I_8$

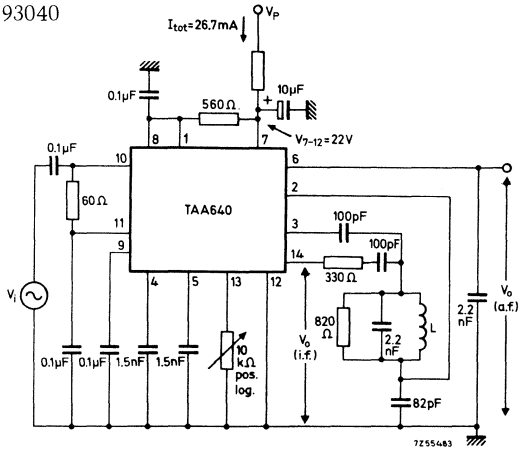
APPLICATION INFORMATION

Detector coil L: 6.5 turns 0.5 mm Cu wire.

Coil former: AP3016/02 (used without Ferroxcube frame)

Can: AP3015/02

Screw core: 3122 104 93040



TELEVISION SIGNAL PROCESSING CIRCUIT

The TAA700 is a silicon monolithic integrated signal processing circuit for television receivers. It combines following functions:

- video pre-amplifier with emitter follower output.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner (delayed)
- noise inverter for gating the a.g.c. and sync separator circuits
- sync. separator
- automatic horizontal synchronisation
- vertical sync. pulse separator
- blanking facility for the video amplifier

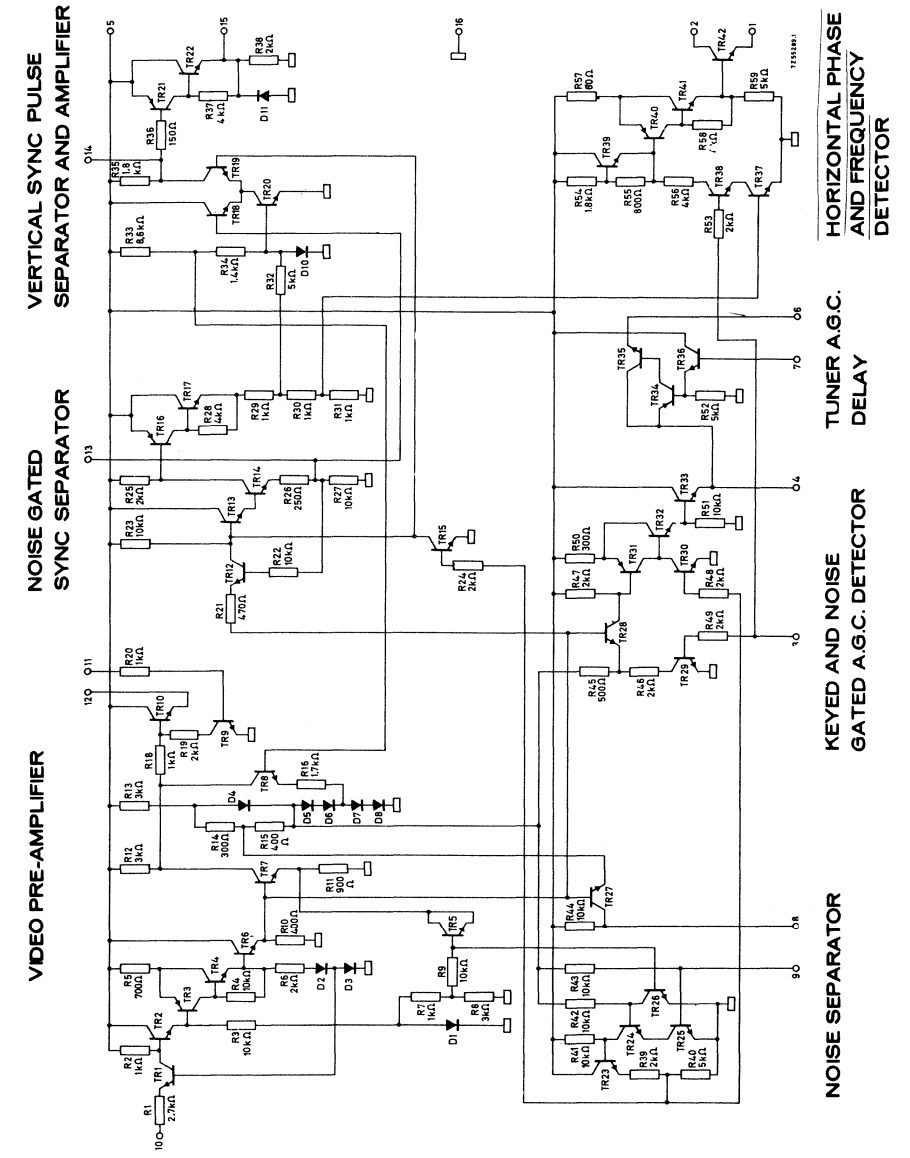
The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages, and with n-p-n transistors in the tuner and i.f. amplifier.

Only signals with negative modulation can be handled by the circuit.

QUICK REFERENCE DATA				
Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}		25	°C
Video input voltage (peak to peak value)	$V_{10\text{-}16\ (p\text{-}p)}$	typ.	2	V
Voltage gain of the video amplifier	G_v	typ.	9.5	dB
A.G.C. voltage for i.f. part (R_1 = 2 kΩ)	$V_{4\text{-}16}$	typ.	0 to 8	V
A.G.C. voltage for tuner (R_1 = 1 kΩ)	$V_{6\text{-}16}$	typ.	0 to 7	V
Output voltage horizontal phase detector	$\pm V_{2\text{-}1}$	typ.	3	V
Vertical sync. output voltage (positive going pulse; peak to peak value)	$V_{15\text{-}16(p\text{-}p)}$	>	10	V

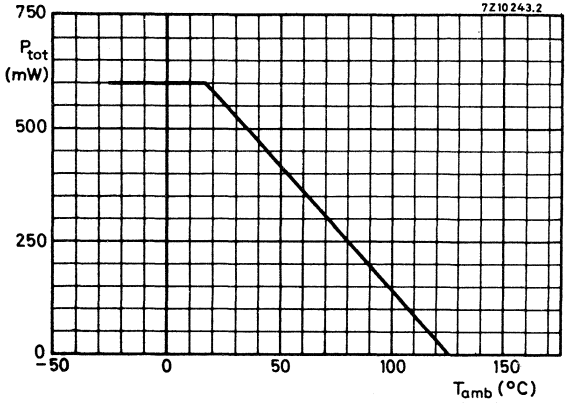
MECHANICAL DATA (See page 7)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	16	V [1])
Power dissipation	P_{tot}	max.	600	mW



Temperatures

Storage temperature	T_{stg}	−25	to +125	°C
Operating ambient temperature	T_{amb}	−25	to +125	°C

[1]) Permissible while tubes are heating up.

CHARACTERISTICS

Supply voltage range	V_P		10 to 14	V	
Measured in circuit on page 6 at T_{amb} = 25 °C; V_P = 12 V					
Video amplifier					
Input resistance (detector load)	R_{10-16}	typ.	2.7	kΩ	
Input capacitance	C_{10-16}	<	1	pF	
Bandwith (3dB)	B	>	5	MHz	
Voltage gain	G_v	typ.	9.5	dB	
Video input voltage (peak to peak value)	$V_{10-16(p-p)}$	typ.	2	V	1)
Video output voltage (peak to peak value)	$V_{12-16(p-p)}$	typ.	6	V	2)
Tolerances on video output voltage:					
I.C. processing spreads	$\pm\Delta V_{12-16}$	<	550	mV	
Temperature drift	$-\Delta V_{12-16}$	<	20	mV/°C	3)
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{12-16}$	<	270	mV	4)
Black level at the output	v_{12-16}	typ.	5	V	5)
Tolerances on the black level at the output:					
I.C. processing spreads	$\pm\Delta v_{12-16}$	<	300	mV	
Temperature drift	Δv_{12-16}	<	7	mV/°C	3)
Spreads over a.g.c. expansion (entire range)	$\pm\Delta v_{12-16}$	<	250	mV	4)6)
Variation black level at the output due to supply voltage variations	$\frac{\Delta V_{12-16}}{\Delta V_P}$	typ.	0.7		
Available video output current (peak value)	I_{12M}	typ.	14	mA	7)

1) Negative going video signal (no pre-bias needed for the detector)
2) Video signal with negative going sync pulse.
3) Because the integrated circuit reaches 95% of its final working temperature in 100 seconds, the temperature variations to be considered are those caused by the slower rise in cabinet temperature and by changes in room temperature.
4) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled. The video signal increases and the black level decreases with increasing antenna signal.
5) Only valid if the video signal is in accordance with the CCIR standard.
6) To this must be added $0.7\Delta V_P$, if operation of the a.g.c. causes a change in V_P.
7) The total load on pin 12 must be such that under nominal conditions $I_{12M} \leq 14$ mA.

CHARACTERISTICS (continued)

Video blanking		
Input voltage (peak to peak value)	$V_{11\text{-}16(p\text{-}p)}$	1 to 5 V
Input resistance	$R11\text{-}16$	typ. 1 kΩ
A.G.C. circuit		
Control voltage i.f. amplifier	$V_{4\text{-}16}$	0 to 8 V [1]
Control voltage tuner	$V_{6\text{-}16}$	0 to 7 V [1]
Signal expansion for full control of i.f. amplifier and tuner		< 15 % [1]
Keying input pulse (peak to peak value)	$V_{3\text{-}16(p\text{-}p)}$	1 to 5 V [2]
Input resistance	$R3\text{-}16$	typ. 1 kΩ
Synchronisation circuit		
Sync. separator		see note 3
Control voltage line oscillator	$\pm V_{2\text{-}1}$	typ. 3 V [4]
Output voltage vertical sync. pulse separator (peak to peak value)	$V_{15\text{-}16(p\text{-}p)}$	> 10 V
Output impedance	$R15\text{-}16$	typ. 2 kΩ

[1]) These figures are obtained with a load impedance of 2 kΩ for the i.f. control point (R4-16) and 1 kΩ for the tuner control point (R6-16). With these impedances the signal expansion for i.f. control and tuner control will be about the same. An increase of these impedances will reduce the signal expansion. Lower values will reduce the available control voltage and increase the dissipation of the integrated circuit. Therefore, the minimum values must be restricted to 1.5 kΩ for the i.f. control point and 750 Ω for the tuner control point.

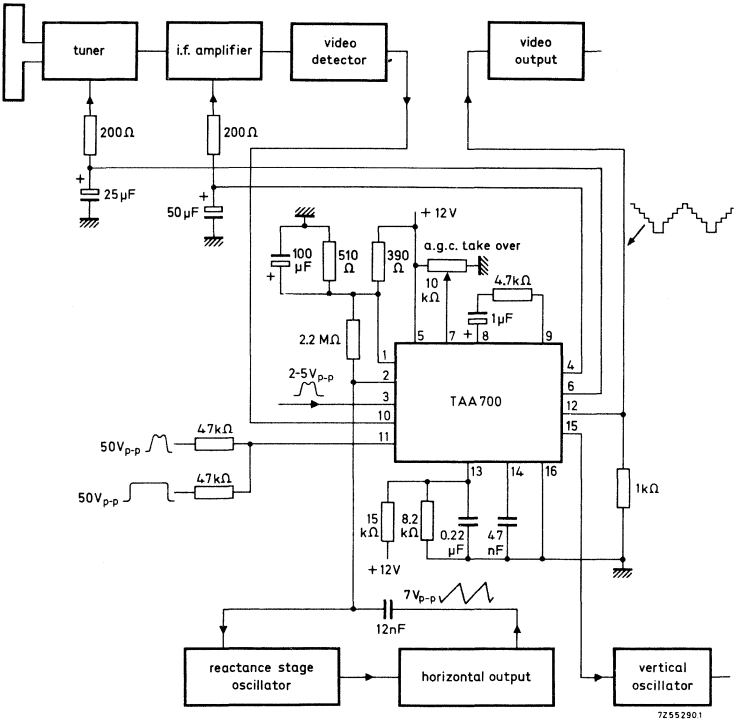
[2]) The TAA700 may be operated unkeyed but then point 3 must be connected to the positive supply line via a resistor of suitable value (e.g. 10 kΩ). However, the following consequences should be borne in mind:

- The decoupling capacitors at the i.f. and tuner control points must be larger to prevent ripple voltages due to the vertical sync pulses. In consequence the a.g.c. will not follow fast signal fluctuations (airplane flutter).
- Since the horizontal phase detector is designed to be keyed, unkeyed operation will result in the phase detector not operating as a frequency detector when the horizontal oscillator is out of sync. This considerably decreases the catching range.

[3]) The sync pulse is sliced about 30% below top sync level.

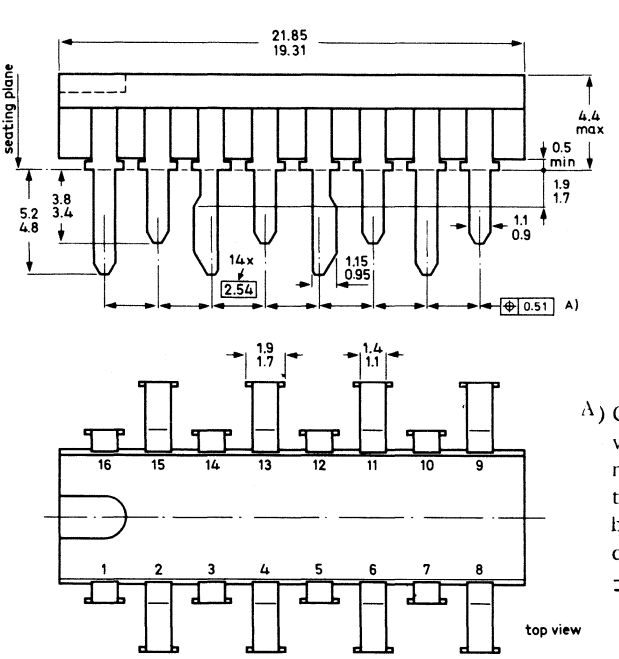
[4]) Required reference voltage $V_{2(p\text{-}p)}$ (sawtooth or differentiated line fly-black pulse) = 7 V. For an oscillator-reactance stage with a control sensitivity of 400 Hz/V this gives a holding range of about ± 1000 Hz.
Because the phase detector is keyed a catching range of ± 700 Hz is obtained without affecting the noise immunity.

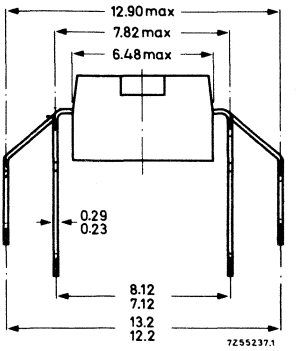
APPLICATION INFORMATION



MECHANICAL DATA

Dimensions in mm





A) Centre-lines of all leads are within ±0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.51 mm.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

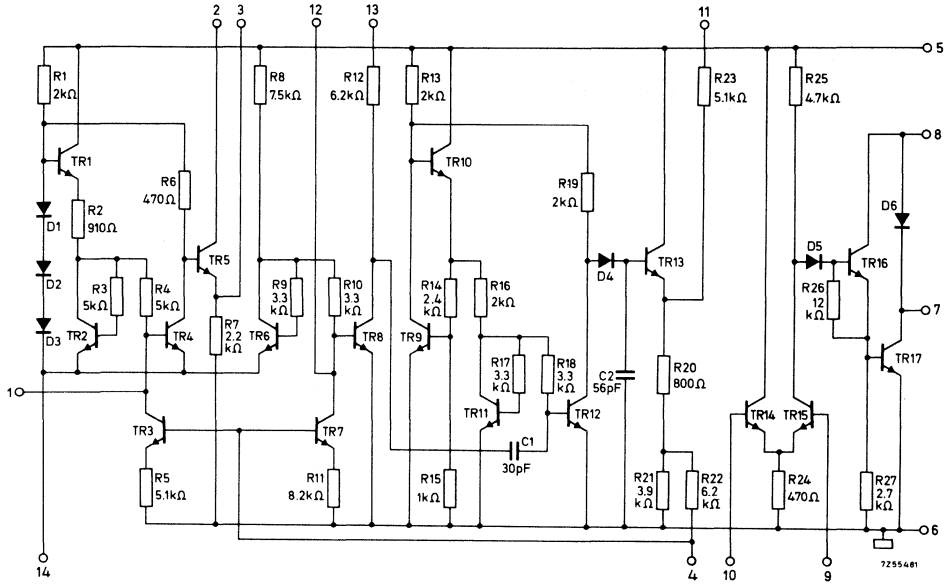
INTEGRATED A.M. RADIO RECEIVER CIRCUIT

The TAA840 is a monolithic integrated circuit for use in a.m. radio; it incorporates an r.f. amplifier, mixer-oscillator, i.f. amplifier, a.g.c., detector, audio pre-amplifier and driver.
An **audio output stage** suiting the requirements of the receiver must be added separately.
The detection capacitor and resistor of the series detector are integrated. The i.f. amplifier incorporates provision for the use of a tuning indicator. Since the circuit is adapted to operate in conjunction with i.f. filters having low input and output impedance, pre-aligned i.f. block-filters can be used.

QUICK REFERENCE DATA				
Ambient temperature	T_{amb}		25	°C
Supply voltage	V_P	typ.	6	V
A.F. output power at d_{tot} = 10% (with AC187/AC188)	P_o	typ.	900	mW
Total quiescent current (except output stages)	I_{tot}	typ.	17	mA
R.F. input voltage (at pin 1) for a signal to noise ratio of 26 dB	V_i	typ.	20	μV
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range)		typ.	64	dB
R.F. signal handling (at pin 1)		typ.	20	mV
R.F. input voltage (at pin 1) for full output (start of clipping at P_o = 650 mW)		typ.	3	μV
Harmonic distortion of h.f. part (over most of a.g.c. range) m = 30%	d_{tot}	typ.	1.2	%
m = 80%	d_{tot}	typ.	2.6	%

PACKAGE OUTLINE : 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum system (IEC 134)

Voltages (tolerated minimum: 0 V)

Pin No. 2 voltage	V_{2-6}	max.	12	V
Pin No. 3 voltage	V_{3-6}	max.	6	V
Pin No. 4 voltage	V_{4-6}	max.	1	V
Pin No. 5 voltage	V_{5-6}	max.	12	V
Pin No. 7 voltage	V_{7-6}	max.	12	V
Pin No. 8 voltage	V_{8-6}	max.	12	V
Pin No.11 voltage	V_{11-6}	max.	12	V
Pin No.13 voltage	V_{13-6}	max.	12	V

Currents (tolerated minimum: 0 mA)

Pin No. 1 current	I_1	max.	80	μA
Pin No. 9 current	I_9	max.	80	μA
Pin No.10 current	I_{10}	max.	80	μA
Pin No.12 current	I_{12}	max.	80	μA

Dissipation	P_{tot}	max.	260	mW

Temperatures

Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	−20 to +55		°C

CHARACTERISTICS at T_{amb} = 25 °C; V_P = 6 V [1])

Measured in the circuit on page 5

Breakdown voltage of driver stage	$V_{(BR)CEO}$	>	12	V
Saturation voltage of driver stage	$V_{CE\ sat}$	<	0.6	V
Pin No.5 voltage at V_P = 6 V (via a series resistor of 68 Ω)	V_{5-6}	typ.	5.5	V
Current drain	$I_2 + I_5 + I_{13}$	typ.	8	mA
	$I_7 + I_8$	typ.	8.4	mA [2])
Quiescent current of a.f. output stage with AC187/AC188	I_Q	typ.	5	mA
Total chip dissipation	P_{tot}	typ.	65	mW
		<	125	mW
Supply voltage for 20 mV (r.m.s value) oscillator operation at f = 1 MHz		>	3	V

A.C. characteristics

A.F. output power at d_{tot} = 10% (with AC187/AC188) f = 1000 Hz	P_o	typ.	900	mW
A.F. output power (onset of clipping) f = 1000 Hz	P_o	typ.	650	mW
R.F. input voltage (at pin 1) for signal to noise ratio of 26 dB	V_i	typ.	20	μV [3]) [4])
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range)		typ.	64	dB [3]) [4])

1) Circuit designed for use in receivers with 6 V or 9 V battery. Voltage at pin 5 to be adjusted 5.5 V regardless of battery voltage; a.f. driver (pin No.8) can be fed direct from either 6 V or 9 V.
2) $I_7 + I_8$ depend on the load resistances at pins 7 and 8.
3) Measured at 1 MHz with the antenna circuit connected (source resistance of about 1 kΩ for pin 1)
4) 30% modulation, f_m = 1000 Hz.

CHARACTERISTICS (continued)

Signal handling:			
R.F. input voltage (at pin 1) to obtain 10% distortion at 80% modulation, f_m = 1 kHz	typ.	20	mV [1]
R.F. input voltage (at pin 1) for 10 mV (a.f.) across volume control	typ.	2.7	μV [1][2]
A.F. voltage across volume control for 100 μV (r.f.) input voltage (at pin 1)	typ.	30	mV [1][2]
Input conductance of r.f. amplifier (at pin 1)	typ.	0.5	$m\Omega^{-1}$ [1]
Input conductance of i.f. amplifier at f = 500 kHz (at pin 12)	typ.	0.5	$m\Omega^{-1}$
Signal to noise ratio for 1 mV (r.f.) input voltage (at pin 1)	typ.	46	dB [1] [2]
A.F. voltage (at pin 9) for 50 mW output power	<	4.5	mV
A.F. voltage (at pin 9) for output power at onset of clipping	typ.	10	mV
Loss of overall receiver sensivity at cell voltage of 0.9 V and 50 mW output power	typ.	4	dB [1][2]
Oscillator frequency shift over range of supply voltage at f_{osc} = 2 MHz	<	1.3	kHz/V

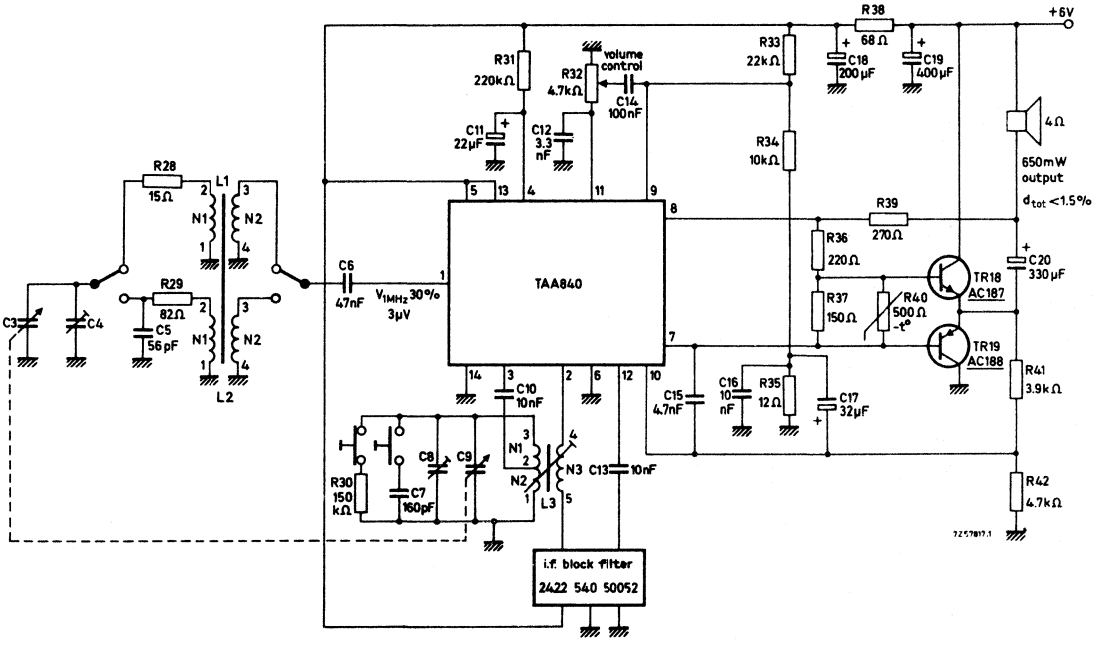
→ Note
Tuning indicator inserted in pin 13

[1]) Measured at 1 MHz with the antenna circuit connected (source resistance of about 1 kΩ for pin 1)

[2]) 30% modulation, f_m = 1000 Hz

APPLICATION INFORMATION

Circuit of a medium wave-long wave radio receiver, with TAA840 (given for m.w.)



Ferrite rod aerial coils

Medium wave: N1 : N2 = 65 : 3.5
L1 = 450 μH; Q_0 = 100 at 1 MHz

Long wave: N1 : N2 = 200 : 10
L2 = 3.5 mH; Q_0 = 75 at 200 kHz

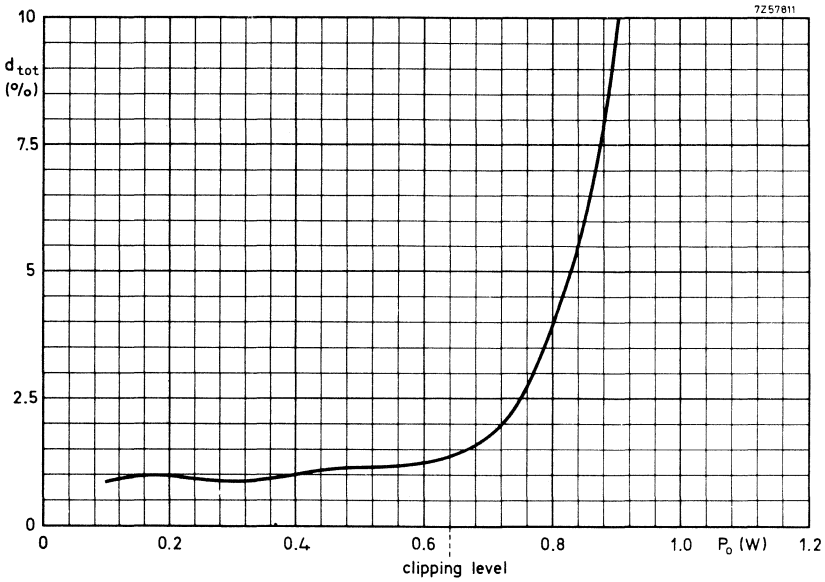
Oscillator coils:

N1 : N2 = 135 : 2 (N1 + N2) : N3 = 137 : 12

L3 = 300 μH; Q_0 = 95 at 1 MHz

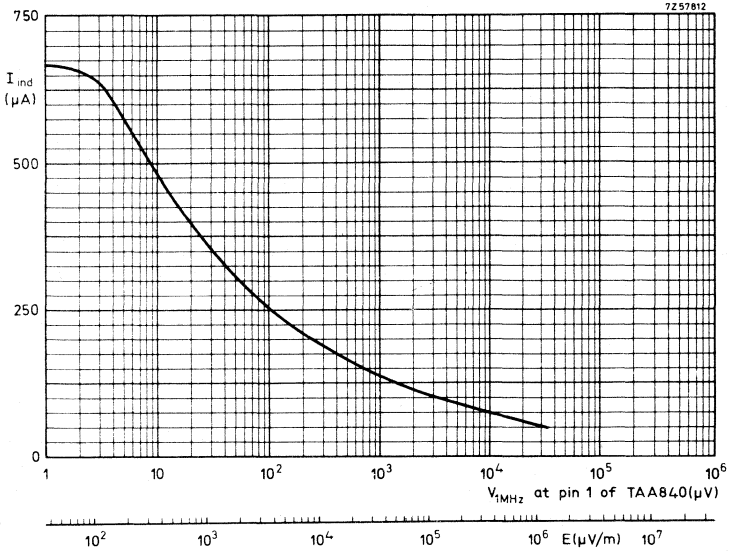
C3 = 0 to 195 pF C9 = 0 to 80 pF
C4 = trimmer C8 = trimmer
} 2222 807 10039

APPLICATION INFORMATION (continued)

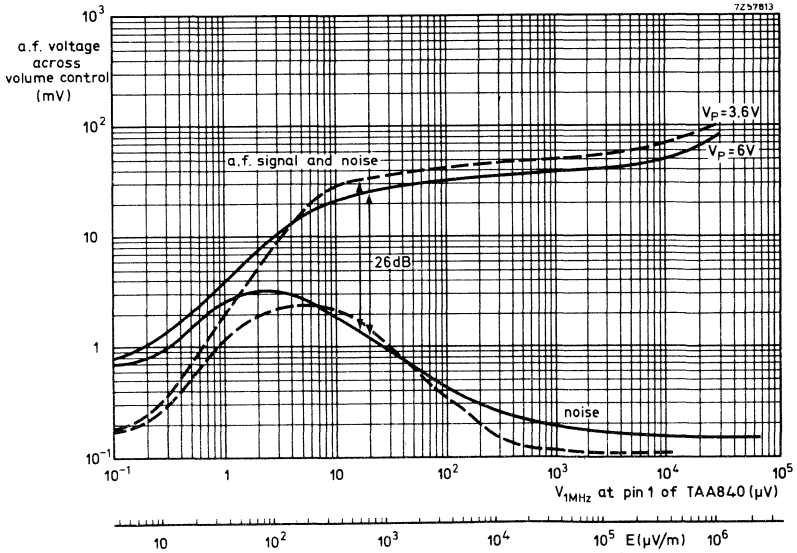


Total harmonic distortion of the audio part versus a.f. output power at 1 kHz

APPLICATION INFORMATION (continued)



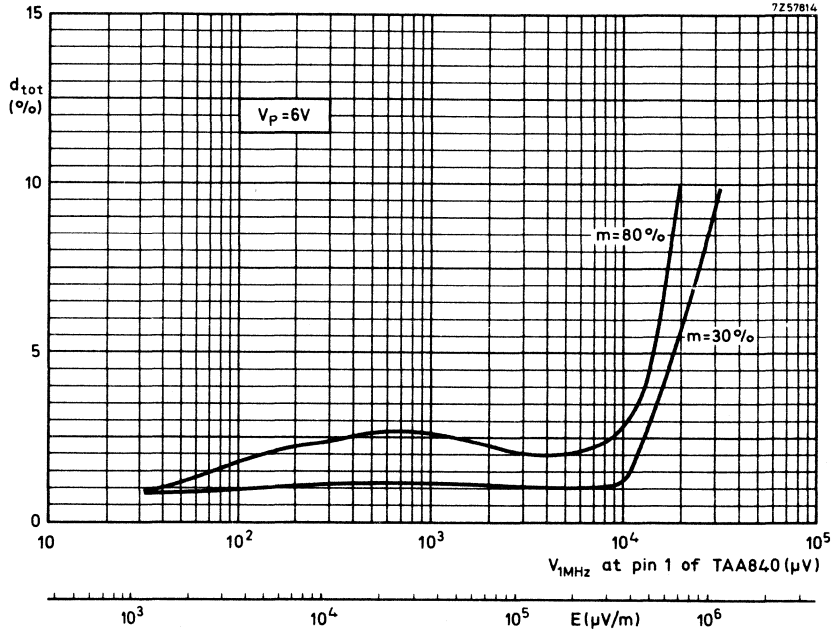
Current flowing through lead (pin 13) in which tuning indicator may be inserted versus r.f. input voltage and field strength. [1])



A.F. signal and noise voltage across volume control and a.f. noise voltage across volume control versus r.f. input voltage and field strength. [1])

[1]) Field strength scale valuable for ferrite aerial of 200 mm length and 10 mm diameter; R.F. input signal 30% modulated with 1 kHz sine wave.

APPLICATION INFORMATION (continued)



Total harmonic distortion of the h.f. part measured across volume control versus r.f input voltage and field strength.
Input signal 30% and 80% modulated with 1 kHz sinewave.
Field strength scale valuable for ferrite aerial of 200 mm length and 10 mm diameter.

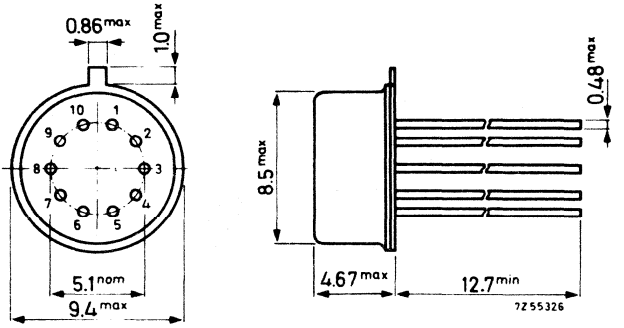
TRIPLE AMPLIFIER FOR ACTIVE FILTERS

The TAA960 consists of three identical general-purpose amplifiers integrated in a single silicon chip. The amplifiers can be used **separately** or can be cascaded to give a voltage gain of 117 dB. One of the amplifiers has an additional emitter-follower stage. The TAA960 is very suitable for use in an active RC band-pass filter with Q up to 60.

QUICK REFERENCE DATA				
Supply voltage	V_{3-10}	nom.	6	V
Supply current	I_3	typ.	2	mA
Transfer admittance (each amplifier)	$\|y_{fs}\|$	typ.	9.5	$m\Omega^{-1}$
Voltage gain (each amplifier)	G_v	typ.	39	dB
Input resistance (on pins 1, 7 and 8)	R_i	>	25	kΩ
Output resistance (on pins 2, 5 and 6)	R_o	typ.	9	kΩ
(on pin 4)	R_o	typ.	500	Ω
Q factor (in typical RC filter)	Q	typ.	45	

PACKAGE OUTLINE TO-74; reduced height

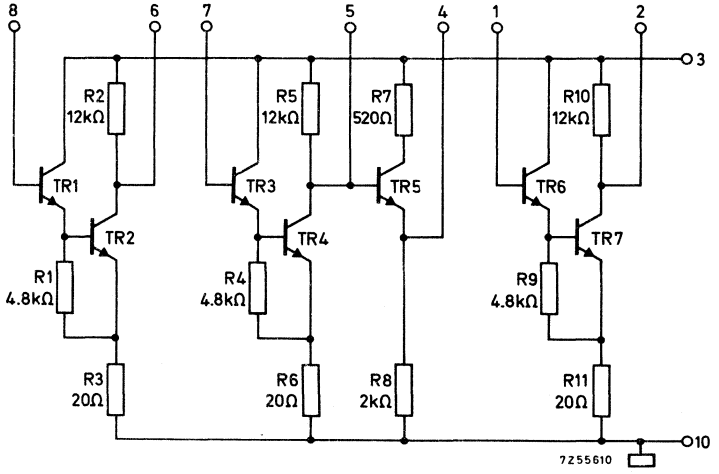
Dimensions in mm



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages with respect to pin 10				
Supply voltage [1])	V_3	max.	10	V
Input voltage	V_8, V_7, V_1	max.	4	V
Output voltage	V_6, V_5, V_4, V_2	max.	10	V
Currents				
Input current	I_8, I_7, I_1	max.	50	μA
Total power dissipation	P_{tot}	max.	250	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +125		°C
Operating ambient temperature	T_{amb}	−55 to + 65		°C

CIRCUIT DIAGRAM



[1]) With lower d.c. potential on all other terminals.

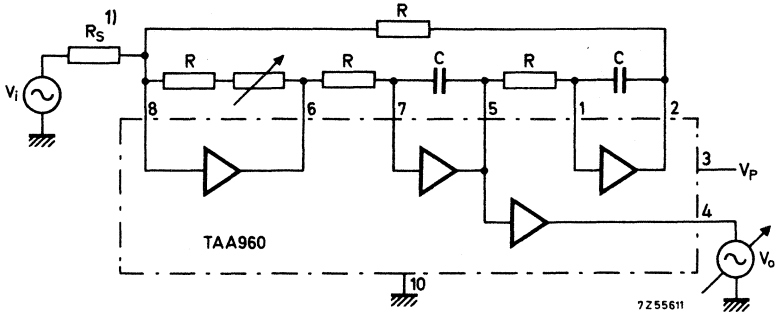
CHARACTERISTICS at V_3 = 6 V; T_{amb} = 25 °C unless otherwise specified.

Supply current [1])	I_3		1.5 to 2.5	mA
		typ.	2.0	mA
Supply current [1]) at V_3 = 10 V	I_3		1.5 to 3.8	mA
		typ.	2.6	mA
Voltage gain (each amplifier)	G_v		60 to 150	
		typ.	90	
Input resistance (each amplifier)	R_i	>	25	kΩ
Output resistance on terminals 2, 5 and 6	R_o	>	8	kΩ
		typ.	9	kΩ
on terminals 4	R_o		135 to 750	Ω

[1]) Terminal 8 connected to terminal 6
" 7 " " " 5
" 1 " " " 2

APPLICATION INFORMATION

Active RC filter for frequencies up to 150 kHz



R = 10 kΩ

Frequency	f	typ.	$\frac{1}{2\pi RC}$	
Supply voltage	V_P	typ.	6	V
Filter performance				
at T_{amb} = 25 °C	Q	typ.	40 to 55	
			45	
at T_{amb} = −30 to +65 °C	Q		35 to 55	
Input voltage	V_i	typ.	400	mV
Output voltage	V_o	typ.	400	mV
Distortion at V_o = 350 mV	d_{tot}	typ.	2	%
S/N ratio at V_o = 400 mV	S/N	>	50	dB
Input resistor 1)	R_S	typ.	470	kΩ

1) Value of input resistor to be determined for $\frac{V_o}{V_i}$ = 0.90 to 1.1.

MICROPHONE AMPLIFIER

The TAA970 is a monolithic integrated microphone amplifier for use in telephone systems. It is compatible with both piezo-electric and dynamic microphones of suitable impedance and sensitivity.

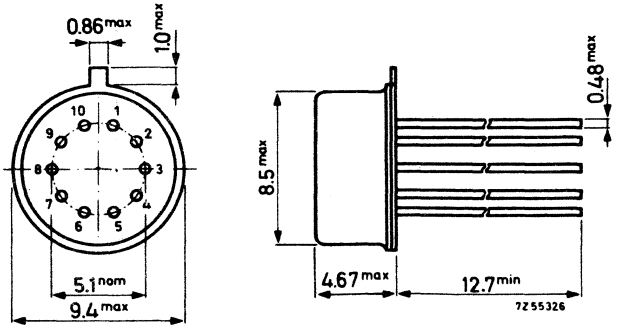
Special features are:

- almost constant voltage gain and d.c. voltage drop with supply current variations of 10 to 100 mA
- output voltage before limiting: 1 V (r.m.s. value)
- operation is independent of supply voltage polarity
- gain can be set to either of two values
- only one external capacitor required
- output impedance determined by internal feed back

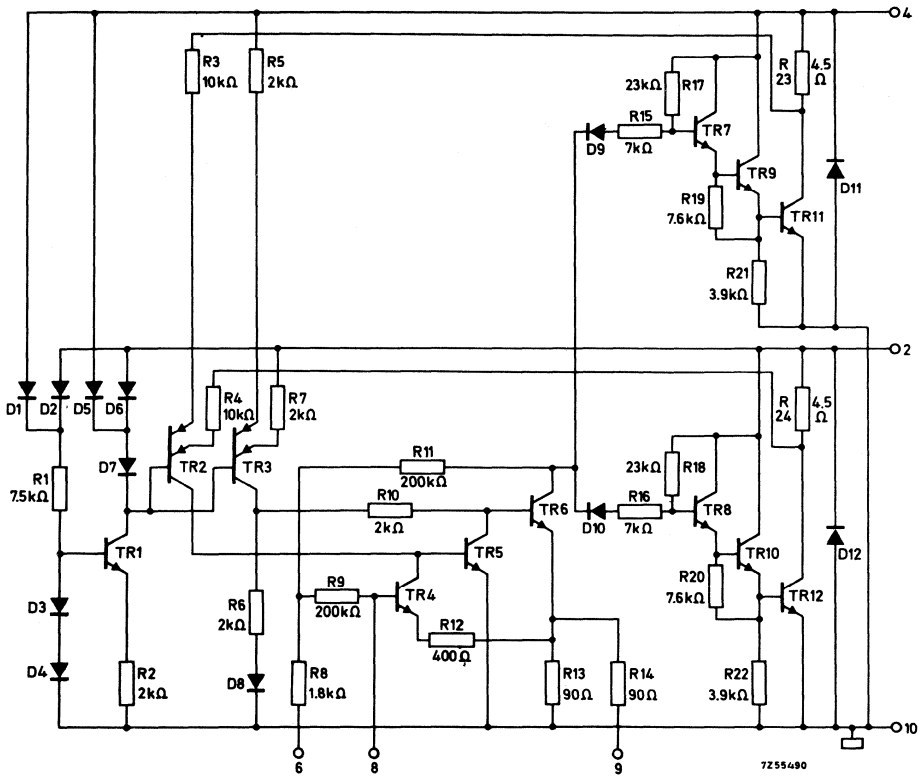
QUICK REFERENCE DATA			
Supply current	$\pm I_2$	10 to 100	mA
Supply voltage drop	$\pm V_{2-4}$	typ. 4.8	V
Voltage gain			
pin 9 not connected	G_V	typ. 130	
pin 9 connected to pin 10	G_V	typ. 180	
Output impedance			
pin 9 not connected	R_O	typ. 80	Ω
pin 9 connected to pin 10	R_O	typ. 115	Ω

PACKAGE OUTLINE

TO-74 (reduced height) Dimensions in mm



CIRCUIT DIAGRAM



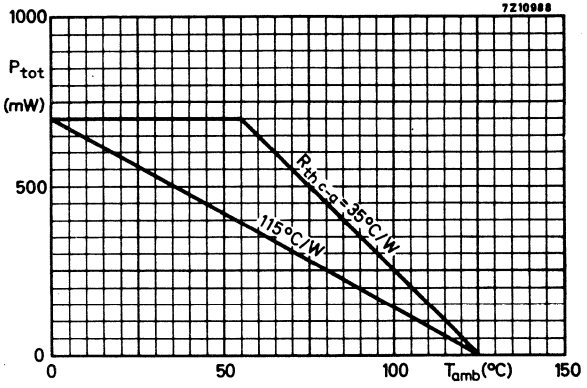
RATINGS Limiting values in accordance to the Absolute Maximum System (IEC 134).

Currents

Supply current (d.c.)	I_2	-100 to +100		mA
A.C. component of supply current (peak value)	I_{2m}	max.	100	mA
Pin No.6 current	I_6	max.	100	μA
Pin No.8 current	I_8	max.	100	μA

Power dissipation

Total power dissipation	P_{tot}	max.	700	mW



Temperatures

Storage temperature	T_{stg}	-55 to +125		°C
Operating ambient temperature	T_{amb}	-35 to + 75		°C

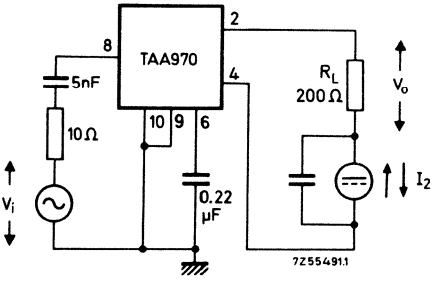
THERMAL RESISTANCE

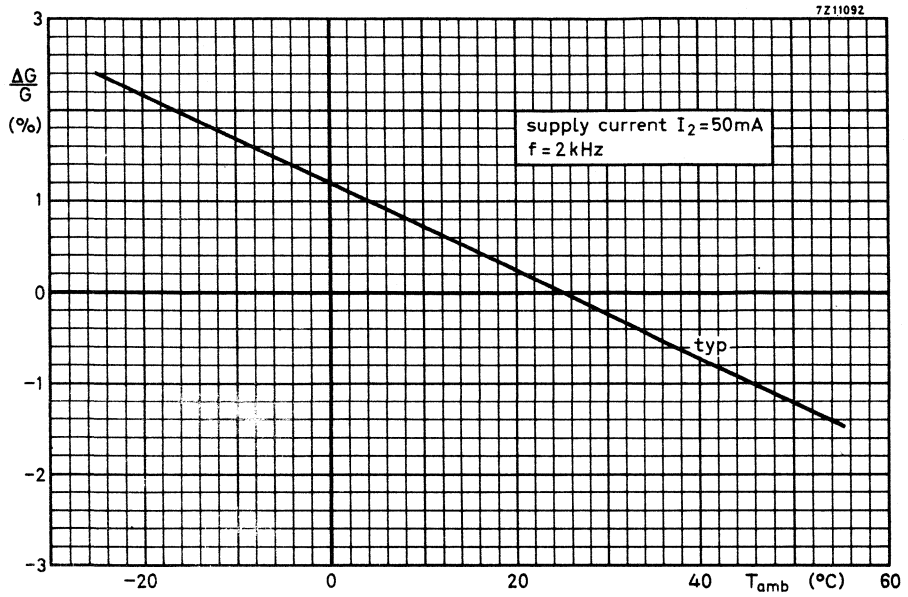
From junction to case	$R_{th\ j-c}$	=	65	°C/W

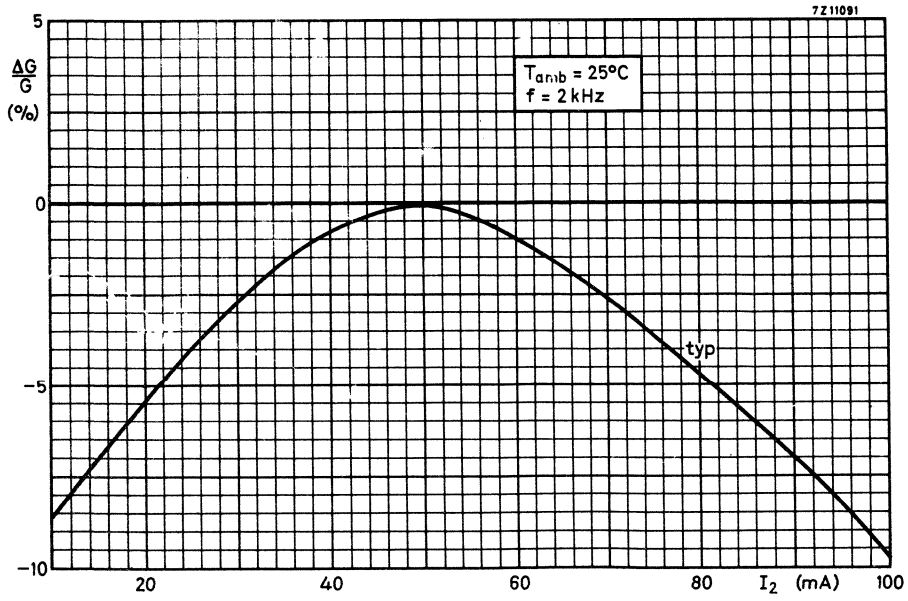
CHARACTERISTICS at R_L = 200Ω; f = 2 kHz; T_{amb} = 25 °C unless otherwise specified. (see test circuit below).

Supply voltage drop at $R_{th\ j-a}$ = 100 °C/W				
$\pm I_2$ = 10 mA	$\pm V_{2-4}$	<	5.4	V
$\pm I_2$ = 50 mA	$\pm V_{2-4}$	typ.	4.5	V
		<	5.8	V
$\pm I_2$ = 100 mA	$\pm V_{2-4}$	<	6.3	V
Voltage gain				
pin 9 not connected, $\pm I_2$ = 10 mA	G_V	105 to 155		
pin 9 not connected, $\pm I_2$ = 50 mA	G_V	typ.	130	
		105 to 155		
pin 9 connected to pin 10, $\pm I_2$ = 10 mA	G_V	135 to 200		
pin 9 connected to pin 10, $\pm I_2$ = 50 mA	G_V	typ.	180	
		150 to 200		
Change of voltage gain				
due to change of supply voltage polarity	ΔG_V	<	10	%
Gain reduction at f = 300 Hz (with respect to f = 2 kHz)	ΔG_V	typ.	1	dB
		<	3	dB
Output impedance at $\pm I_2$ = 50 mA				
pin 9 not connected	R_o	typ.	80	Ω
pin 9 connected to pin 10	R_o	typ.	115	Ω
Noise output voltage at B = 0.3 kHz to 4 kHz				
pin 9 not connected	$V_{n(rms)}$	<	1	mV
pin 9 connected to pin 10	$V_{n(rms)}$	<	1.3	mV
Output voltage				
I_2 = 50 mA; d_{tot} = 5%	V_o	>	0.7	V
		typ.	1.0	V

Test circuit:




7Z11092
3
ΔG/G (%)
1
0
−1
−2
−3
supply current I_2 = 50mA
f = 2kHz
typ
−20
0
20
40
T_{amb} (°C)
60


7Z11091
5
ΔG/G (%)
0
−5
−10
T_{amb} = 25°C
f = 2kHz
typ
20
40
60
80
I_2 (mA)
100

RING (DE)MODULATOR FOR TELEPHONY AND INDUSTRIAL EQUIPMENT

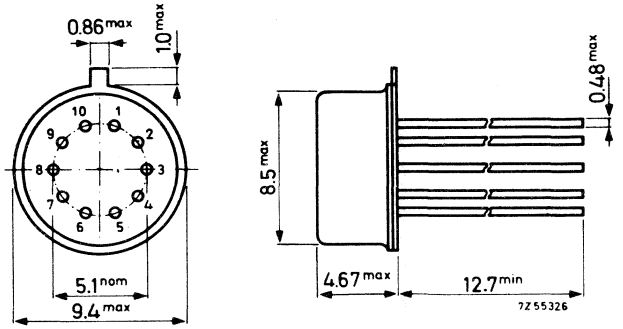
The TAB101 is a monolithic integrated circuit comprising a 4-transistor modulator and demodulator circuit. The circuit being made on a single crystal ensures a great similarity in characteristics of the transistors and optimal tracking of their parameters with temperature variations. Consequently, the TAB101 gives a better balancing and therefore less carrier leakage than a conventional circuit. The use of transistors instead of diodes provides a better isolation between input and output circuits.

QUICK REFERENCE DATA				
Collector cut-off current V_{CB} = 5 V; T_{amb} = 25 °C	I_{CBO}	<	100	nA
Base-emitter voltage differences between transistors 1, 2, 3, 4 V_{CB} = 5 V; $-I_E$ = 150 μA	$\lvert V_{BE1}-V_{BE2} \rvert$	<	5	mV
	$\lvert V_{BE3}-V_{BE4} \rvert$	<	5	mV
Common-base current gain differences between transistors 1, 2, 3, 4 V_{CB} = 5 V; $-I_E$ = 150 μA	$\lvert h_{FB1}-h_{FB2} \rvert$	<	0.008	
	$\lvert h_{FB3}-h_{FB4} \rvert$	<	0.008	

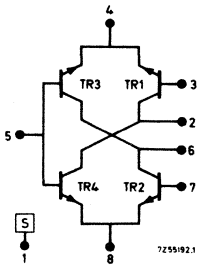
PACKAGE OUTLINE

Dimensions in mm

TO-74 (reduced height)



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (each transistor)

Collector-base voltage (open emitter)	V_{CBO}	max.	10	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V
Collector-substrate voltage	V_{CS}	max.	12	V

Currents (each transistor)

Collector current	I_C	max.	10	mA

Power dissipation (4 transistors)

Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	100	mW

Temperatures

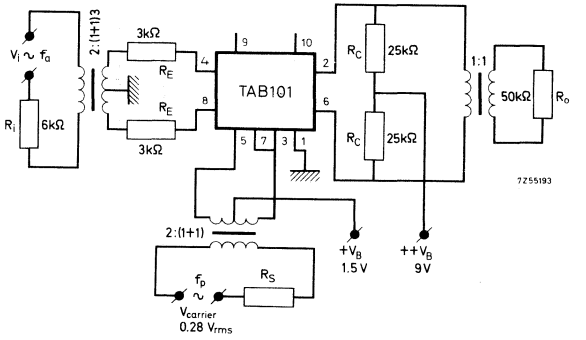
Storage temperature	T_{stg}	−35 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +100	°C

CHARACTERISTICS (each transistor) T_{amb} = 25 °C

Collector cut-off current				
I_E = 0; V_{CB} = 5 V	I_{CBO}	typ. <	5 100	nA nA
Collector-substrate leakage current				
V_{CS} = 9.5 V	I_{CS}	typ. <	5 100	nA nA
Emitter cut-off current				
I_C = 0; V_{EB} = 1 V	I_{EBO}	typ. <	5 100	nA nA
Break down voltages				
I_E = 0; I_C = 10 μA	$V_{(BR)CBO}$	>	10	V
I_B = 0; I_C = 10 μA	$V_{(BR)CEO}$	>	9	V
$-I_S$ = 10 μA	$V_{(BR)CS}$	>	12	V
I_C = 0; I_E = 200 μA	$V_{(BR)EBO}$	>	5	V
D.C. current gain				
I_C = 150 μA; V_{CE} = 5 V	h_{FE}	> typ.	20 75	
Spot noise figure at f = 1 kHz				
$-I_E$ = 150 μA; V_{CB} = 5 V				
R_S = 1 kΩ; Bandwidth: 200 Hz		typ.	6	dB
Base-emitter voltage difference				
between transistors TR1 and TR2 at				
$-I_{E1} = -I_{E2}$ = 150 μA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert V_{BE1}-V_{BE2}\rvert$	typ. <	2 5	mV mV
between transistors TR3 and TR4 at				
$-I_{E3} = -I_{E4}$ = 150 μA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert V_{BE3}-V_{BE4}\rvert$	typ. <	2 5	mV mV
Current amplification factor difference				
between transistors TR1 and TR2 at				
$-I_{E1} = -I_{E2}$ = 150 μA; $V_{CB1} = V_{CB2}$ = 5 V	$\lvert h_{FB1}-h_{FB2}\rvert$	typ. <	0.002 0.008	
between transistors TR3 and TR4 at				
$-I_{E3} = -I_{E4}$ = 150 μA; $V_{CB3} = V_{CB4}$ = 5 V	$\lvert h_{FB3}-h_{FB4}\rvert$	typ. <	0.002 0.008	

APPLICATION INFORMATION

Telephony carriers ring modulator



Performance at T_{amb} = 25 °C

Conversion gain at f_a = 1 kHz, V_i = 0.4 V; f_p = 34 kHz	G_c	typ.	−0.75	dB
Carrier leakage power in R_o at f_p = 34 kHz	P_{oc}	typ.	3	nW

INTEGRATED A.M.-RADIO RECEIVER CIRCUIT

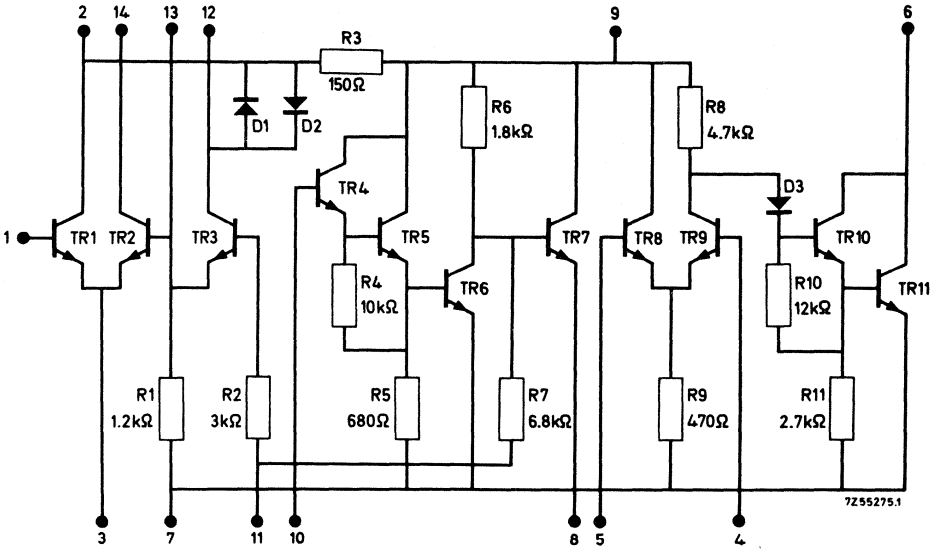
The TAD100 is a monolithic integrated circuit, primarily intended for a.m.-radio receivers. The circuit incorporates the mixer, oscillator, i.f. amplifier, a.g.c., detector, audio pre-amplifier and driver stages. The audio output transistors are not included. This enables the use of different power output stages to suit individual receiver requirements. The frequency response of the circuit is such that the front half of the circuit may be used as part of an i.f. amplifier at 10.7 MHz for f.m. receivers.

QUICK REFERENCE DATA

Ambient temperature	T_{amb}		25		°C
Supply voltages	V_P	nom.	6.0	9.0	V
Output power at d_{tot} = 10% (with AC187/AC188)		typ.	0.7	1.5	W
Total quiescent current (except output stages)		typ.	15	23	mA
R.F. input signal level (at pin 1) for a signal to noise ratio of 26 dB		typ.	30	25	μV
A.G.C. range (change in R.F. input voltage for 10 dB expansion in audio range)		typ.	62	62	dB
R.F. signal handling (at pin 1)		typ.	30	30	mV
Harmonic distortion of h.f. part (over most of a.g.c. range)		<	2.5	2.5	%

PACKAGE OUTLINE; 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Pin No. 6 voltage	V_{6-7}	max.	12	V
Pin No. 2 voltage	V_{2-7}	max.	9	V
Pin No. 9 voltage (via 150 Ω)	V_{9-7}	max.	9	V
Currents				
Pin No. 6 current (peak value)	I_{6M}	max.	30	mA
Pin No. 6 average current	I_{6AV}	max.	20	mA
Power dissipation				
Total power dissipation	P_{tot}	max.	150	mW
Temperatures				
Storage temperature	T_{stg}	−25 to +85		°C
Operating ambient temperature	T_{amb}	−10 to +55		°C

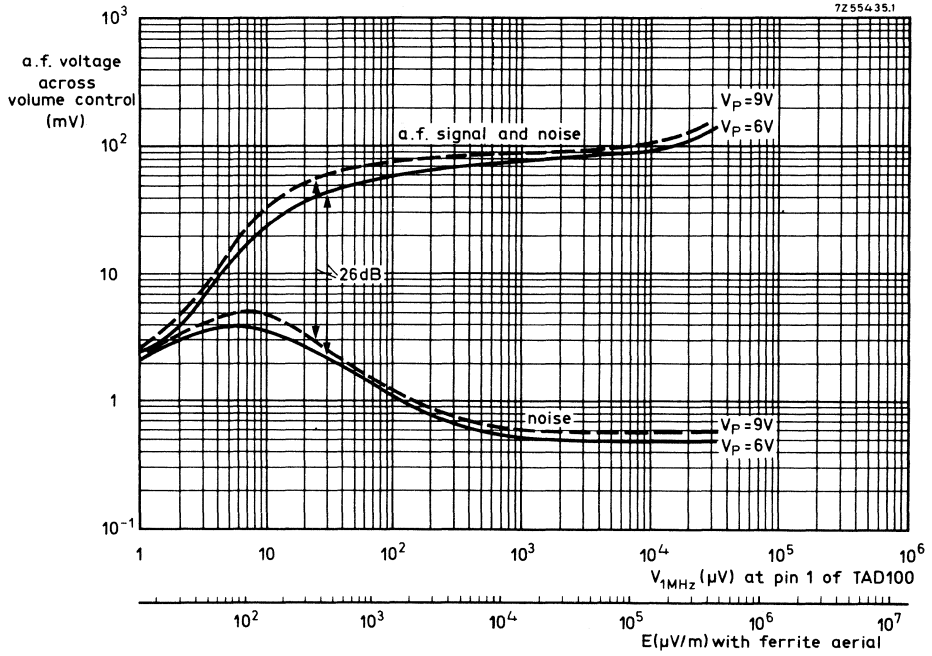
CHARACTERISTICS at T_{amb} = 25 °C

A.F. driver saturation voltage		
I_C = 30 mA	typ.	0.82 V
	<	1.0 V
I_C = 1.0 mA	>	0.70 V

Measured in the circuit on page 5:	V_P = 9	6 V
Output power at d_{tot} = 10% (with AC187/AC188)	typ. 1.5	0.7 W
Total receiver current drain	17 to 26	11 to 15 mA
(excepting the output matched pair AC187/AC188)	typ. 20	13 mA
R.F. input voltage (at pin 1) for a signal to noise ratio of 26 dB	typ. 25	30 μV [1]
A.G.C. range(change in r.f. input voltage for 10 dB expansion in audio range)	typ. 62	62 dB [1]
Harmonic distortion of h.f. part (over most of a.g.c. range)	< 2.5	2.5 % [1]
Signal handling: R.F. input voltage (at pin 1) to obtain 10% distortion at 80% modulation; f_m = 400 Hz ; R.F. = 1 MHz	typ. 30	30 mV
R.F. input voltage (at pin 1)	typ. 3.3	5 μV [1]
for 10 mV a.f. at detector load	< 6.0	10 μV [1]
A.F. voltage at detector load	> 30	30 mV [1]
for 100 μV r.f. at pin 1	typ. 50	50 mV [1]
Signal to noise ratio for r.f. input voltage of 1 mV (at pin 1)	typ. 40	41 dB [1]
A.F. voltage (at pin 4) for 50 mW output power	< 5.0	5.0 mV
Loss of overall receiver sensitivity for 50 mW output power at cell voltage of 0.9 V	typ. 7	11 dB [1]
Oscillator voltage at pin 13 (r.m.s. value) at a battery voltage of 3.6 V to 9 V	> 95	95 mV
Oscillator-frequency shift at 2 MHz over a.g.c. range	< 350	350 Hz
Oscillator-frequency shift at 2 MHz over range of supply voltage	typ. 300	300 Hz
Typical overall fidelity (flat within 3 dB)		120 to 2000 Hz

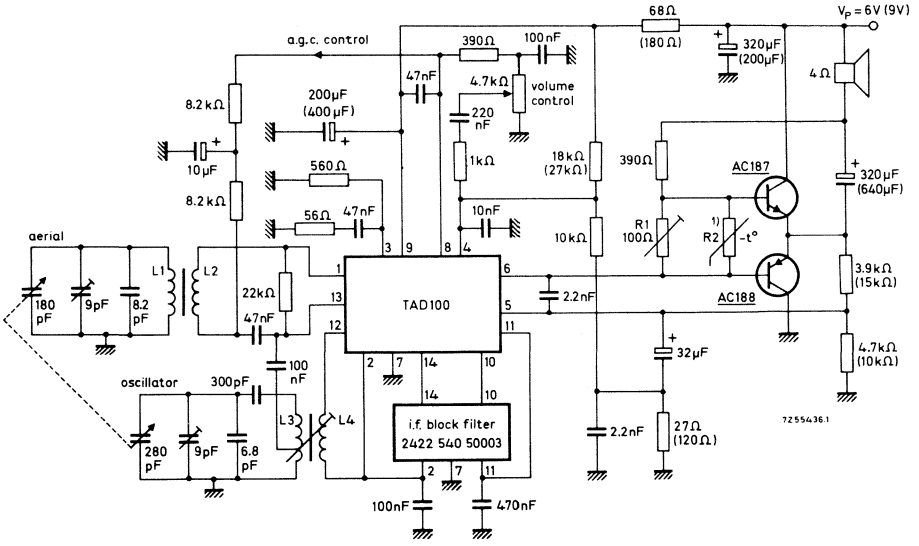
[1]) R.F. = 1 MHz; 30% modulation; f_m = 400 Hz

CHARACTERISTICS (continued)



APPLICATION INFORMATION

Medium-wave receiver using the TAD100



Medium wave aerial coil:

L1 = 310 µH; Q_{loaded} = 100 at 1 MHz; FXC rod for 2 MHz

$$\frac{V_{L1}}{V_{L2}} \approx 11$$

Medium wave oscillator coil:

L3 = 165 µH; Q_0 = 100 at 1.4 MHz; tapping ratio L3 $\approx \frac{1}{46}$

$$\frac{V_{L3}}{V_{L4}} \approx 9$$

Quiescent current (adjusted by R1): 5 mA

Modification for 9 V supply voltage:

Values in brackets refer only to a 9 V supply, the others apply to 6 V and 9 V supplies.

AC187 and AC188 with cooling clip 56227 on 1.5 mm blackened Al. heatsinks of 9 cm^2.

APPLICATION INFORMATION bulletins available on request

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1) For 6 V supply: 130 Ω; disk type NTC resistor (2322 610 90004)
For 9 V supply: 50 Ω; disk type NTC resistor on metal strip (2322 610 90016)

OPERATIONAL AMPLIFIER

The TBA221 is a silicon monolythic integrated operational amplifier for use at temperatures from 0 to 70 °C. Special features are:

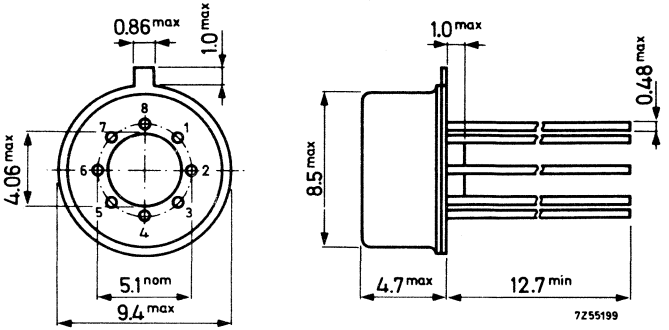
- no frequency compensation required
- continuous short circuit protection
- offset voltage adjustable to zero
- large input voltage range
- low power consumption
- no latch up

The TBA221 is equivalent to 741C.

QUICK REFERENCE DATA				
Positive supply voltage	V_P		15	V
Negative supply voltage	$-V_N$		15	V
Characteristics at T_{amb} = 25 °C				
Voltage gain at $R_L \geq 2$ kΩ; $V_o = \pm 10$ V	G_v	typ.	100.000	
Common mode rejection ratio	CMRR	typ.	90	dB
Differential input resistance	R_i	typ.	1	MΩ
Peak output voltage swing at R_L = 10 kΩ	V_{OM}	>	±12	V
Input voltage range	V_i	>	±12	V
Power dissipation	P_{tot}	typ.	50	mW

PACKAGE OUTLINE TO-99

Dimensions in mm



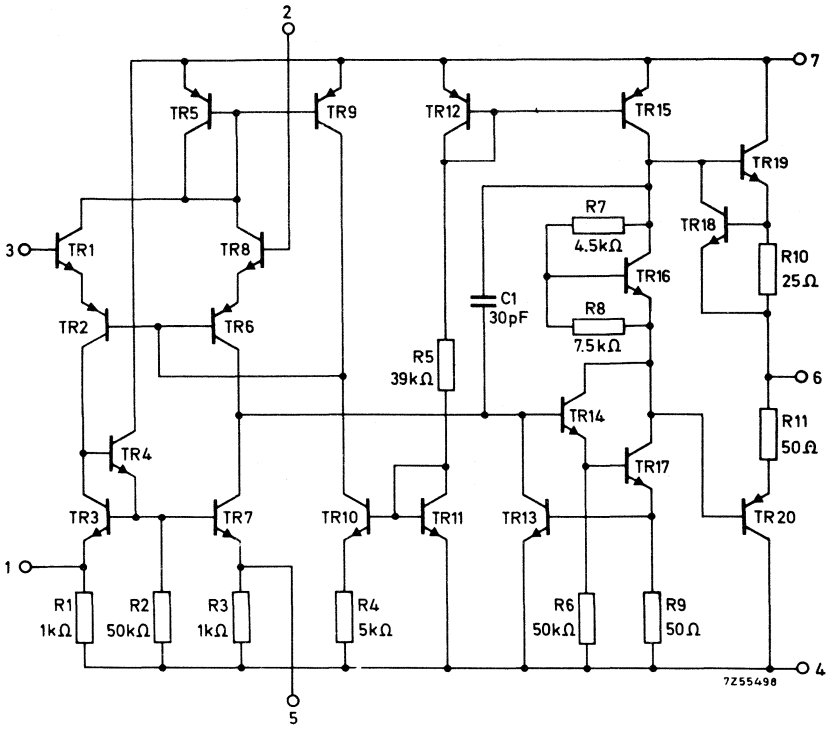
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Positive supply voltage	V_P	max.	18	V
Negative supply voltage	$-V_N$	max.	18	V
Common mode input voltage [1]	V_i	max.	±15	V
Differential input voltage	V_{2-3}	max.	±30	V
Power dissipation	P_{tot}	max.	500	mW
Output short circuit duration [2]		indefinite		
Temperatures				
Operating ambient temperature	T_{amb}	0 to +	70	°C
Storage temperature	T_{stg}	− 65 to +	150	°C

1) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

2) Continuous short circuit is allowed to ground or either supply.

CIRCUIT DIAGRAM



CHARACTERISTICS at V_P = 15 V: $-V_N$ = 15 V: T_{amb} = 25°C unless otherwise specified

Voltage gain; $R_L \geq 2$ kΩ: $V_O = \pm 10$ V	G_v	>	20.000	
		typ.	100.000	
Input offset voltage; $R_S \leq 10$ kΩ	V_{io}	typ.	2.0	mV
		<	6.0	mV
Input bias current	I_i	typ.	0.2	μA
		<	0.5	μA
Input offset current	I_{io}	typ.	30	nA
		<	0.2	μA
Common mode rejection ratio; $R_S \leq 10$ kΩ	CMRR	>	70	dB
		typ.	90	dB
Input voltage range	V_i	>	±12	V
		typ.	±13	V
Differential input resistance	R_i	>	0.3	MΩ
		typ.	1	MΩ
Supply voltage rejection ratio; $R_S \leq 10$ kΩ	SVRR	typ.	30	μV/V
		<	150	μV/V
Peak output voltage swing at $R_L \geq 10$ kΩ	V_{OM}	>	±12	V
		typ.	±14	V
$R_L \geq 2$ kΩ	V_{OM}	>	±10	V
		typ.	±13	V
Power dissipation at $V_O = 0$	P_{tot}	typ.	50	mW
		<	85	mW

Transient response (unity gain)

V_i = 20 mV; R_L = 2 kΩ; C_L = 100 pF

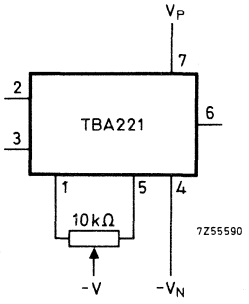
Rise time	typ.	0.3	μs
Overshoot	typ.	5.0	%

Slew rate (unity gain)

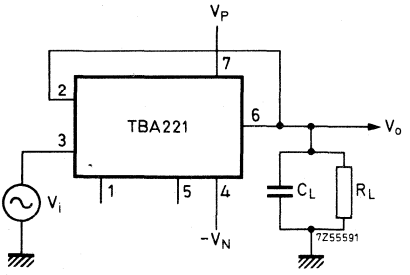
$R_L \geq 2$ kΩ	typ.	0.5	V/μs

CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 0 to 70 °C unless otherwise specified

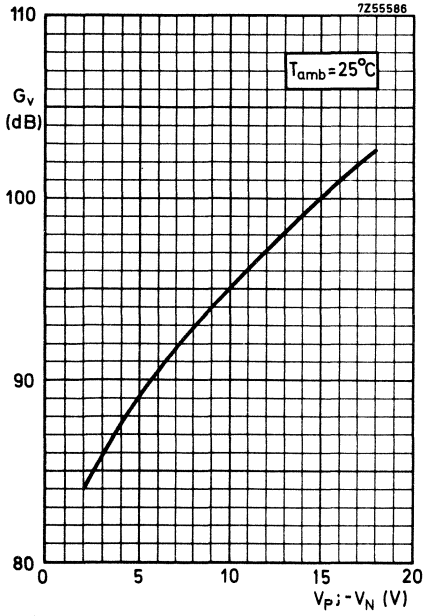
Voltage gain; $R_L \geq 2$ kΩ; $V_o = \pm 10$ V	G_v	>	15.000	
Input offset voltage; $R_S \leq 10$ kΩ;	V_{io}	<	7.5	mV
Input bias current	I_i	<	0.8	μA
Input offset current	I_{io}	<	0.3	μA
Peak output voltage swing; $R_L \geq 2$ kΩ	V_{OM}	>	±10	V

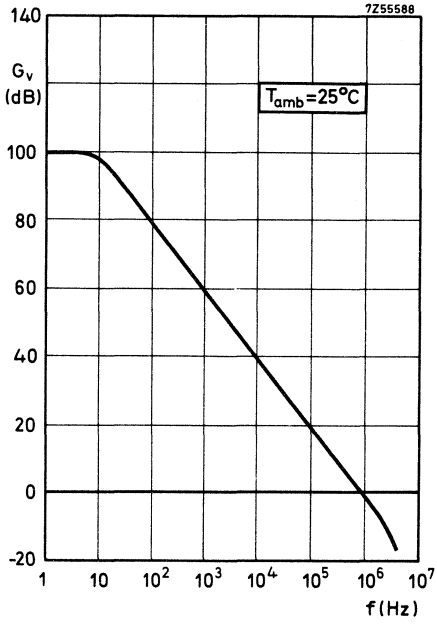


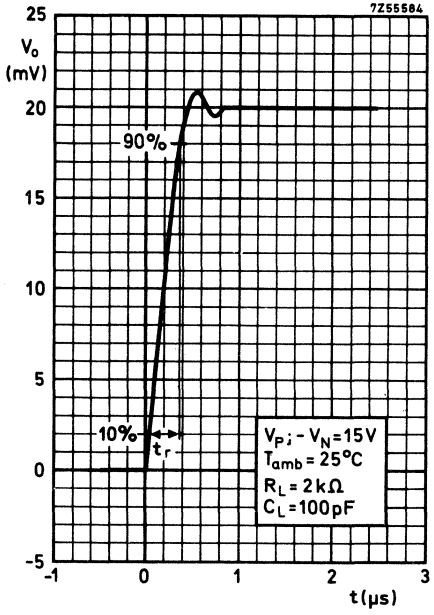
Offset voltage zeroing circuit



Transient response test circuit


7Z55586
110
100
90
80
G_v
(dB)
T_{amb}=25°C
0
5
10
15
20
$V_{P;}$ - V_N (V)


7Z55588
140
100
80
60
40
20
0
-20
G_v
(dB)
T_{amb}=25°C
1
10
10^2
10^3
10^4
10^5
10^6
10^7
f(Hz)


7Z55584
25
20
15
10
5
0
-5
V_o
(mV)
90%
10%
t_r
$V_{P;}$ - V_N=15V
T_{amb} = 25°C
R_L = 2kΩ
C_L=100pF
-1
0
1
2
3
t(μs)

OPERATIONAL AMPLIFIER

The TBA222 is a silicon monolithic integrated operational amplifier for use at temperatures from −55 to +125 °C. Special features are:

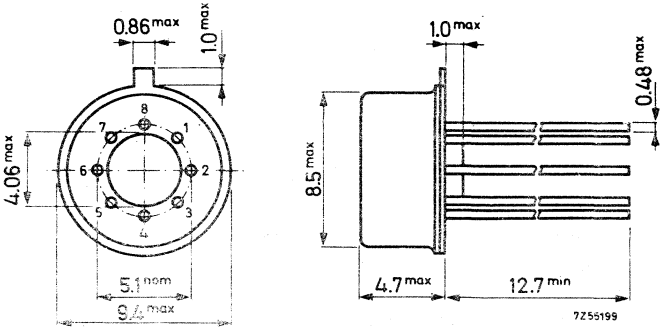
- no frequency compensation required
- continuous short-circuit protection
- offset voltage adjustable to zero
- large input voltage range
- low power consumption
- no latch-up

The TBA222 is equivalent to 741.

QUICK REFERENCE DATA				
Positive supply voltage	V_P		15	V
Negative supply voltage	$-V_N$		15	V
Characteristics at T_{amb} = 25 °C				
Voltage gain at $R_L \geq 2$ kΩ; $V_O = \pm 10$ V	G_v	typ.	200 000	
Common mode rejection ratio	CMRR	typ.	90	dB
Differential input resistance	R_i	typ.	1	MΩ
Peak output voltage swing at $R_L = 10$ kΩ	V_{OM}	>	±12	V
Input voltage range	V_i	>	±12	V
Power dissipation	P_{tot}	typ.	50	mW

PACKAGE OUTLINE TO-99

Dimensions in mm



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

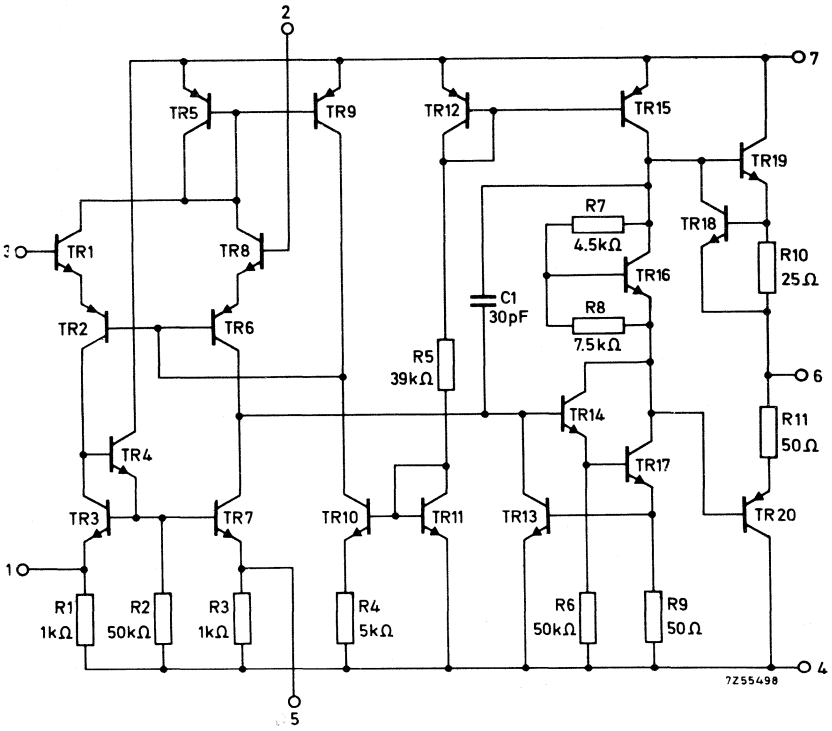
Voltages				
Positive supply voltage	V_P	max.	22	V
Negative supply voltage	$-V_N$	max.	22	V
Common mode input voltage [1]	V_i	max.	±15	V
Differential input voltage	V_{2-3}	max.	±30	V
Power dissipation [2]	P_{tot}	max.	500	mW
Output short circuit duration [3]		indefinite		
Temperatures				
Operating ambient temperature	T_{amb}	−55 to +125		°C
Storage temperature	T_{stg}	−65 to +150		°C

[1]) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

[2]) Rating applies for case temperatures up to 125 °C; derate linearly at 6.5 mW/°C for ambient temperatures above 75 °C.

[3]) Continuous short circuit is allowed for case temperatures up to 125 °C and ambient temperatures up to 70 °C. Short circuit is allowed to ground or either supply.

CIRCUIT DIAGRAM

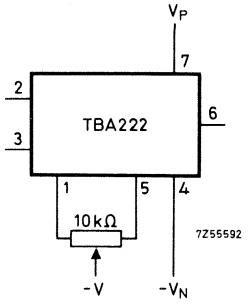


CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = 25 °C unless otherwise specified

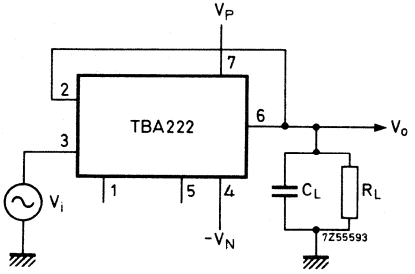
Voltage gain; $R_L \geq$ 2 1Ω; V_O = ± 10 V	G_v	>	50 000	
		typ.	200 000	
Input offset voltage; $R_S \leq$ 10 kΩ	V_{io}	typ.	1.0	mV
		<	5.0	mV
Input bias current	I_i	typ.	0.2	μA
		<	0.5	μA
Input offset current	I_{io}	typ.	30	nA
		<	0.2	μA
Common mode rejection ratio; $R_S \leq$ 10 kΩ	CMRR	>	70	dB
		typ.	90	dB
Input voltage range	V_i	>	±12	V
		typ.	±13	V
Differential input resistance	R_i	>	0.3	MΩ
		typ.	1.0	MΩ
Supply voltage rejection ratio; $R_S \leq$ 10 kΩ	SVRR	typ.	30	μV/V
		<	150	μV/V
Peak output voltage swing at $R_L \geq$ 10 kΩ	V_{OM}	>	±12	V
		typ.	±14	V
$R_L \geq$ 2 kΩ	V_{OM}	>	±10	V
		typ.	±13	V
Power dissipation at V_O = 0	P_{tot}	typ.	50	mW
		<	85	mW
Transient response (unity gain) V_i = 20 mV; R_L = 2 kΩ; $C_L \leq$ 100 pF				
Rise time		typ.	0.3	μs
Overshoot		typ.	5.0	%
Slew rate (unity gain) $R_L \geq$ 2 kΩ		typ.	0.5	V/μs

CHARACTERISTICS at V_P = 15 V; $-V_N$ = 15 V; T_{amb} = −55 to +125 °C unless otherwise specified.

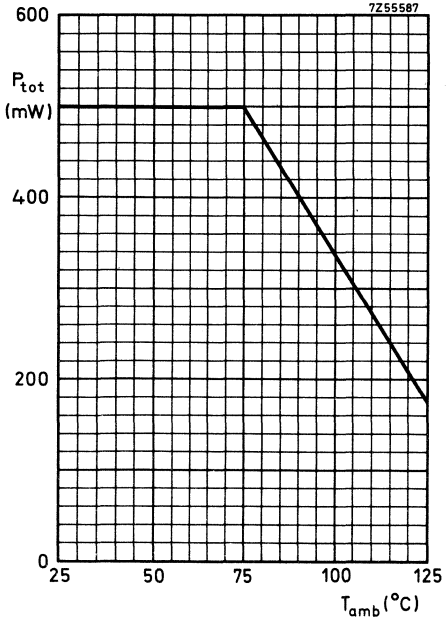
Voltage gain; $R_L \geq 2$ kΩ; V_O = ±10 V	G_v	>	25.000	
Input offset voltage; $R_S \leq 10$ kΩ	V_{io}	<	6	mV
Input bias current	I_i	<	1.5	μA
Input offset current	I_{io}	<	0.5	μA
Peak output voltage swing $R_L \geq 2$ kΩ	V_{OM}	>	±10	V

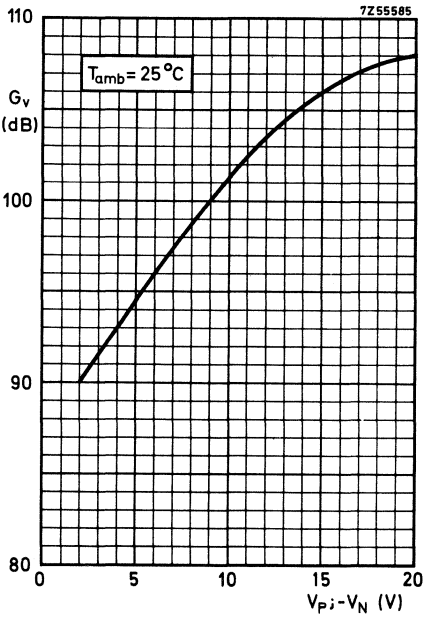


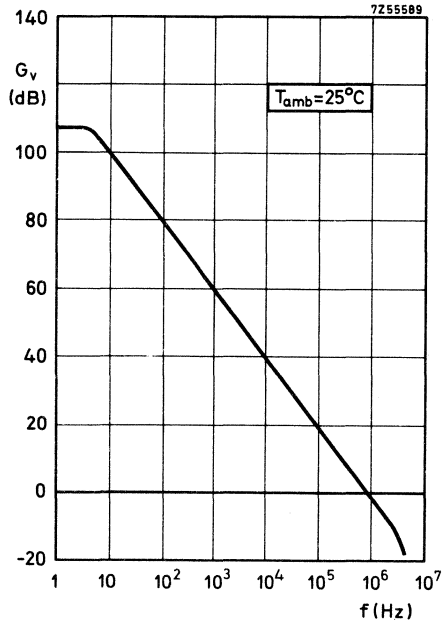
Offset voltage zeroing circuit

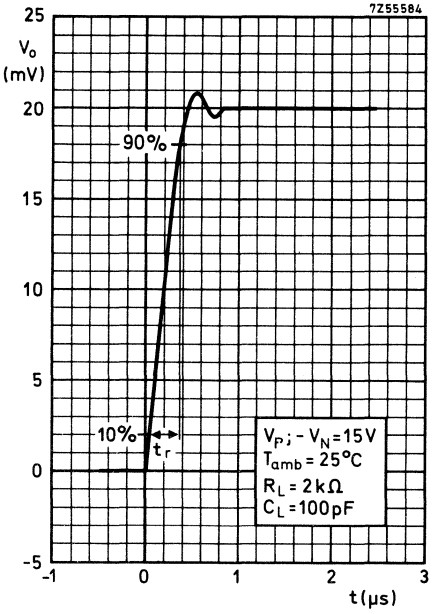


Transient response test circuit


7Z55587
600
400
200
0
P_{tot}
(mW)
25
50
75
100
125
T_{amb} (°C)


7Z55585
110
100
90
80
G_v
(dB)
T_{amb} = 25 °C
0
5
10
15
20
V_{Pi}-V_N (V)


7Z55589
140
100
80
60
40
20
0
-20
G_v
(dB)
T_{amb}=25°C
1
10
10^2
10^3
10^4
10^5
10^6
10^7
f(Hz)


7Z55584
25
20
15
10
5
0
-5
V_o
(mV)
90%
10%
t_r
V_{Pi} - V_N = 15 V
T_{amb} = 25 °C
R_L = 2 kΩ
C_L = 100 pF
-1
0
1
2
3
t(μs)

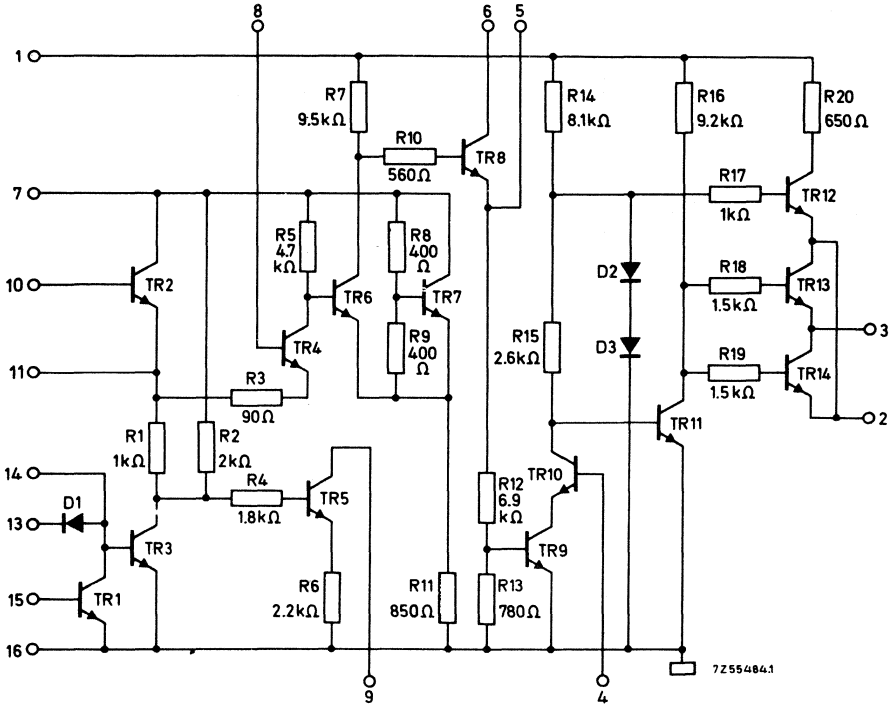
AUTOMATIC LINE SYNCHRONISATION CIRCUIT

The TBA240 is a monolithic integrated noise detector and inverter, sync separator, catching circuit, and line discriminator. It can be used in a wide variety of b-w and colour television receivers and is designed for best operation with negative-modulated video signals but is also compatible with positive modulation. The required supply voltages are +5.5 V and +12 V.

QUICK REFERENCE DATA			
Supply voltages	V_{7-16}	typ. 5.5	V
	V_{1-16}	typ. 12	V
Ambient temperature	T_{amb}	typ. 25	°C
Total average power dissipation	P_{tot}	typ. 100	mW
Required input signals			
Typical composite peak white to peak sync voltage	V_{10-16}	0.5 to 3	V
Negative noise pulse current (peak value)	I_{13M}	> 100	μA
Positive noise pulse current (peak value)	I_{15M}	> 10	μA
Delivered output signals			
Discriminator output voltage (peak to peak value)	$V_{3-16(p-p)}$	< 4	V
Positive going sinc pulse voltage (peak to peak value)	$V_{5-16(p-p)}$	typ. 7.5	V
Negative going noise pulse voltage (peak to peak value)	$V_{9-16(p-p)}$	typ. 2	V
Typical composite video , with inverted noise pulses, peak white to peak sync voltage	V_{11-16}	0.5 to 3	V

PACKAGE OUTLINE : 16 lead quadruple in-line (See page 8)

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Pin No. 1 voltage ($V_{1-16} > V_{7-16}$)	V_{1-16}	max. 13 V [1]
Pin No. 2 voltage	see test circuit on page 5	
Pin No. 3 voltage	do not apply external voltage	
Pin No. 4 voltage (via $R_2 \geq 1$ kΩ)	V_{4-16}	−5 to +1.5 V [2]
Pin No. 6 voltage (connect pin 6 to pin 1, via $R_3 \leq 2$ kΩ); $V_{6-16} > V_{7-16}$	V_{6-16}	max. 13 V [1][2]

[1] Tolerated minimum voltage: 0 V

[2] See test circuit on page 5.

RATINGS (continued)

Pin No. 7 voltage	V_{7-16}	max.	7	V [1]
Pin No. 8 voltage (connect pin 8 to pin 7, via R4 > 50 kΩ)	V_{8-16}	max.	7	V [1]
Pin No. 9 voltage (connect pin 9 to pin 7, via R5 < 10 kΩ)	V_{9-16}	max.	7	V [1]
Pin No. 10 voltage (via R6 > 2 kΩ) $V_{10-16} < V_{7-16}$	V_{10-16}	max.	7	V [1]
Pin No. 11 voltage	do not apply external voltage			
Pin No. 12 voltage	do not connect			
Pin No. 13 voltage (via R_7 > 1 kΩ)	V_{13-16}	−1 to	+5	V
Pin No. 15 voltage	$-V_{15-16}$	max.	5	V
Currents				
Pin No. 5 current	I_5	−5 to	+0.5	mA
Pin No. 11 current	$\pm I_{11}$	max.	250	μA
Pin No. 13 current	$-I_{13}$	max.	1	mA [2]
Pin No. 14 current	$\pm I_{14}$	max.	1	mA
Pin No. 15 current	I_{15}	max.	1	mA
Total power dissipation	P_{tot}	max.	260	mW [3]
Temperatures				
Operating ambient temperature	T_{amb}	0 to	+60	°C
Storage temperature	T_{stg}	−25 to	+125	°C

[1]) Tolerated minimum voltage: 0 V

[2]) Tolerated minimum current: 0 mA

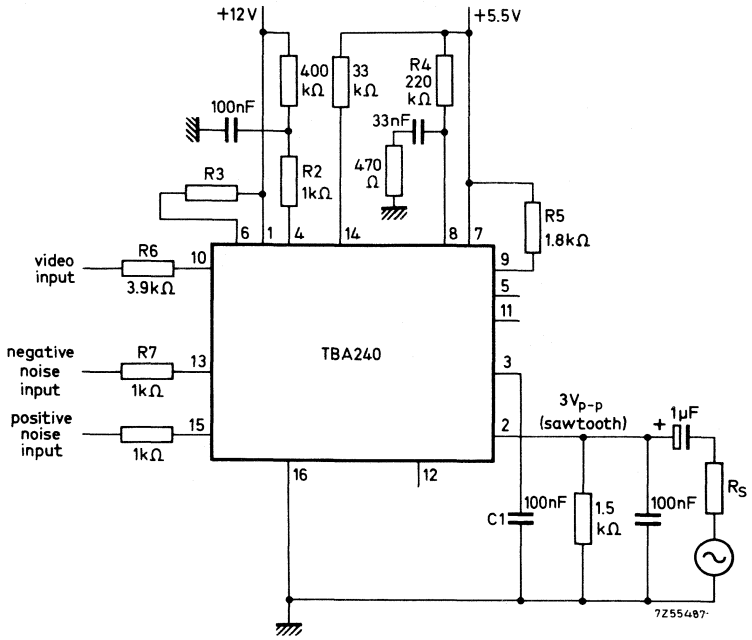
[3]) Derated from $T_{amb} \geq 60$ °C with 4 mW/°C.

CHARACTERISTICS at T_{amb} = 25 °C; V_{7-16} = 5.5 V; V_{1-16} = 12 V

Total average power dissipation	P_{tot}	typ.	100	mW
Required input signals				
Typical composite peak white to peak sync voltage	V_{10-16}		0.5 to 3	V
Negative noise pulse current (peak value)	I_{13M}	≥	100	μA
Positive noise pulse current (peak value)	I_{15M}	≥	10	μA
Delivered output signals				
Discriminator output voltage (peak to peak value)	$V_{3-16(p-p)}$	≤	4	V
Positive going sync pulse voltage (peak to peak voltage)	$V_{5-16(p-p)}$	typ.	7.5	V
Negative going noise pulse voltage (peak to peak value)	$V_{9-16(p-p)}$	typ.	2	V
Typical composite video, with inverted noise pulses, peak white to peak sync voltage (to be utilized if external frame sync is applied)	V_{11-16}		0.5 to 3	V
Frequency response for signal voltages:				
V_{2-16}, V_{5-16} and V_{9-16} with respect to V_{10-16}	$t_{pdr} + t_r$	≤	600	ns
	$t_{pdf} + t_f$	≤	600	ns
Symmetry fault in discriminator				
Pin No. 2 and No. 3 voltage difference (for symmetrical saw tooth of 3 V_{p-p})	$V_{2-16} - V_{3-16}$	≤	0.2	V

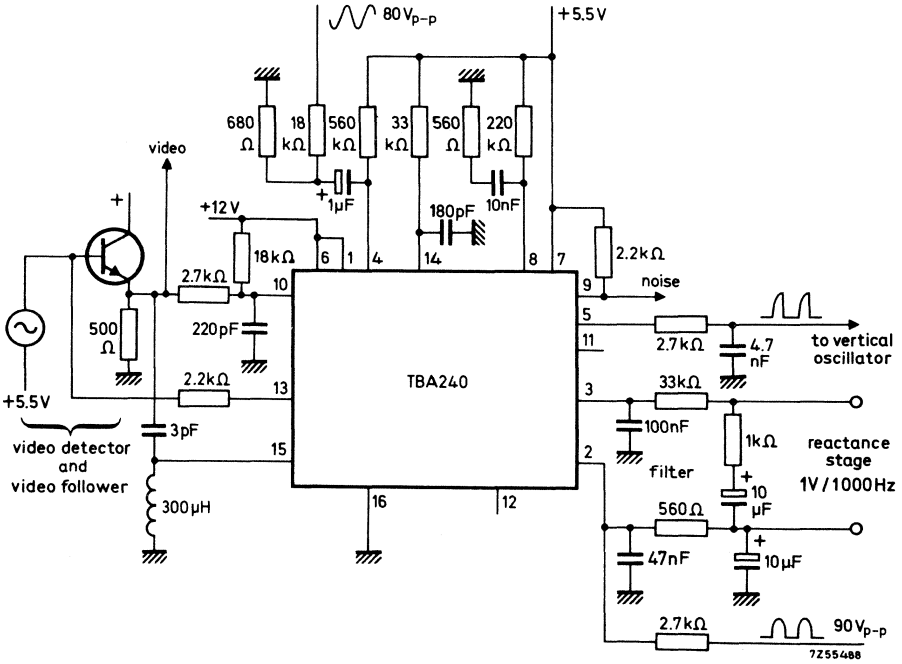
CHARACTERISTICS (continued)

Test circuit:



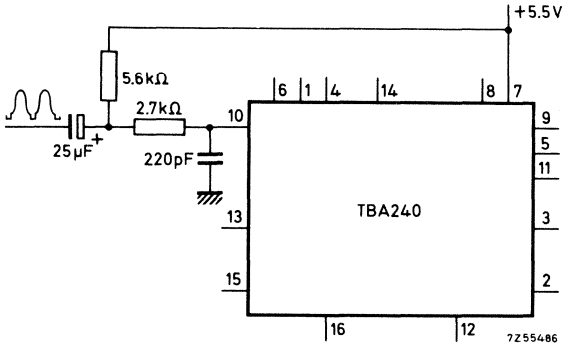
APPLICATION INFORMATION

Example of a circuit for negative modulated signals



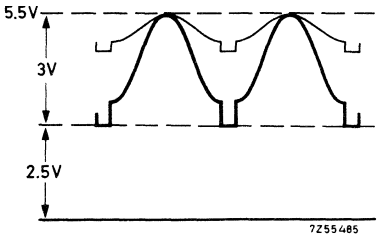
Notes:

1. The video signal is d.c. coupled to the clipping circuit and the sync pulse is sliced about 30% below top sync.
2. For positive modulation a.c. coupling is preferred (see figure below); slicing then varies between 10% and 30% below top sync, depending on picture content.



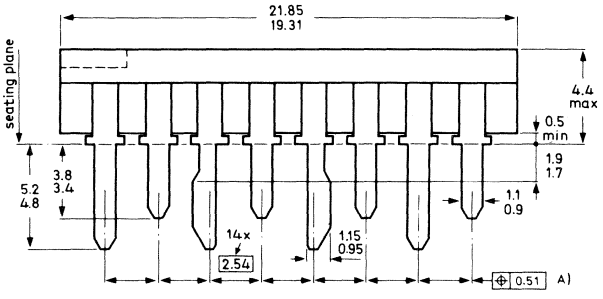
APPLICATION INFORMATION (continued)

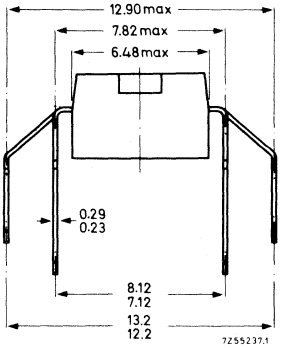
3. In the top circuit on page 6, pin 13 gives amplitude selective and pin 15 frequency selective noise inversion. The amplitude selective inversion starts when impulses pass zero in the negative direction; the frequency selective inversion, when the peak voltage across the coil exceeds 0.7 V.
4. The keying voltage on pin 4 (top circuit on page 6) is derived from the voltage across the capacitor in series with the line deflection coils; alternatively, it can be derived from a positive flyback voltage across the coils (less components), but in that case the vertical pulse may exercise a stronger influence on the line flywheel.
5. In the out-of-sync conditions the phase discriminator operates as a frequency detector; to keep the catching range from being shifted, the d.c. load at pin 3 should not be allowed to exceed about 6 μA. Good results are obtained with a reactance stage sensitivity of 1 kHz/V ($\pm$ 700 Hz catching range).
6. An integral stabilization circuit (TR12) establishes the level of the comparison sawtooth at pin 2. To avoid overloading the stabilization circuit, the direct current from pin 2 to earth must not exceed 1 mA.
7. The clipper input (pin 10) calls for a video signal with negative-going sync pulses. The figure below shows the optimum levels.
   The clipped slice is proportional to the difference between the top sync level and +5.5 V (i.e. to 3 V in figure below).

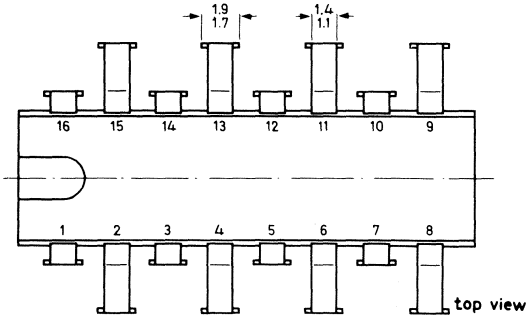


16 LEAD QUADRUPLE IN-LINE

Dimensions in mm







A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

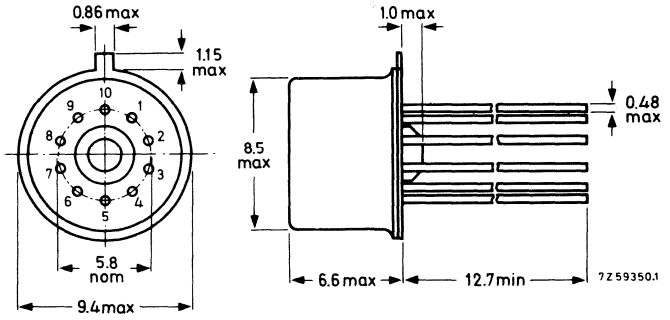
   The same precautions and limits apply as in (1) above.

VOLTAGE REGULATOR

The TBA281 is a monolithic voltage regulator. It comprises a temperature compensated reference amplifier, an error amplifier, a power series pass transistor and current limit circuitry. External series pass transistors may be added if the load current exceeds the maximum limit. The circuit can be used with adjustable current limiting and remote shut down. It features low stand-by current drain, low temperature drift and high ripple rejection. The TBA281 can be used with positive or negative supply voltages as a series, shunt, switching or floating regulator in the ambient temperature range 0 to +70°C. The TBA281 is equivalent to the 723C.

QUICK REFERENCE DATA			
Line regulation V_i = 12V to 40V	typ.	0.1	$\%V_o$
Load regulation I_L = 1 mA to 50 mA	typ.	0.03	$\%V_o$
Stand-by current drain V_i = 30V, I_o = 0	typ.	2.3	mA
Input voltage range		9.5 to 40	V
Output voltage range		2.0 to 37	V
Input-output voltage difference		3.0 to 38	V

PACKAGE OUTLINE Dimensions in mm



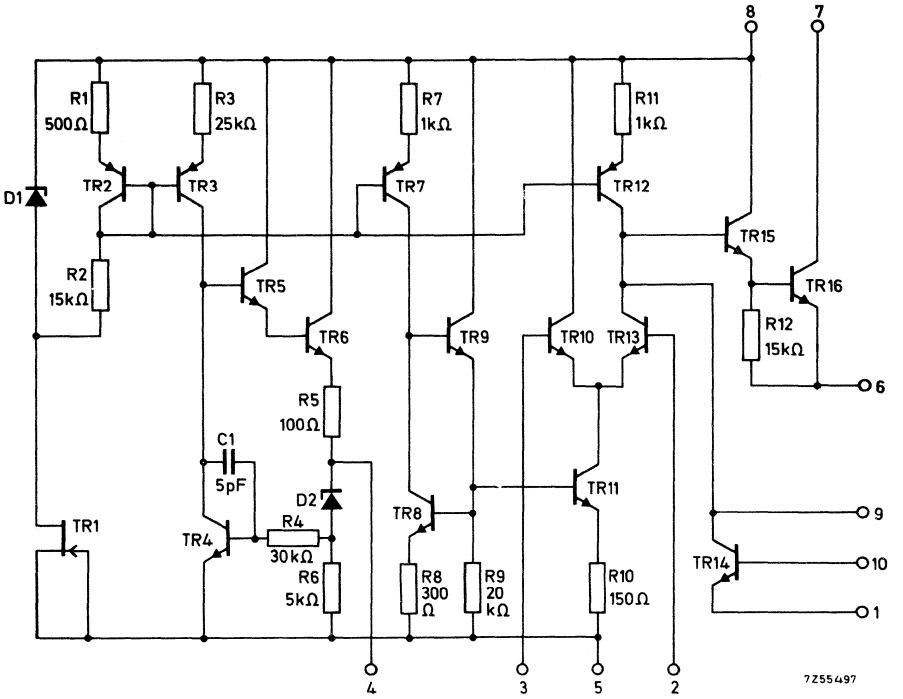
For details of pin numbering see page 3.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Input voltage	V_7	max.	40	V
Supply voltage	V_8	max.	40	V
Input-output voltage difference	V_{7-6}	max.	40	V
Currents				
Output current	$-I_6$	max.	150	mA
Current from reference amplifier output	$-I_4$	max.	15	mA
Power dissipation [1])	P_{tot}	max.	800	mW
Temperatures				
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

1) For operation above ambient temperature of 25 °C derate linearly at 6.8 mW/°C.

CIRCUIT DIAGRAM



PINNING

1. Current sense
2. Inverting input
3. Non-inverting input
4. **Reference voltage (V_{ref})**
5. Negative supply voltage ($-V_N$)
6. **Output voltage (V_o)**
7. **Collector voltage (V_C)**
8. Positive supply voltage (V_P)
9. Frequency compensation
10. Current limit

CHARACTERISTICS at $T_{amb} = 25\,^{o}C$; $V_i = V_P = V_C = 12V$; $-V_N = 0V$; $V_o = 5V$; $I_L = 5\,mA$, $R_{sc} = 0$; $C_1 = 100\,pF$; $C_{ref} = 0$ unless otherwise specified; (for testcircuit see figs. 1, 2 and 3 on page 5)

Line regulation				
at V_i = 12 to V_i = 15V		typ.	0.01	$\%V_o$
		<	0.1	$\%V_o$
at V_i = 12 to V_i = 40V		typ.	0.1	$\%V_o$
		<	0.5	$\%V_o$
at V_i = 12 to V_i = 15V; $T_{amb} = 0$ to $+70\,^{o}C$		<	0.3	$\%V_o$
Load regulation				
at I_L = 1 to I_L = 50 mA		typ.	0.03	$\%V_o$
		<	0.2	$\%V_o$
at I_L = 1 mA to I_L = 50 mA; $T_{amb} = 0$ to $+70\,^{o}C$		<	0.6	$\%V_o$
Ripple rejection at f = 50 Hz to 10 kHz				
$C_{ref} = 0$		typ.	74	dB
$C_{ref} = 5\,\mu F$		typ.	86	dB
Average temperature coefficient of output voltage at $T_{amb} = 0$ to $+70\,^{o}C$		typ.	0.003	$\%/^{o}C$
		<	0.015	$\%/^{o}C$
Short circuit current limit				
$R_{sc} = 10\Omega$; $V_o = 0$		typ.	65	mA
Reference voltage	V_4	typ.	7.15	V
			6.8 to 7.5	V
Output noise voltage at B = 100 Hz to 10 kHz				
$C_{ref} = 0$	V_n	typ.	20	μV
$C_{ref} = 5\,\mu F$	V_n	typ.	2.5	μV
Long term stability over 1000 hours			0.1	%
Stand-by current drain				
$I_L = 0$; $V_i = 30V$	I_P	typ.	2.3	mA
		<	4.0	mA
Input voltage range	V_i		9.5 to 40	V
Output voltage range	V_o		2.0 to 37	V
Input-output voltage difference	$V_i - V_o$		3.0 to 38	V

CHARACTERISTICS (continued)

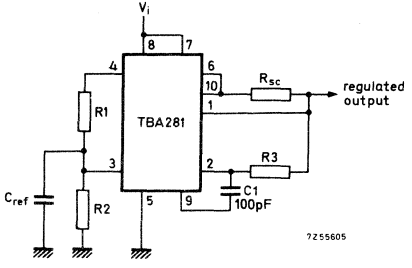


Fig. 1 [1][2]
Basic low voltage regulator
(V_O = 2 to 7V)
Typical performance
Regulated output voltage = 5V
Line regulation (ΔV_i = 3V) = 0.5mV
Load regulation (ΔI_L = 50mA) = 1.5mV

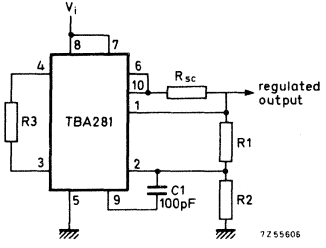


Fig. 2 [1][2]
Basic high voltage regulator
(V_O = 7 to 37V)
Typical performance
Regulated output voltage = 15V
Line regulation (ΔV_i = 3V) = 1.5mV
Load regulation (ΔI_L = 50mA) = 4.5mV

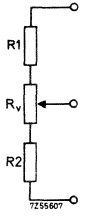


Fig. 3 [2]
Output voltage adjust

---

[1]) $R_3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift. R_3 may be eliminated for minimum component count.

[2]) For adjustable output voltage replace R_1/R_2 in fig. 1 and 2 with divider circuit shown in fig. 3.

Formulae for intermediate output voltages

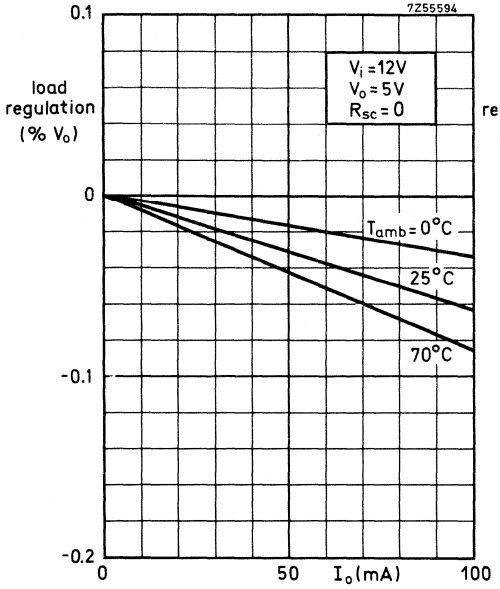
Outputs from +2 V to +7 V (fig. 1) $V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$

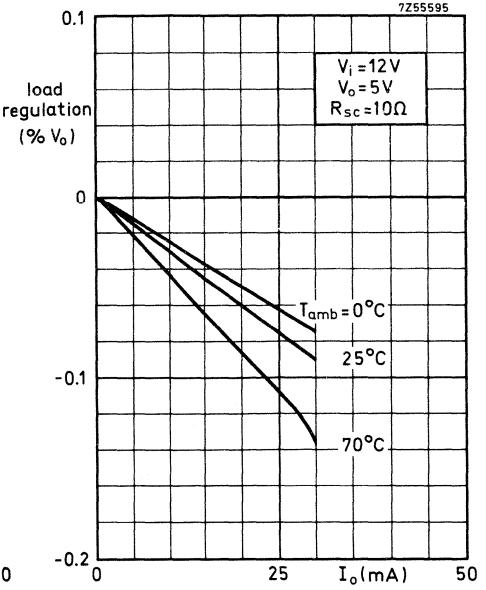
Outputs from +7 V to +37 V (fig. 2) $V_o = V_{ref} \times \frac{R_1 + R_2}{R_2}$

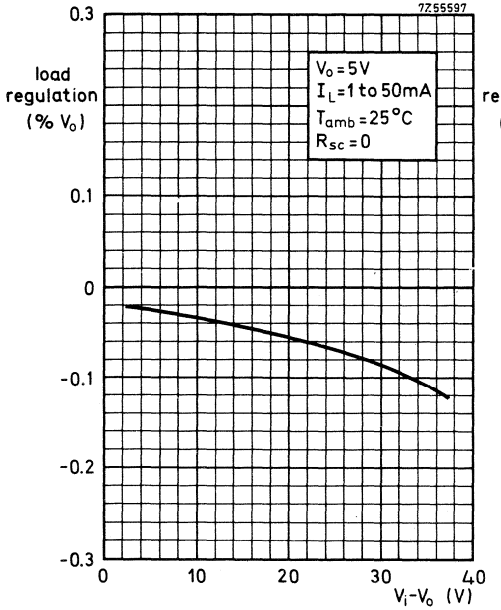
Resistor values (kΩ) for standard output voltages.

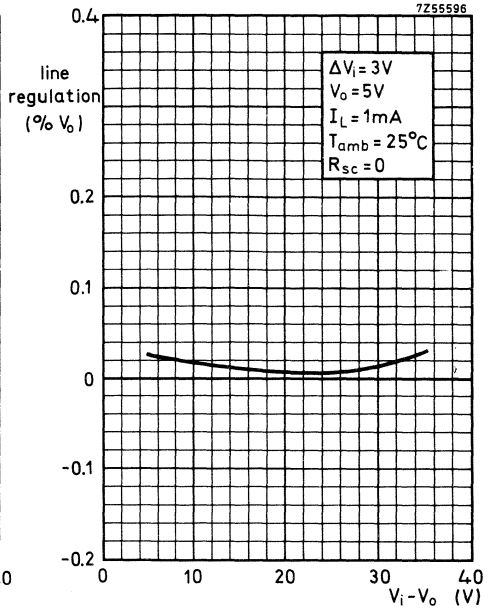
positive output voltage (V)	figure	fixed output ± 5%		adjustable output [1] ± 10% (see fig. 3)		
		R_1	R_2	R_1	R_v	R_2
+ 3.0	1	4.12	3.01	1.8	0.5	1.2
+ 3.6	1	3.57	3.65	1.5	0.5	1.5
+ 5.0	1	2.15	4.99	0.75	0.5	2.2
+ 6.0	1	1.15	6.04	0.5	0.5	2.7
+ 9.0	2	1.87	7.15	0.75	1.0	2.7
+ 12	2	4.87	7.15	2.0	1.0	3.0
+ 15	2	7.87	7.15	3.3	1.0	3.0
+ 28	2	21.0	7.15	5.6	1.0	2.0

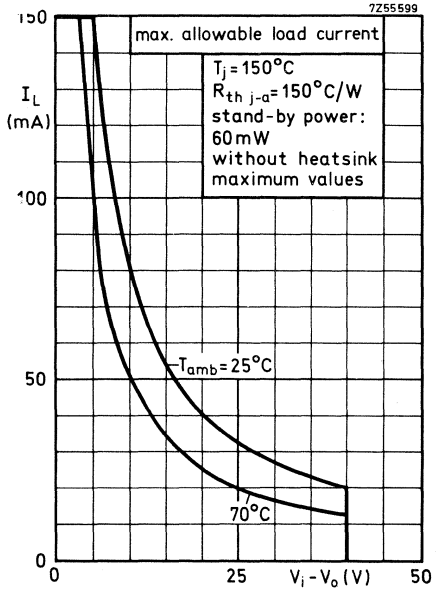
[1] For adjustable output voltage replace R_1/R_2 in fig. 1 and 2 with divider circuit shown in fig. 3 (on page 5).

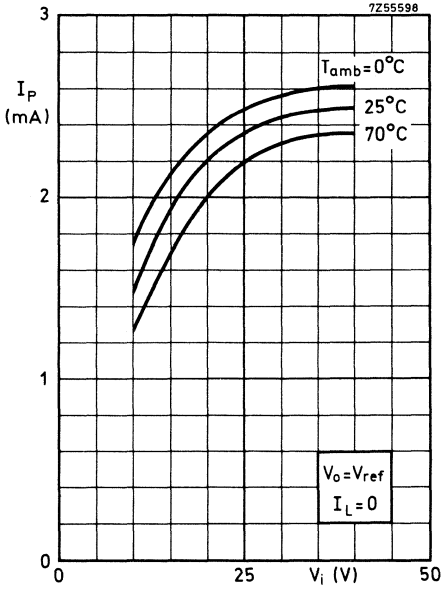

7Z55594
load regulation (% V_o)
V_i = 12V
V_o = 5V
R_{sc} = 0
T_{amb} = 0°C
25°C
70°C
0.1
0
-0.1
-0.2
0
50
100
I_o (mA)

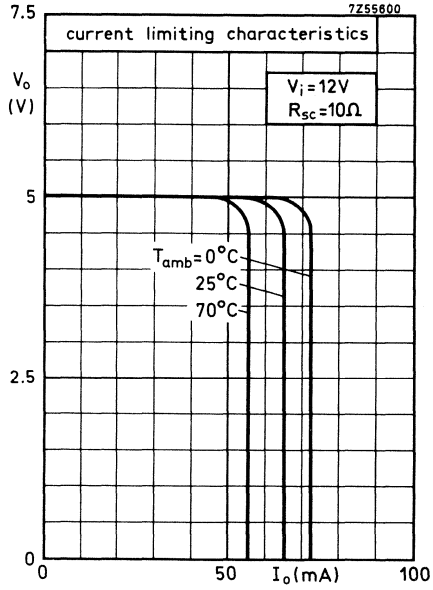

7Z55595
load regulation (% V_o)
V_i = 12V
V_o = 5V
R_{sc} = 10Ω
T_{amb} = 0°C
25°C
70°C
0.1
0
-0.1
-0.2
0
25
50
I_o (mA)

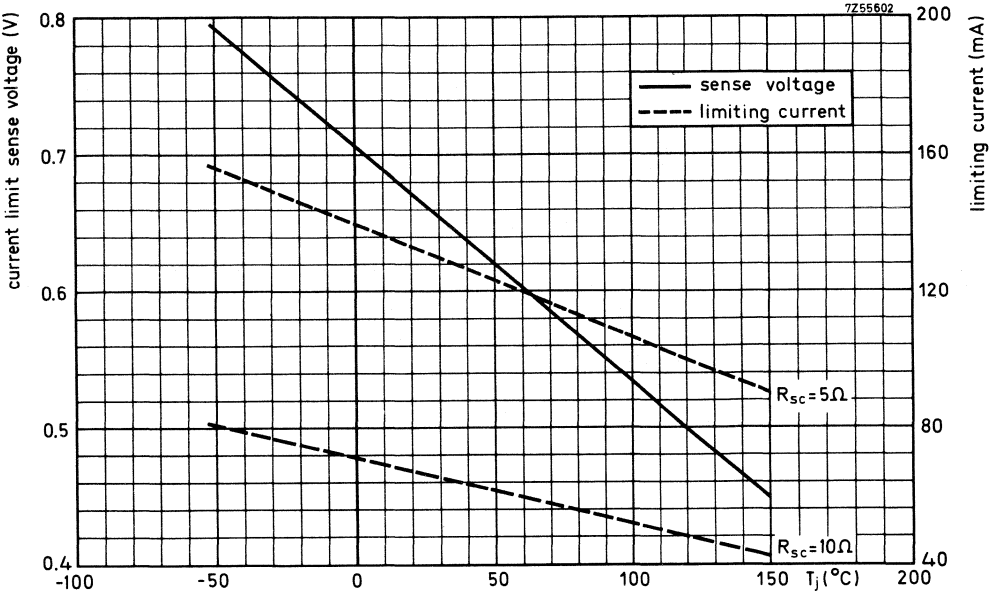

7Z55597
load regulation (% V_o)
V_o = 5V
I_L = 1 to 50mA
T_{amb} = 25°C
R_{sc} = 0
0.3
0.1
0
-0.1
-0.2
-0.3
0
10
20
30
40
V_i - V_o (V)

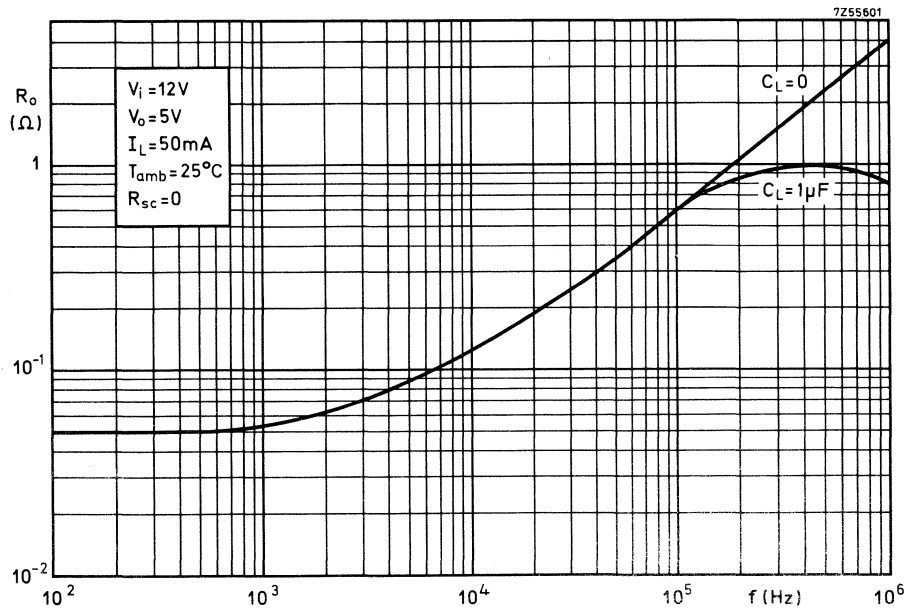

7Z55596
line regulation (% V_o)
ΔV_i = 3V
V_o = 5V
I_L = 1mA
T_{amb} = 25°C
R_{sc} = 0
0.4
0.2
0.1
0
-0.1
-0.2
0
10
20
30
40
V_i - V_o (V)

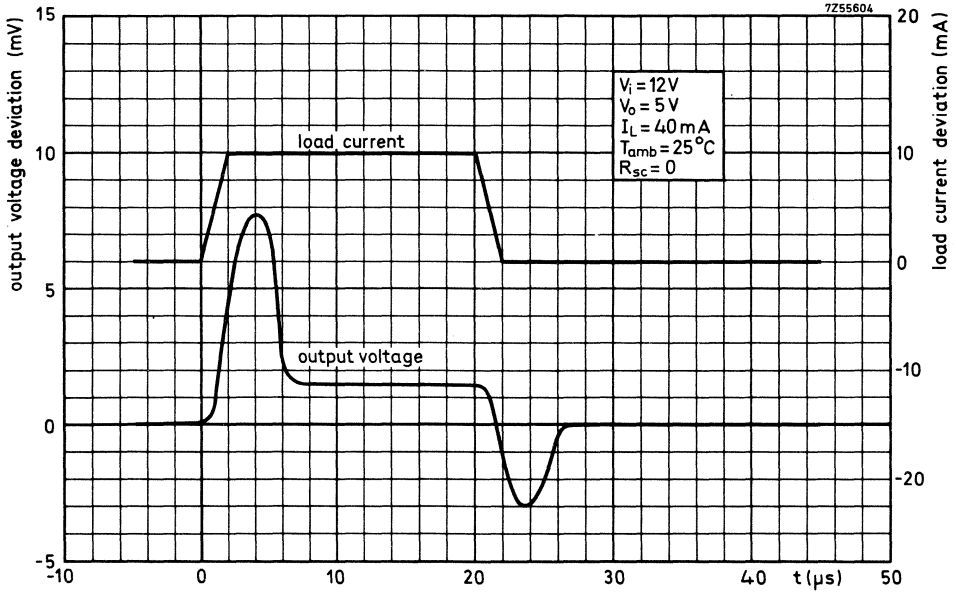

7Z55599
max. allowable load current
$T_j = 150°C$
$R_{th\ j-a} = 150°C/W$
stand-by power:
60 mW
without heatsink
maximum values
I_L (mA)
150
100
50
0
$T_{amb} = 25°C$
70°C
0
25
50
$V_i - V_o$ (V)

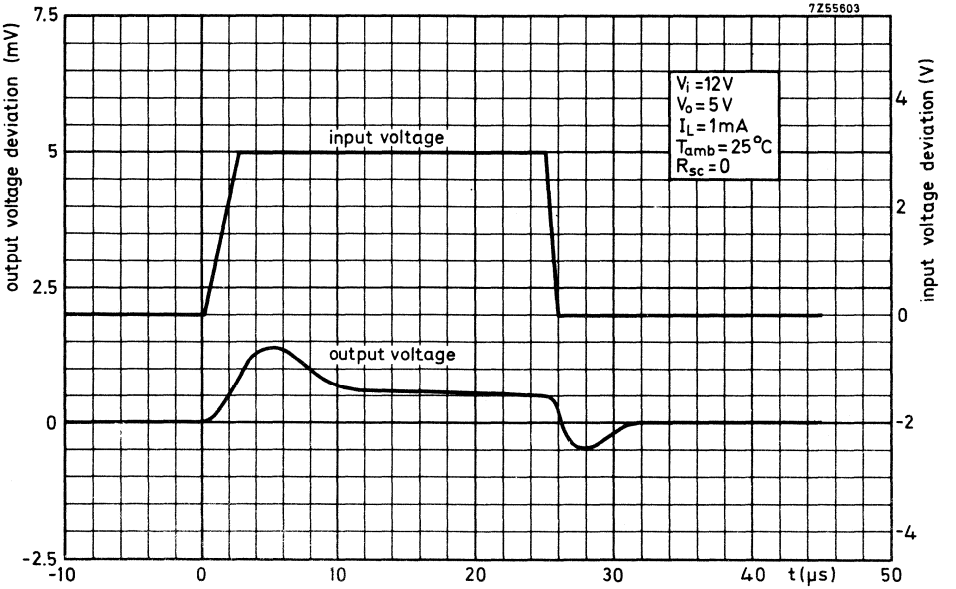

7Z55598
I_P (mA)
3
2
1
0
$T_{amb} = 0°C$
25°C
70°C
$V_o = V_{ref}$
$I_L = 0$
0
25
50
V_i (V)


7Z55600
current limiting characteristics
$V_i = 12V$
$R_{sc} = 10\Omega$
V_o (V)
7.5
5
2.5
0
$T_{amb} = 0°C$
25°C
70°C
0
50
100
I_o (mA)


7Z55602
current limit sense voltage (V)
limiting current (mA)
sense voltage
limiting current
R_{sc}=5Ω
R_{sc}=10Ω
0.8
0.7
0.6
0.5
0.4
200
160
120
80
40
-100
-50
0
50
100
150
200
T_j(°C)


7Z55601
R_o (Ω)
V_i=12V
V_o=5V
I_L=50mA
T_{amb}=25°C
R_{sc}=0
C_L=0
C_L=1μF
1
10^{-1}
10^{-2}
10^2
10^3
10^4
10^5
10^6
f (Hz)


7Z55604
output voltage deviation (mV)
load current deviation (mA)
load current
output voltage
V_i = 12V
V_o = 5V
I_L = 40mA
T_{amb} = 25°C
R_{sc} = 0
t (μs)


7Z55603
output voltage deviation (mV)
input voltage deviation (V)
input voltage
output voltage
V_i = 12V
V_o = 5V
I_L = 1mA
T_{amb} = 25°C
R_{sc} = 0
t (μs)

INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

DTL = FC family
MOS = FD family
TTL = FJ family

TTL = FJ family
L = Linear integrated circuits

General	
D T L	FC family
T T L	FJ family
MOS	FD family
Linear integrated circuits	

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